

# Buck Pulse Width Modulator Stepdown Voltage Regulator

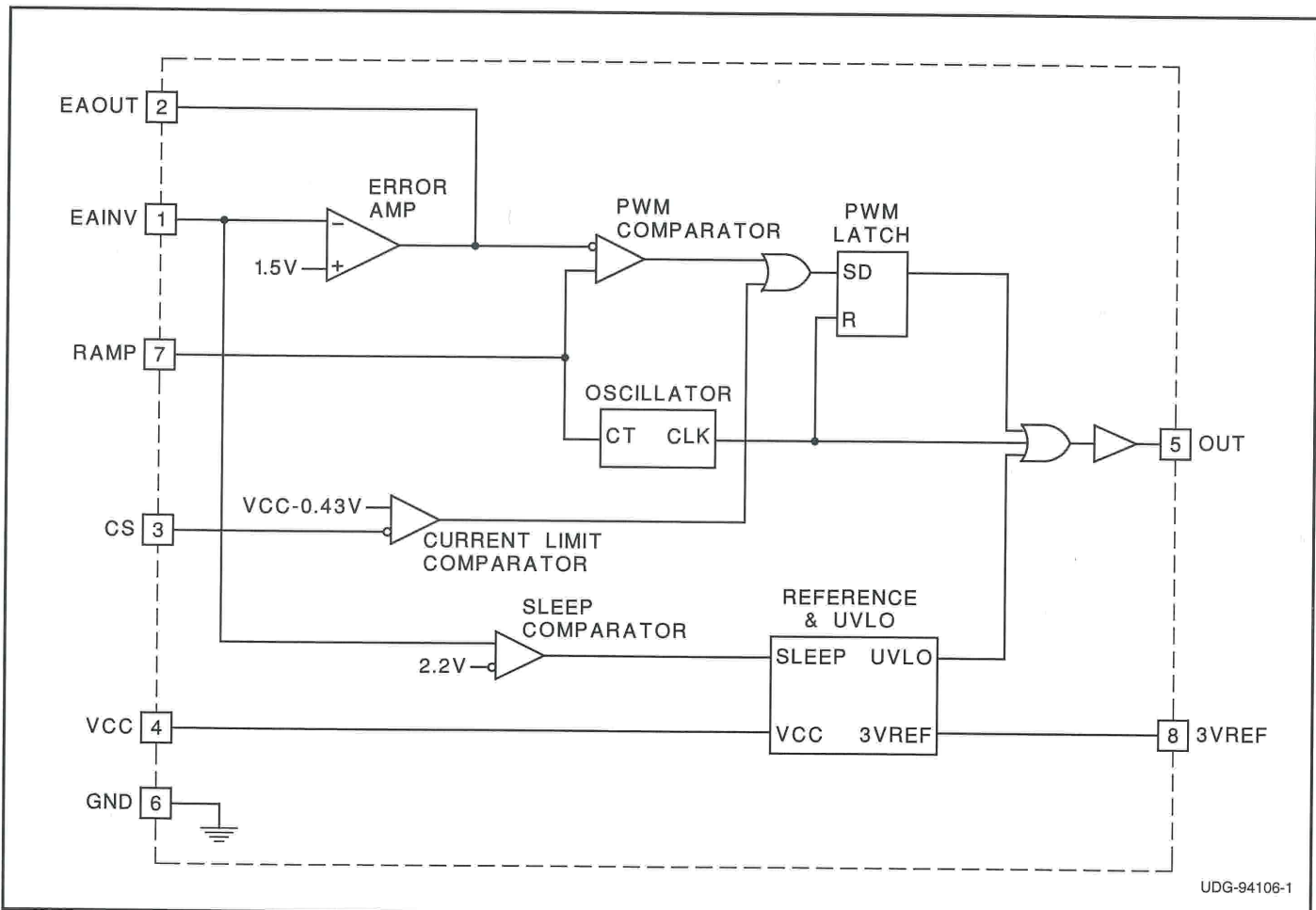
## FEATURES

- Simple Single Inductor Buck PWM Stepdown Voltage Regulation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50µA Sleep Mode Current

## DESCRIPTION

The UC3573 is a Buck pulse width modulator which steps down and regulates a positive input voltage. The chip is optimized for use in a single inductor buck switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3573 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Input current can be sensed and limited to a user determined maximum value. In addition, a sleep comparator interfaces to the UVLO circuit which turns the chip off when the input voltage is below the UVLO threshold. This reduces the supply current to only 50µA, making the UC3573 ideal for battery powered applications.

## BLOCK DIAGRAM

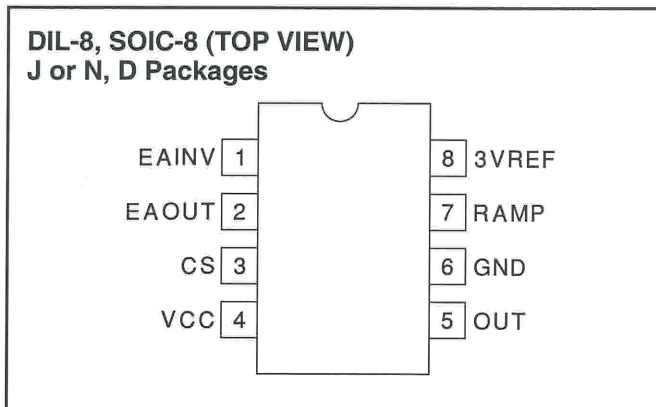


## ABSOLUTE MAXIMUM RATINGS

VCC	35V
EAINV	-0.6V to VCC
I <sub>EAOUT</sub>	25mA
RAMP	-0.3V to 4V
CS	-0.3V to VCC
I <sub>OUT</sub>	-0.7A to 0.7A
I <sub>3VREF</sub>	-15mA
Storage Temperature	-65°C to +150°C
Junction Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

## CONNECTION DIAGRAMS



**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, these parameters apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1573,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2573, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3573,  $V_{CC} = 5\text{V}$ ,  $C_T = 680\text{pF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Reference Section</b>					
3VREF		2.94	3	3.06	V
Line Regulation	$V_{CC} = 4.75$ to $30\text{V}$		1	10	mV
Load Regulation	$I_{3VREF} = 0$ to $-5\text{mA}$		1	10	mV
<b>Oscillator Section</b>					
Frequency	$V_{CC} = 5\text{V}$ , $30\text{V}$	85	100	115	kHz
<b>Error Amp Section</b>					
EAINV	EAOUT = $2\text{V}$	1.45	1.5	1.55	V
I <sub>EAINV</sub>	EAOUT = $2\text{V}$		-0.2	-1	$\mu\text{A}$
AVOL	EAOUT = $0.5\text{V}$ to $3\text{V}$	65	90		dB
EAOUT High	EAINV = $1.4\text{V}$	3.6	4	4.4	V
EAOUT Low	EAINV = $1.6\text{V}$		0.1	0.2	V
I <sub>EAOUT</sub>	EAINV = $1.4\text{V}$ , EAOUT = $2\text{V}$	-350	-500		$\mu\text{A}$
	EAINV = $1.6\text{V}$ , EAOUT = $2\text{V}$	7	20		mA
Unity Gain Bandwidth	$T_J = 25^\circ\text{C}$ , $F = 10\text{kHz}$	0.6	1		MHz
<b>Current Sense Comparator Section</b>					
Threshold (referred to VCC)		-0.39	-0.43	-0.47	V
Input Bias Current	CS = VCC		150	800	nA
CS Propagation Delay			400		ns
<b>Gate Drive Output Section</b>					
OUT High Saturation	$I_{OUT} = 0$		0	0.3	V
	$I_{OUT} = -10\text{mA}$		0.7	1.5	V
	$I_{OUT} = -100\text{mA}$		1.5	2.5	V
OUT Low Saturation	$I_{OUT} = 10\text{mA}$		0.1	0.4	V
	$I_{OUT} = 100\text{mA}$		1.5	2.2	V
Rise Time	$T_J = 25^\circ\text{C}$ , $C_{LOAD} = 1\text{nF} + 3.3\text{ Ohms}$		30	80	ns
Fall Time	$T_J = 25^\circ\text{C}$ , $C_{LOAD} = 1\text{nF} + 3.3\text{ Ohms}$		30	80	ns
<b>Pulse Width Modulator Section</b>					
Maximum Duty Cycle	EAINV = $1.4\text{V}$		92	96	%
Minimum Duty Cycle	EAINV = $1.6\text{V}$			0	%
Modulator Gain	EAOUT = $1.5\text{V}$ to $2.5\text{V}$	25	35	45	%/V
<b>Undervoltage Lockout Section</b>					
Start Threshold		3.5	4.2	4.5	V
Hysteresis		100	200	300	mV

**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, these parameters apply for  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for the UC1573,  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  for the UC2573, and  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  for the UC3573,  $V_{CC} = 5\text{V}$ ,  $C_T = 680\text{pF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Sleep Mode Section</b>					
Threshold		1.8	2.2	2.6	V
<b>Supply Current Section</b>					
$I_{VCC}$	$V_{CC} = 30\text{V}$		9	12	mA
$I_{VCC}$	$V_{CC} = 30\text{V}, E_{AINV} = 3\text{V}$		50	150	$\mu\text{A}$

## PIN DESCRIPTIONS

**3VREF:** Precision 3V reference. Bypass with 100nF capacitor.

**CS:** Peak current limit sense pin. Senses the current across a current sense resistor placed between  $V_{CC}$  and source of the PMOS Buck switch. OUT will be held high (PMOS buck switch off) if  $V_{CC} - CS$  exceeds 0.4V.

**EAINV:** Inverting input to error amplifier. VOUT sense feedback connected to this pin. The non-inverting input of the error amplifier is internally connected to:

$$\frac{3V_{REF}}{2} \text{ Volts.}$$

Connecting the EAINV pin to an external voltage greater than 2.6V commands the chip to go into a low current sleep mode.

**EAOUT:** Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

**GND:** Circuit Ground.

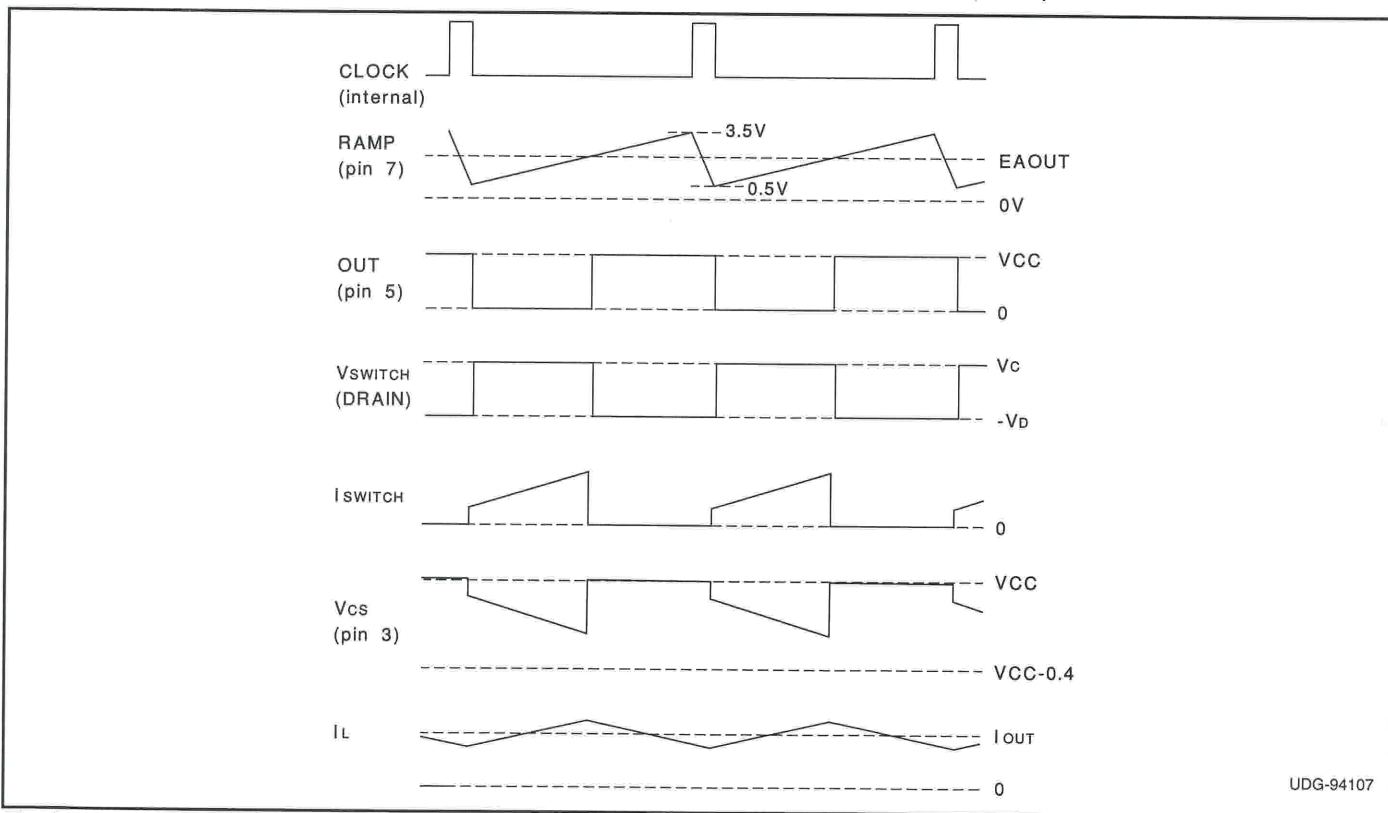
**OUT:** Gate drive for external PMOS switch connected between  $V_{CC}$  and the flyback inductor. OUT drives the gate of the PMOS switch between  $V_{CC}$  and GND.

**RAMP:** Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \cdot C_{RAMP}}$$

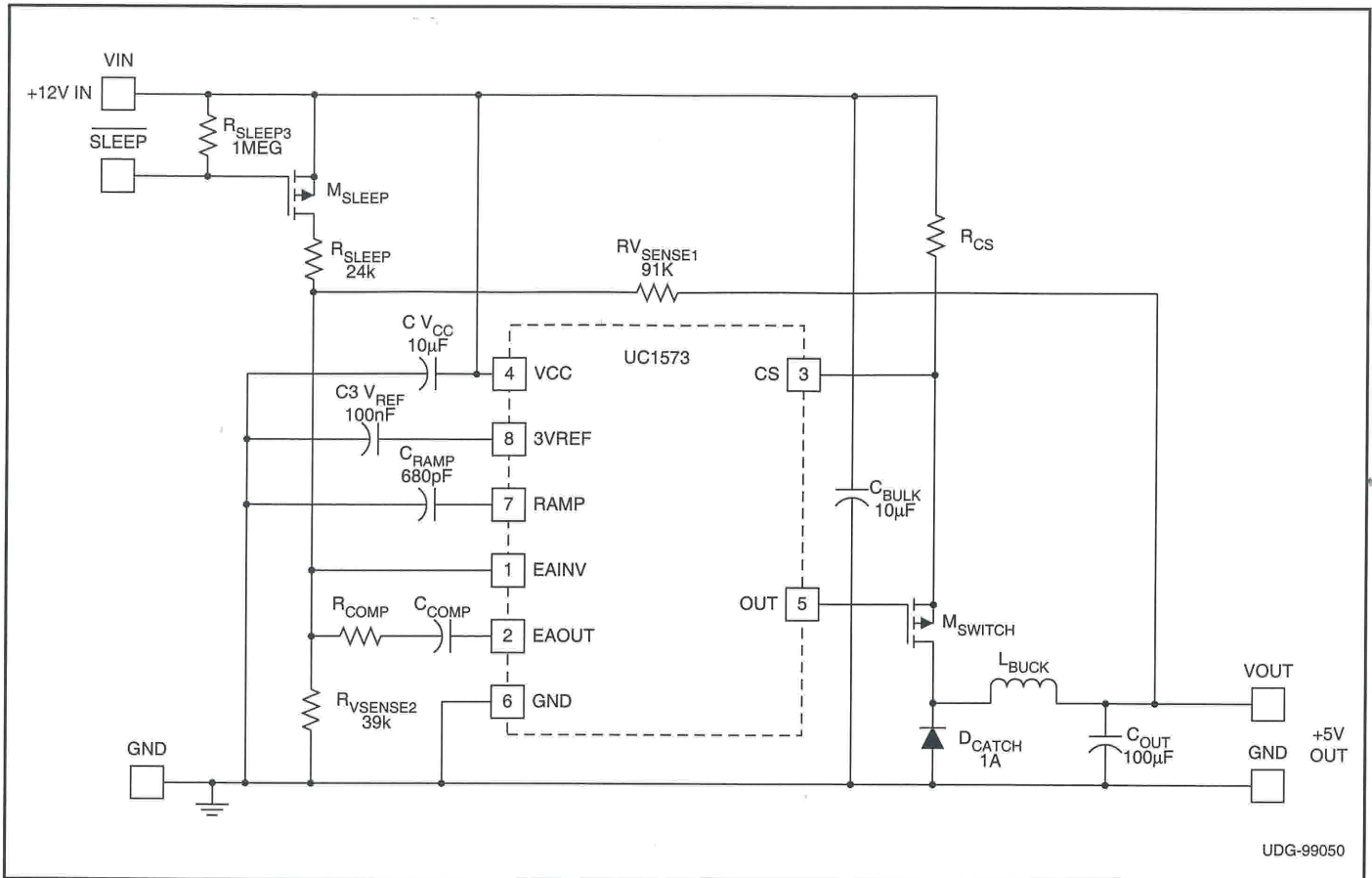
Recommended operating frequency range is 10kHz to 200kHz.

**VCC:** Input voltage supply to chip. Range is 4.75V to 30V. Bypass with a 1 $\mu\text{F}$  capacitor.



Typical Waveforms.

**TYPICAL APPLICATION: 12V TO 5V BUCK CONVERTER**



**REVISION HISTORY**

SLUS346 to SLUS346A, July 2010:

Changed Supply Current I<sub>VCC</sub> units from A to μA

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2573D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2573D	<a href="#">Samples</a>
UC2573DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2573D	<a href="#">Samples</a>
UC2573DTR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2573D	<a href="#">Samples</a>
UC3573D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3573D	<a href="#">Samples</a>
UC3573DTR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3573D	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2573DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3573DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2573DTR	SOIC	D	8	2500	340.5	338.1	20.6
UC3573DTR	SOIC	D	8	2500	353.0	353.0	32.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UC2573D	D	SOIC	8	75	507	8	3940	4.32
UC2573DG4	D	SOIC	8	75	507	8	3940	4.32
UC3573D	D	SOIC	8	75	507	8	3940	4.32



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated