Selecting an A/D Converter

ABSTRACT

Selecting an A/D converter for a digitizing system can seem an arduous task. There are a plethora of converters available in the marketplace from a wide variety of manufacturers. The process of selection can be simplified by means of a checklist, organized by importance. This bulletin is intended to walk the reader through this checklist, describe the factors in some detail, learn which manufacturer's specifications apply to these factors and how to interpret those specifications.

The selection checklist can be broken up into two areas — primary facts which cannot be compromised, and secondary factors which may allow the designer some flexibility.

PRIMARY

- What is the required level of system accuracy?
- How many bits of resolution are required?
- What is the nature of the analog input signal?
- How fast must the converter operate (conversion speed)?
- What are the environmental conditions?
- Is a track-and-hold circuit required?

SECONDARY

- Does the system have multiple channels?
- Should the reference be internal or external?
- What are the drive amplifier requirements?
- What are the digital interface requirements?
- What type of digital output format is required?
- What are the timing conditions?

Not shown in the A/D converter checklist is the most important element in the process: the first step is the complete definition of the design objectives for the digitizing system. The converter checklist can be used as a guideline to insure all important factors are considered. The objective is to find an A/D converter which fits into the system design, not vice versa.

Secondly, once the converter selection process has begun, it is very important to have a complete understanding of the specifications. Understand what the absolute requirements are, and insist on guaranteed specifications for those parameters. Although most reputable manufacturers' typical specifications have some measure of validity, never depend on those values if they are critical in the system's performance. Understand the test conditions of the specifications, making certain they closely match the operating conditions in the digitizing system.

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1 Primary Factors

1.1 Accuracy

The accuracy of the overall system must be considered. In most cases, the A/D converter is only one element of the digitizing system. For example, if the overall system accuracy requirement is 0.012% (12-bits), the A/D converter usually needs to be more accurate, perhaps 0.006% (13-bits) which would allow the analog front end an error budget of one LSB (least significant bit). One good rule of thumb to follow when selecting analog components for a digitizing system is for each component to be five to ten times more accurate than the total system accuracy. Resolution should not be confused with accuracy—these two terms are somewhat exclusive. Resolution simply refers to the theoretical number of states (2^n) which the analog input can be resolved into, where *n* is the number of bits of resolution. Accuracy indicates how close the converter comes to the theoretical limits. For this section, accuracy will be examined in the time domain, where specifications are static (DC). The four key static accuracy specifications are: differential nonlinearity (DNL), integral nonlinearity (INL), offset error and gain error. The ideal transfer function of a 3-bit A/D converter is shown in Figure 1.
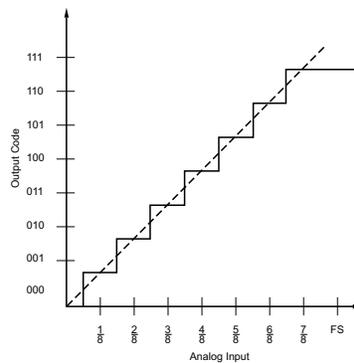
Figure 1. Ideal 3-Bit A/D Converter Transfer Function

1.1.1 Offset Error

The transfer function of a 3-bit A/D converter with an offset error of +1 LSB is shown in Figure 2. Output code is shown on the Y-axis and analog input amplitude is shown on the X-axis. Offset error is the amount by which the first code transition (from 000 to 001) deviates from the ideal position at an input equivalent to 0.5 LSB. Another way to consider offset error is to examine the distance between X-Y intercept on the graph and where the straight line drawn through the actual transfer function intercepts the X-axis. Offset error will cause the entire transfer function to shift along the Y-axis (output code is the dependent variable). Offset error is commonly expressed as LSBs, volts or percentage of full-scale range (%FSR).
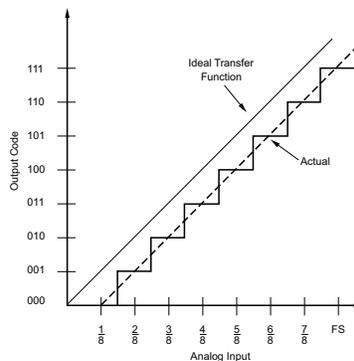
Figure 2. Offset Error of +1LSB

1.1.2 Gain Error

Figure 3 is an illustration of a 3-bit A/D converter transfer function with a gain error. From this figure, gain error can be described as the deviation of the straight line through the transfer function at the intercept of full scale. It can also be expressed as the deviation from the ideal gain slope of +1. Gain error is usually expressed as a percentage of full scale range (%FSR), but can also be specified in volts or LSBs. Gain error is dominated by errors in the converter's reference voltage, since the value of the reference determines the full scale range of the device.
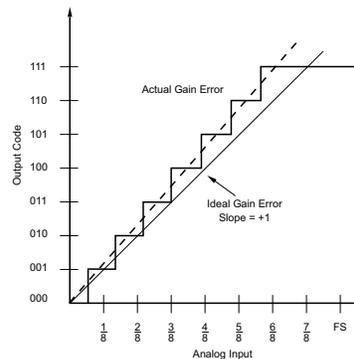

Figure 3. Positive Gain Error

1.1.3 Differential Nonlinearity

Differential nonlinearity is used to describe deviations from the ideal transition voltages in the converter's transfer function. Figure 4 illustrates an example of DNL error.
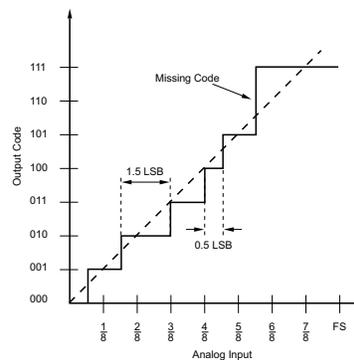

Figure 4. Differential Nonlinearity

Each code transition should occur at an interval equal to 1 LSB. For example, with a 3-bit A/D, if the first transition occurs at 1/8 of full scale (0.125 FSR), the second transition will ideally occur at 0.250 FSR. The deviation from that ideal transition is the differential linearity error for that unique code. The DNL specification for the converter should describe the worst case transition of all the possible transitions of the converter. When the LSB is referred to the resolution of the converter, a DNL error of −1 LSB implies a code is missing. Most converters are specified with "no missing codes" to some level of accuracy, typically equivalent to the resolution of the A/D. In some cases, no missing codes are specified at less than the resolution of a given converter. For example, many 16-bit converters are guaranteed to have no missing codes to 15 bits. A 16-bit converter with no missing codes would have 65,535 possible output codes. If DNL is specified with no missing codes to 16-bits, all of the possible output codes must exist. Note the "no missing codes" specification does not give the user any information about the code width; simply that some portion of every output code will be present. If the 16-bit converter has a specification of −1 LSB, the output is only guaranteed to have 15-bits of information at any given output state. If the converter is specified with no missing codes to 15 bits, then the output is only guaranteed to have 15 bits of information at any given output size. Positive errors indicate long codes, and have no real limit on their value, irrespective of resolution.

A simple test for DNL is to servo the input voltage until a transition is detected, and then measure the voltage required to force that transition. The input voltage required to force the next transition can then be measured, with the difference between the two transitions – 1 LSB defined as the DNL error for that transition. One caution in testing for DNL is the presence of noise in the A/D converter. Since the noise is usually Gaussian, averaging the values of the transition will yield true DNL results.

1.1.4 Integral Nonlinearity

Integral nonlinearity is used to describe the overall shape of the transfer function of the A/D converter. This error is sometimes referred to as static linearity or absolute linearity. Figure 5 illustrates an example of integral nonlinearity referred to end points and Figure 6 is an example of integral nonlinearity referred to the best-fit line. For the end point linearity, a straight line is drawn between the converter's offset and gain intercept points, the transfer function is plotted against that straight line. The maximum deviation from the line is the worst case integral nonlinearity. For the best-fit example, the transitions are used in a least-squares calculation, the line of best-fit is drawn, and the transfer function is plotted against that line. As in the example of the end point linearity, the maximum deviation from the best-fit line describes the integral nonlinearity of the converter. Integral nonlinearity can also be found by summing and integrating the DNL errors that occur with the same polarity. A strict definition of INL is the measure of maximum deviation of the actual transition points in an A/D's transfer function from the chosen straight line (ideal, best-fit or endpoint).
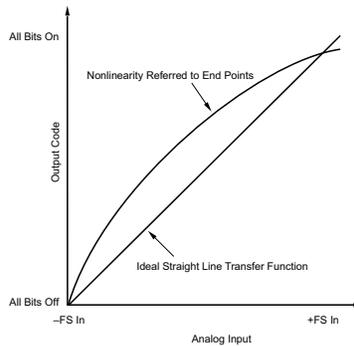
Figure 5. Integral Nonlinearity Referred to Inputs
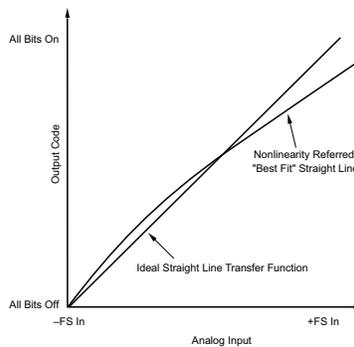
Figure 6. Integral Nonlinearity Referred to Best-Fit Straight Line

1.2 *Dynamic Specifications*

Dynamic specifications are expressed in the frequency domain, often using Fast Fourier Transforms (FFTs) to derive the specifications. In order to easily recognize where these specifications are found on an FFT, refer to Figure 7.

This particular FFT was derived from an ADC614, a 14-bit 5.12-MHz sampling A/D converter. The input frequency for this test was a 2.35-MHz sine wave.

The fundamental input signal (A) is shown at 2.35 MHz, which was the frequency of the analog input. Note that the power is down from full scale. This is known as headroom (E), which is used to avoid clipping of the input signal in the case of offsets from the A/D converter or input signal generator. Headroom in most FFT testing is typically 0.5 dB. For purposes of illustration, headroom has been expanded in Figure 7.
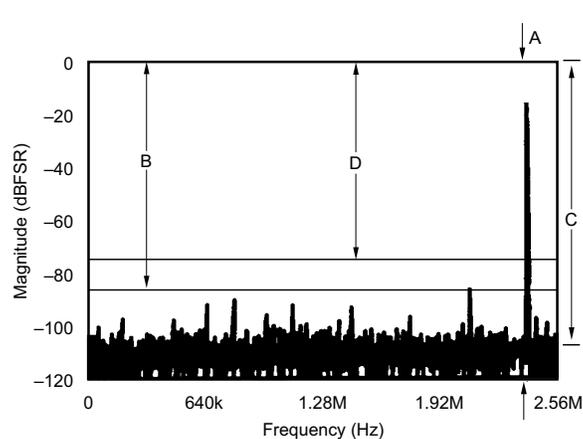
Figure 7. Dynamic Specifications

Spurious-free dynamic range (SFDR) of the converter is defined as the distance in dB from the fundamental amplitude to the peak spur level (B) in the output frequency spectrum, not necessarily limited to harmonic components of the fundamental.

The average noise floor (C) is derived from both the average noise of the A/D converter and the FFT itself. The ideal noise floor of the FFT is expressed as:

$6.02n + 1.76 + 10\log(m/2)$

where

- n = A/D resolution
- m = FFT points

The noise performance of the A/D converter itself (D) is expressed as signal-to-noise ratio, or SNR. The signal is the rms power of the input fundamental, and the noise is the rms sum of all nonfundamental harmonics in the Nyquist band, excluding DC.

Theoretical SNR = $6.02n + 1.76$

where

- n = resolution

A good rule of thumb for acceptable SNR in an A/D converter is to multiply the resolution by six. For example, good SNR for an 8-bit A/D should be 48 dB, and for a 12-bit A/D, 72 dB. Because it is very difficult to scale down $1/f$ noise in amplifiers used in the internal circuitry of high resolution (≥ 12-bit) A/D converters, the "times 6" rule of thumb does hold for these higher resolution converters. For such high resolution converters, SNR is also somewhat dependent upon the input signal frequency. For a given sampling frequency, f_S, the theoretical rms quantization noise in the bandwidth of input frequencies from DC to $f_S/2$ is given as q/√n, where q is the weight of the LSB and n is the number of bits. When the ratio of the input signal frequency to sampling rate frequency is decreased, the quantization noise is dispersed over a narrower bandwidth, resulting in an increase in noise over the analog input bandwidth. Figure 8 is a plot of SNR versus input frequency for Burr-Brown's ADS602, a 12-bit 1.0MSPS sampling A/D converter. There is very little degradation in SNR as the input frequency increases for this converter. For higher speed or higher resolution converters, there will be more degradation in SNR with increasing input frequencies. This is primarily due to difficulties in reducing wideband noise in the sample-and-hold as well as problems reducing internal $1/f$ noise.
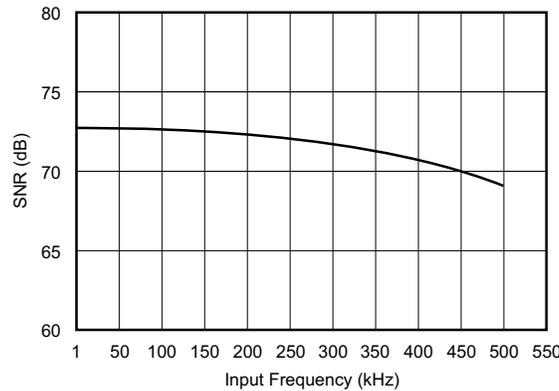
Figure 8. SNR vs Input Frequency for ADS602

Other dynamic specifications of interest include total harmonic distortion (root-sum-square of the power in the fundamental's harmonics), signal-to-noise ratio with distortion (SINAD) which includes harmonic power in the SNR calculation and effective bits (ENOB), an alternative expression for SNR. A useful approximation of ENOB is given by:

ENOB = (SNR − 1.76 dB) / 6.02

1.3 System Accuracy and Resolution

The selection process should normally start with determining the required accuracy of the A/D converter, which is indicated by the overall accuracy requirements of the complete digitizing system. First of all, it is fundamentally important to define the difference between *resolution* and *accuracy*. Resolution only indicates what the theoretical accuracy can be; it does not imply accuracy to a given level. An *n*-bit A/D converter is capable of converting a infinite range of analog input values into a finite range of $2^n - 1$ digital steps, where *n* is the resolution of the converter. Table 1 illustrates the relationship between number of bits and values for LSBs for some common A/D input ranges.

Table 1. LSB Values vs Resolution and Input Range

BITS	CODES	LSB VALUE		
		20 V RANGE	**5 V RANGE**	**2 V RANGE**
8	256	78.1 mV	19.5 mV	7.81 mV
10	1024	19.5 mV	4.88 mV	1.95 mV
12	4096	4.88 mV	1.22 mV	488 µV
14	16384	1.22 mV	305 µV	122 µV
16	65536	305 µV	76.3 µV	30.5 µV
18	262144	76.3 µV	19.1 µV	7.63 µV
20	1048576	19.1 µV	4.78 µV	1.91 µV

Accuracy is used to describe how close a converter comes to meeting its theoretical resolution. Accuracy in a converter is limited by the theoretical quantization noise, discrete nonlinearities in the transfer function, and by additional sources of noise in the A/D converter circuitry. As an example of determining system accuracy in the time do- main, assume the goal is to measure a temperature with a span of 1000°C within an accuracy of 0.25°C. The required system resolution will be 1000/.25, or 4000 codes. Selecting a 12-bit converter will provide a resolution of 4096 codes. The accuracy, assuming the DNL error for the converter is one-half LSB, will be 0.244°C.

Unfortunately, the A/D converter is not the only element affecting accuracy in the digitizing system. Often contained in the front-end analog signal conditioning pathway are instrumentation amps, op-amps, multiplexers and drive amplifiers. The total error budget can be found by computing the root-sum-square errors of the signal conditioning components. As an example of the 12-bit system described above, assume the following errors as shown in Table 2.

Table 2. Typical Errors in a 12-Bit Data Acquistion System

ERROR SOURCE	TYPICAL PART	TYPICAL ERROR
Instrumentation Amp	INA114	0.003%
Multiplexer	MPC508	0.0025%
Drive Amp	OPA602	0.01%
A/D Converter	ADS7806	0.01%

As a first order approximation, the total error for this system would be 0.0147%. For a ±10V input range, this would imply an error of 2.93 mV. Considering FSR (20 V) and the need to have 4000 increments (1000°C/0.25°), the system must be accurate to 5 mV (20/4000). This data acquisition system is adequate (typically) for the application requirements. In the case of frequency domain accuracy, there will be pre-existing requirements for maintaining spectral purity which will aid the user in selecting the proper A/D converter.

1.4 Conversion Speed

Conversion speed indicates how fast the converter will operate. For sampling A/D converters, the conversion rate is often expressed in samples per second. For example, ADS7804 accepts a conversion clock of up to 100 kHz, so it is said to have a sample rate of 100 kSPS. Conversion time can also be expressed in terms of frequency or in units of time. A 100 kHz converter has a conversion time of 10µs.

Two main elements to consider when selecting a sample rate are the input signal bandwidth and the required update rate. When digitizing a signal, the Nyquist rule must be followed. The Nyquist rule states that sampling rate of the A/D must be at least twice that of the input signal bandwidth of interest. This does not mean the fundamental input frequency must be limited to one-half of the sample rate; it only refers to the *bandwidth* of the input signal. The ability to process fundamental input signals which are greater than Nyquist allow for undersampling. Techniques of undersampling are discussed in detail in an article, *The Benefits of Undersampling*, published in EDN magazine, July 12, 1994.

Exercising an A/D converter at close to Nyquist rate has some drawbacks. Although the converter is capable of digitizing signal bandwidths between DC and one-half the sample rate, two new problems must be considered. First, the analog input bandwidth of the sampling mechanism may be inadequate to process the signal without introducing distortion. The second problem with Nyquist rate sampling is aliasing. Most input signals contain harmonics of the fundamental, which will be digitized by the converter. Additionally, there may be interactions between the high-frequency input harmonics and the clock signals inside the converter, causing unwanted harmonics to be digitized. It is usually necessary to filter out the input harmonics using a low-pass or band-pass filter. Passing an input signal close to Nyquist while attempting to filter out harmonics above Nyquist requires a rigorous "brick wall" type of filter, which may be prohibitively expensive. It is preferable to select a converter whose sample rate is several times greater than the analog input bandwidth, to avoid expensive high-order input filters.

When designing a multiple channel system, it may be cost beneficial to use a single higher speed A/D in place of multiple converters. The cost of higher speed monolithic industrial converters has come down considerably, enabling the user to realize a large cost reduction in multiple channels systems. There also may be benefits in reducing the cost of input filtering, as discussed in the previous paragraph.

1.5 Analog Input Signal

It is obviously necessary to know the nature of the analog input signal prior to selecting the proper A/D converter. Some important considerations include:

- Is the signal ac or DC?
- Does the signal contain discontinuities?
- What is the signal's characteristic source impedance?
- Is the signal noisy?
- What is the signal amplitude?

First of all, consider whether the signal is slowly varying or rapidly varying. Very slowly varying signals can be also considered DC, especially if the conversion rate is high. For example, a 100-kHz input looks like DC to a 10-MSPS converter. Slowly varying signals will generally not require an input sample-and-hold circuit, and also will work well with many different architectures. For AC signals, it may be more effective to consider frequency domain performance, since the A/D is now digitizing waveforms as opposed to voltage levels (DC). In many AC applications, absolute scale errors may be unimportant, possibly saving money for the user.

Does the signal contain discontinuities? If so, the choice of architecture is usually limited to "single-shot" type A/D converters (such as SAR, subranging, flash) since A/D converters which are continuous (delta-sigma, integrating, VFC, dual slope) tend to integrate signal discontinuities, giving false outputs.

What is the characteristic source impedance of the signal? Most A/D converters require a low dynamic source impedance, which is discussed in detail in the "Drive Requirements" section of this application bulletin. There may be some advantages in matching the A/D converter's input impedance to the source impedance to reduce distortion problems caused by reflections.

If the input signal is noisy, it may be best to consider using an integrating type of A/D, since the integration acts to reduce noise. However, most integrating converters have fairly slow sample rates and analog input bandwidth. If the input signal is both fast and noisy, the user has some options, such as driving the A/D with an integrating amplifier, using a bandpass filter to reduce input noise, using a high speed A/D and averaging the results, or digitally filtering the results in DSP. Generally speaking, for slow input signals, using a type of integrating converter is a very cost-effective solution.

The signal amplitude should be closely matched to the analog input range of the A/D. This is done to maximize the dynamic range of the converter. For example, if a 12-bit converter with a 20-V input range is selected, the value of one LSB is 4.88 mV. It would be ineffective to use only a small part of that range, for example, if the input signal was 2 V. A better solution would be to select a converter with a more optimal input range, or to insert a gain block in front of the A/D (keep in mind new errors which the gain block will introduce). Many high speed converters, due to process voltage breakdown limitations, have small input ranges. If the signal bandwidth is small and a high degree of accuracy is needed, it may be advantageous to consider using a lower speed A/D with a larger input range.

1.6   *Environmental Conditions*

Environmental conditions for the digitizing system are often predetermined. Since it is generally not possible to compromise those conditions, it is important to select a converter which will be guaranteed to operate to required accuracy levels within the system environment. In addition to environmental conditions, the system may have limited power supplies, in terms of voltage and current. For low frequency systems, specifications of interest include offset drift, gain drift, and linearity drift. Offset drift is often specified as bipolar zero error drift in the case of converters with bipolar input ranges. For dynamic systems, if the system will have a wide temperature variation under operation, the A/D must have its dynamic specifications such as SFDR and SNR guaranteed over the required temperature range.

Table 3. Comparison of Errors Over Temperature Between Autocalibrating and Non-Calibrating Devices[1]

PARAMETER	ADS7803BP	ADS7804PB
Temperature Range	–40°C to 85°C	–40°C to 85°C
Gain Error	0.25 LSB	10 LSB
Gain Drift	0.2ppm Typical	5ppm Typical
Offset Error	0.25 LSB	2 LSB
Offset Drift	0.2ppm Typical	2ppm Typical
DNL Error	0.5 LSB	0.45 LSB

[1]   For ADS7803BP, errors shown are after a calibration cycle.

One possible solution to obtaining good performance over a wide temperature range would be to select an A/D with an *autocalibrating* architecture. These converters contain internal calibration circuitry which allows for very small offset, gain and linearity errors. However, not all autocalibrating converters guarantee performance over the full temperature range without additional calibration cycles. Also, when using this type of converter, the user must allow for a certain period to allow calibration to take place. A strong

argument can be made for using a standard converter with an external offset and gain adjustment, if those adjustments are stable over long periods of time. Table 3 compares a typical 12- bit autocalibrating A/D, ADS7803, with a 12-bit non-autocalibrating device, ADS7804. Although the initial errors for the ADS7804 may appear large, it should be noted it is very easy to null these errors out, and life tests have shown the errors to be very stable over long periods.

Another point to consider when selecting a converter for a specific temperature range is whether the temperature is specified as *ambient* (T_A), or *case* (T_C). Most low-power CMOS converters are specified and tested at ambient temperatures, while faster bipolar converters are specified with case temperatures. For the converters which are specified with case temperatures, it may be very helpful to use a heat sink to provide improved temperature performance, since the case specification negates any heat dissipation benefits gained through the use of a heat sink. Finally, it should be noted that older converters typically are specified only at room temperature, with drift coefficients given only for gain and offset parameters. Most modern converters have a single specification-full temperature range, which provides the user with an excellent worst-case specification.

Another area of concern related to environmental conditions is package type. Hermetic packaging, whether in a metal bucket or CERDIP package, generally provide the most resistance to hostile environments where high temperatures and humidity pose a threat to the long term reliability of the silicon circuits. However, with the advent of hermetic passivation, many plastic packages can offer very good moisture endurance. It may well be worth the time to consult a detailed reliability report for a plastic packaged device, as the cost savings can be substantial. It should not be assumed the hermetic package is always more reliable.

1.7 Sampling Mechanism

Track and hold circuits are used to enhance the dynamic performance of A/D converters, where the input signal is changing too rapidly for the converter to maintain good linearity. Track and hold circuits are often referred to as sample and hold. The two circuits are identical when the hold command is direct-coupled. The term "sample and hold" is used when the hold command is ac coupled. For all practical purposes, the two terms are interchangeable. For the discussion of A/D converters, the function can be thought of as a sample mechanism in front of the A/D converter.

A track and hold circuit is used to reduce the aperture time of the sample system (sampling mechanism in combination with the A/D converter). Converters in the industrial and high speed ranges (12-bits, >10 kSPS) usually are built with an architecture which requires the input held constant during a conversion cycle. Architectures employing an iterative conversion include successive approximation (SAR) and subranging. Parallel converters such as flashes can also benefit from sampling mechanisms, since the time delays of all the comparators are not identical. The tolerance of the iterative architecture to changes in input levels is very limited. For example, a 12-bit 1-MSPS A/D converter has a theoretical Nyquist rate of 500 kHz. However, without a track and hold circuit, an accuracy level of one-half LSB limits the input frequency to only 38.9Hz!

An excellent and detailed explanation of track and hold circuits and specifications can be found in Burr-Brown Application Bulletin AB-027, *High Speed Data Conversion*. The remainder of this discussion will focus on so- called "sampling A/D converters". CMOS SAR converters are said to be inherently sampling. This is a function of the architecture, which traps charge from the input signal on a capacitor array. Details of this architecture can be found in Burr-Brown Application Bulletin AB-178, *CDAC Architecture Plus Resistor Divider Gives ADC574 Pinout With Sampling, Low Power, New Input Ranges*. The technique seems straightforward, but unfortunately, it is not bulletproof. A quick glance at the data sheets of many of these converters reveals distortion problems at high input frequencies. This distortion is not due to inherent nonlinearities in the A/D converter. The problem lies with nonlinearities in the FET switches in the capacitor array, primarily due to problems in matching R_{ON}. These problems manifest themselves at higher input frequencies, as dV/dt across the switches increase. This distortion is not due to the inherent nonlinearities of the A/D converter, since the track and hold circuit guarantees the converter will always see a DC signal (assuming there is a reasonable droop rate associated with the track and hold circuit). Early recognition of this phenomenon and some clever design techniques has allowed Burr-Brown to provide sampling CMOS A/D converters with very good Nyquist rate performance. These parts are called the "ADS78xx Family", starting with part number ADS7804. Table 4 shows a comparison of distortion of several generations of sampling A/D systems. For a more detailed explanation of the sampling distortion phenomena, refer to Burr-Brown's *Application Seminar Fall 1994 Handbook*, pages 5.71 through 5.80.

Table 4. Examples of Sampling Distortion and SNR vs Input Frequency

MODEL	SFDR			SINAD		
	1 kHz	10 kHz	45 kHz	1 kHz	10 kHz	45 kHz
ADC774 / SHC5320	92	82	77	73	72	70.5
ADS774	91	80	73	72	71	68
ADC1674	94	89	88	71	71	71
ADS7804	94	93	93	73	73	73

AD1674 is a monolithic BiCMOS device manufactured by Analog Devices which is included in this table to demonstrate another way of implementing a sampling A/D converter. In that architecture, the track and hold circuit has been designed with bipolar devices, yielding a "true" track and hold with good performance. The bottom line when selecting a sampling A/D is to be certain the converter will meet the distortion goals at the system's input frequencies.

2 Secondary Considerations

2.1 Multiple Channel Systems

The selection process for an A/D converter begins with the elements of no compromise, where the systems needs must be met. Now to be investigated are the secondary considerations, where the designer has the ability to combine elements of both system design and A/D selection. The first point to consider is the cost and complexity tradeoff of multiplexing. If the system has multiple channels, no immediate assumption should be made that a multiplexed system is the best approach. In a traditional multiplexed system, many new errors can be introduced. A simple diagram of multiplexed system is shown in Figure 9.
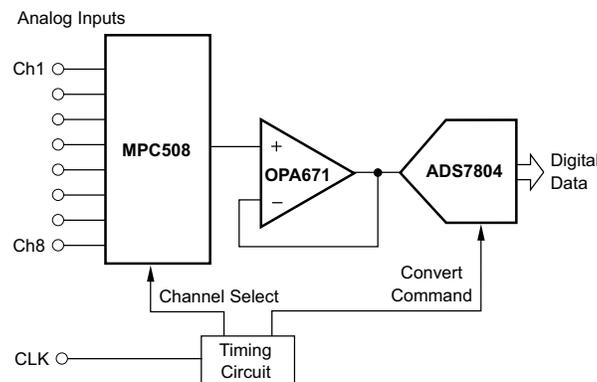

Figure 9. Traditional Analog Multiplexing System

When designing this type of system, care must be taken to reduce errors caused by mismatches in the different channels. For example, to minimize errors caused by Δ R ON of the multiplexer, components must be selected with proper impedances. The input to the multiplexer needs to be driven with a low source impedance, and the outputs should drive a very high load impedance. Additionally, the bias current of the load can interact with the R ON of the multiplexer causing voltage offset errors. If the error budget in the system is limited, it may be more cost effective to use multiple converters. In 1995, in OEM quantities, the price of 12-bit 100-kHz A/D converters is under $10, while 16-bit 100-kHz A/D converters are priced under $30.

2.2 Reference

All A/D converters require a voltage reference. The reference determines the full scale range of the A/D. The voltage reference can either be internal or external. In some cases, the manufacturer allows the user to access the reference, either to drive external circuitry or to input a user-defined reference. In general, an internal reference is a valuable function for the user. In addition to a cost saving, there will be less PC board "real estate" for such a converter. In the case of multiple channel systems, it may be beneficial to use an external reference, since the drift of the reference dominates the gain drift of the A/D converter. However, not all references are created equally. Particularly, for some CMOS SAR converters, the requirements for the reference (or at least the reference value where the part is specified) may be an unusual value, not available in an off-the-shelf reference. In these cases, the user will need to implement a voltage divider, which takes up board space, allows for additional noise and could introduce new drift problems. There are also some components which use different reference values to specify AC and DC performance. It is recommended for the reference to be some common value, which will hold down cost and complexity.

2.3 Drive Requirements

Several points must be considered when driving an A/D converter, impedance matching, charge injection, noise reduction and accuracy. For a bipolar input A/D without a track and hold circuit, the input to the A/D is a summing junction of a comparator which is connected to an internal digital-to-analog converter. This node is essentially a dynamic impedance that is changing throughout the conversion. The drive amplifier must have low enough output impedance at fairly high frequencies to not introduce errors.

For a CMOS sampling A/D converter, the input is basically driving a switch. As the switch changes from hold mode to track mode, there is some amount of charge injection. The drive amplifier must have sufficient output current and fast settling time to drive the charge injection pulse. Figure 10 models two different CMOS input structures, showing both the "traditional" and the type used for Burr-Brown's ADS7804. Note the resistor divider input on the ADS7804. The divider in combination with a more efficiently designed switch greatly reduces charge injection. A typical value of the current spike on the traditional structure is 20 mA, where the ADS7804 structure is approximately 250 µA. This will lessen the requirements (and the cost) for the drive amplifier. The input structure of ADS7804 is typical of the "ADS78xx Family" with different resistor values providing different input ranges.
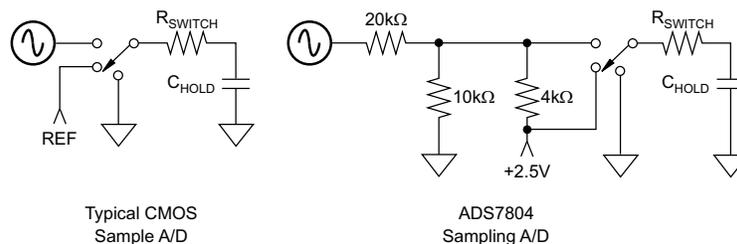

Figure 10. Comparison of Input Structures

In order not to introduce excess noise into the system, the drive amplifier and all of its noise sources should be considered. At a minimum, the drive amplifier must have better SNR than the theoretical limit of the A/D converter. Fortunately, virtually all modern op amps have noise performance much better than 12-bits, and finding op amps with good 16-bit noise performance is not a difficult task. However, it is important to keep in mind the noise power of the two sources is additive. To determine the noise power, convert the SNR values from dB to voltage (divide by 20 and calculate 10 x). Then calculate the root-sum-square and return the values to dB. This calculation will show that the SNR of the op amp will cause degradation in the SNR of the converter. An op amp with a 3-dB SNR improvement over the A/D converter will reduce the overall SNR by 1.8 dB, while an op amp with 12 dB improved SNR will cause an overall drop of 0.27 dB.

The amplifier can also cause gain accuracy problems if it does not have adequate open-loop gain. There must be a substantial amount of gain over the input signal bandwidth. A simple example of the need for a wide-bandwidth drive amp can be seen in Figure 11, which plots the ratio of pole frequency to input frequency needed for maintaining 0.25-LSB accuracy. This particular plot applies only to a simple, single-pole system. By inspection, bandwidth requirements increase substantially for high-resolution A/D converters. Wide bandwidth op amps improve accuracy by maintaining a low output impedance over the entire input signal bandwidth.
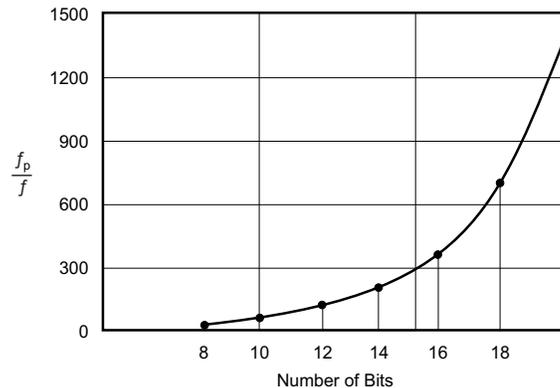

Figure 11. Ratio of First Pole to Input Frequency Required to Maintain 0.25 LSB Accuracy

2.4 Interface and Output Formats

Another secondary consideration which merits advance planning is the digital interface. There are control lines for the A/D converter as well as the digital output information which have many different possible configurations. The primary signals which are used to control sampling A/D converters include:

- The **Convert Command**, often referred to as *Read/Convert*, is used to initiate a conversion. Modern converters are internally clocked, so the converter only requires a digital transition to begin converting.
- **Chip Enable** is a control line, used on ADC574 type converters, which must be set to an active state to allow for a conversion. In the disable mode, all commands to convert are ignored.
- **Chip Select** is the inverse of Chip Enable. These two somewhat redundant lines are not used in combination on next generation converters, such as ADS78xx. A single line, such as Chip Select, is internally OR'd with the convert command.
- **Byte Select** is used to control how the data comes out of the converter. For the '574 series, this pin is referred to as 12/8 . This line allows for the '574 to be used as either a 12-bit or an 8-bit converter. For the ADS78xx Family, the Byte Select pin on the parallel output versions controls which data bits are on which pins. In addition to these standard control lines, converters with serial output formats require a data clock.

The digital data from the A/D converter to the controller include the following:

- The **Data Output** is intuitive; however, with some devices, the output coding can be programmed into straight binary, two's complement binary, and others. A detailed explanation of coding formats can be found in Burr-Brown's Application Bulletin AB-175, *Coding Schemes Used with Data Converters*.
- The **Status** (or **Busy**) line indicates to the controller when a conversion is being performed. When the Status line changes states, data from the previous conversion becomes valid.

Once the designer has a good understanding of the types of signals which will be necessary to complete the digital interface, the process of selection can again be reduced to a checklist:

1. *What is the logic format (TTL, ECL, CMOS)?* Some converters are specified for multiple compatibility. However, the designer is advised to consult the logic level specifications to ensure true compatibility. Also beware of how the converter may interpret undefined states.

2. *What is the width of the data bus?* The type of controller used may indicate an 8-bit bus or a 16-bit bus. The presence of a 16-bit controller does not indicate the use of a 16-bit converter. The accuracy of the converter is only tied to the system accuracy requirement. If a 16-bit bus is needed with a 12-bit converter, consider how to tie up the unused inputs to avoid introducing errors.

3. *Is there a need for isolation?* If the analog front end is connected to an environment with large common mode voltages or transients, it is usually advisable to isolate the digital side from possible damage. Analog isolation devices are linear to 12-bits, but if 16-bit accuracy is the goal, it may be best to consider the use of isolated digital couplers, either capacitive or optical. It is usually much less expensive to isolate a single channel of data, which may preclude the answer to the next question.

4. *Should the output data be serial, parallel, or in bytes?* To a large extent, the answer to this question was determined by questions 2 and 3. The output data format should be compatible with the controller bus, and if isolation is needed, the serial data format usually presents the most cost effective solution. Another advantage for the serial converter is reduced PC board space. It is also possible to multiplex the control signals where space is at an absolute premium.

2.5 Conversion Timing

One element often overlooked in the selection process is the timing of the conversion system. It is often assumed that by simply applying a convert command, data can be valid immediately following the conversion. However, many converters operate with pipelined timing. This type of timing requires a second conversion in order to have valid output data. This type of converter would not be conducive to "single shot" conversions. The '574 series allows for valid data after the completion of a conversion, provided four specific logic conditions are met simultaneously. It is there- fore important to provide synchronous logic if the converter is to be operated in a continuous mode.

For pipelined timing, a second conversion must be initiated to have valid data. Burr-Brown's ADC603 and ADC614 can be configured to have valid data with preset pipeline delays, either one or two conversions later. If the digitizing system will have non-continuous conversions, the selected A/D converter must not have pipelined data outputs, or some external circuitry must be designed to simulate the subsequent conversions required to obtain valid data. Figure 12 illustrates timing for a serial pipelined converter. Figure 13 illustrates timing for a non-pipelined condition, such as ADS7800. Figure 14 illustrates pipelined timing for a parallel converter, ADC614.
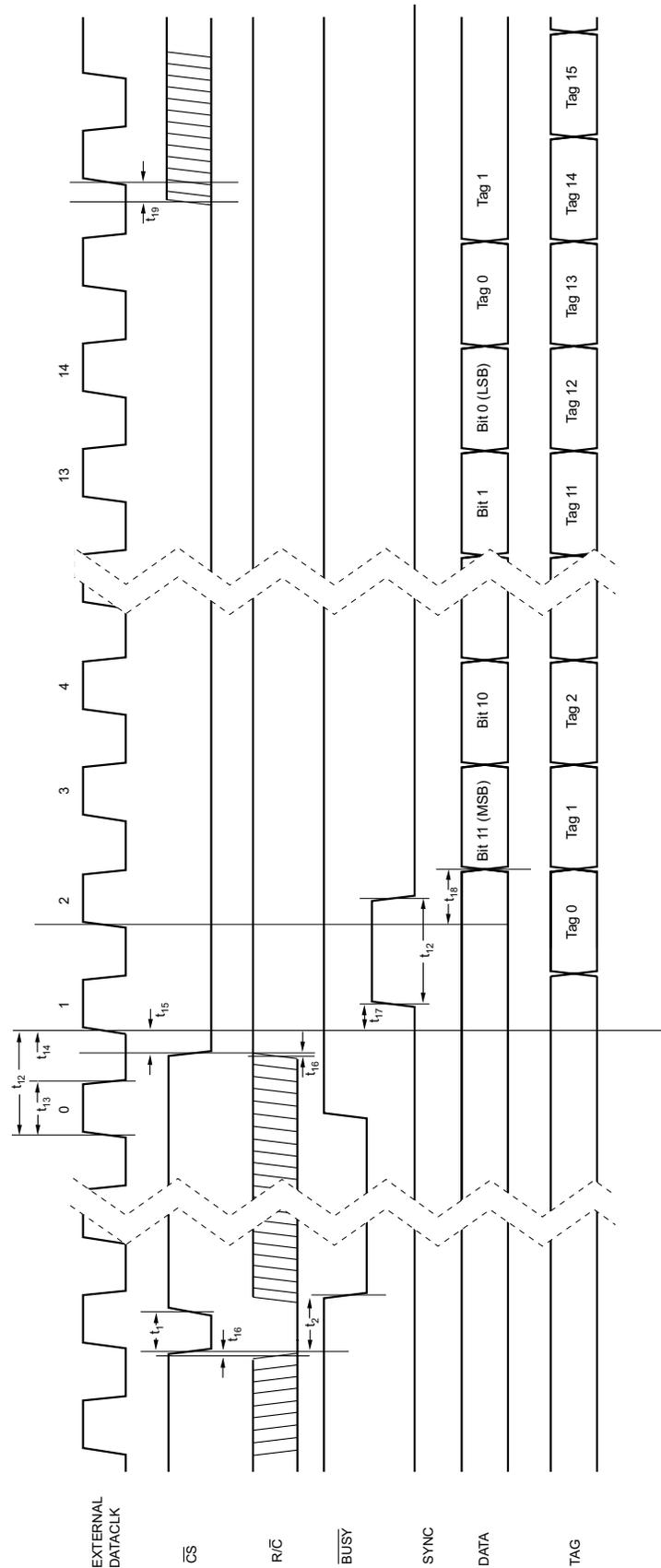
Figure 12. Conversion and Read Timing with External Clock (EXT/INT Tied HIGH), Read After Conversion.
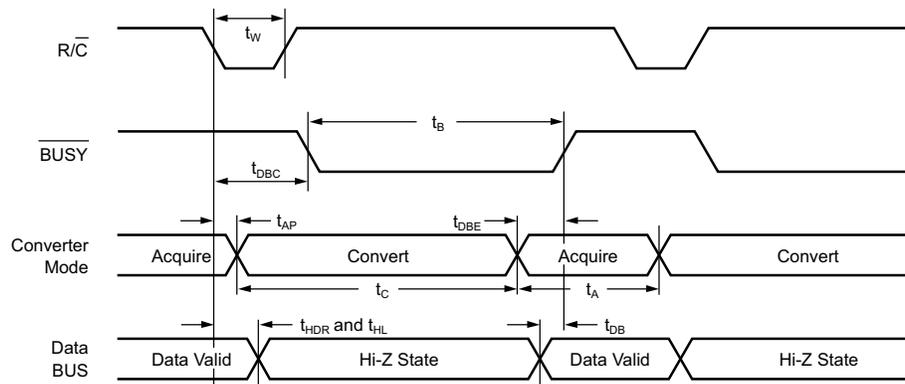
**Figure 13. Convert Mode: R/C Pulse LOW — Outputs Enabled After Conversion**
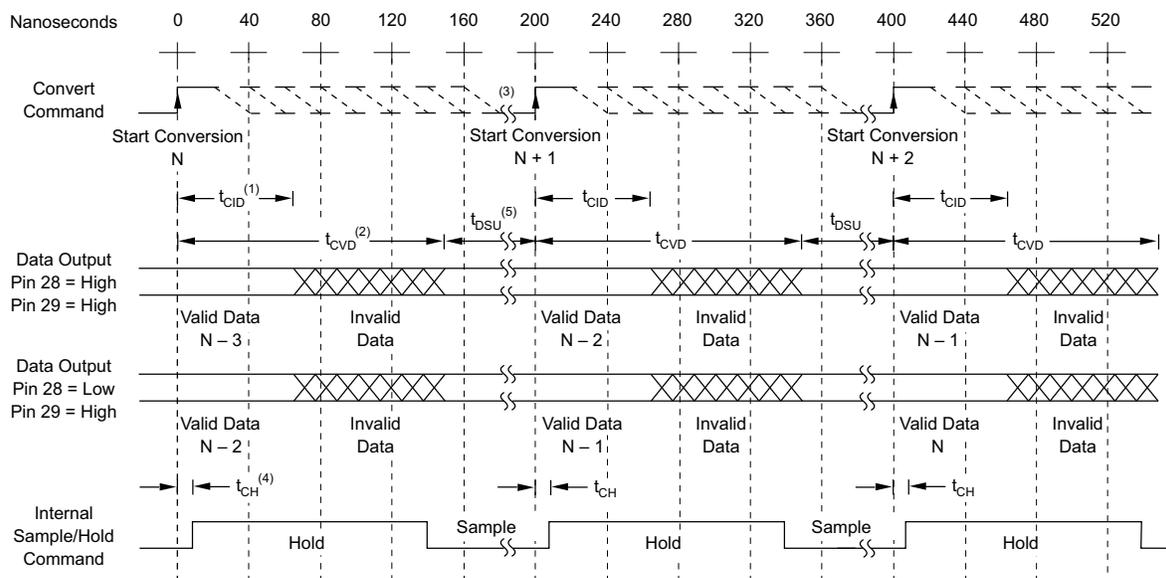
Figure 14. Basic Conversion Timing

2.6 *Summary*

This bulletin has examined the process of selecting an A/D converter for a digitizing system. A checklist of both primary and secondary factors was presented, with detailed explanations of the parameters. Other application bulletins will provide more detail and examples of those selection factors. Through use of the checklist, the designer should be able to narrow down the choices in a fast and logical manner.

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