Application Note

Input Common-Mode Tolerance and High CMRR Modes for TLV320ADCx120 and PCMx120-Q1 Devices

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ABSTRACT

The TLV320ADCx120 (TLV320ADC3120, TLV320ADC5120, and TLV320ADC6120) and PCMx120-Q1 (PCM3120-Q1, PCM5120-Q1, and PCM6120-Q1) family of devices are dual-channel, high-performance, analog-to-digital converters for audio applications. This family of devices supports highly configurable inputs to allow the device to achieve high performance even in the presence of large common-mode signals.

This application note describes the performance of the TLV320ADCx120 and PCMx120-Q1 devices when operating in high common-mode rejection ratio (CMRR) modes for applications with high common-mode requirements.

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Trademarks

1 Introduction

Common-mode in a differential amplifier is formally defined as the average voltage of the two input pins. Difference amplifiers are designed to amplify the differential signal and reject signals common to both input pins, such as a DC bias, noise picked up in the system, or a shifting reference. How well the amplifier does this is called the common-mode rejection ratio, or CMRR. CMRR is formally expressed as the ratio of the amplifier's differential gain to common-mode gain. In practice though, CMRR is typically measured by changing the input common-mode and observing the change in output. This measured change can be referred to the input and considered an offset voltage at the amplifier's inputs.

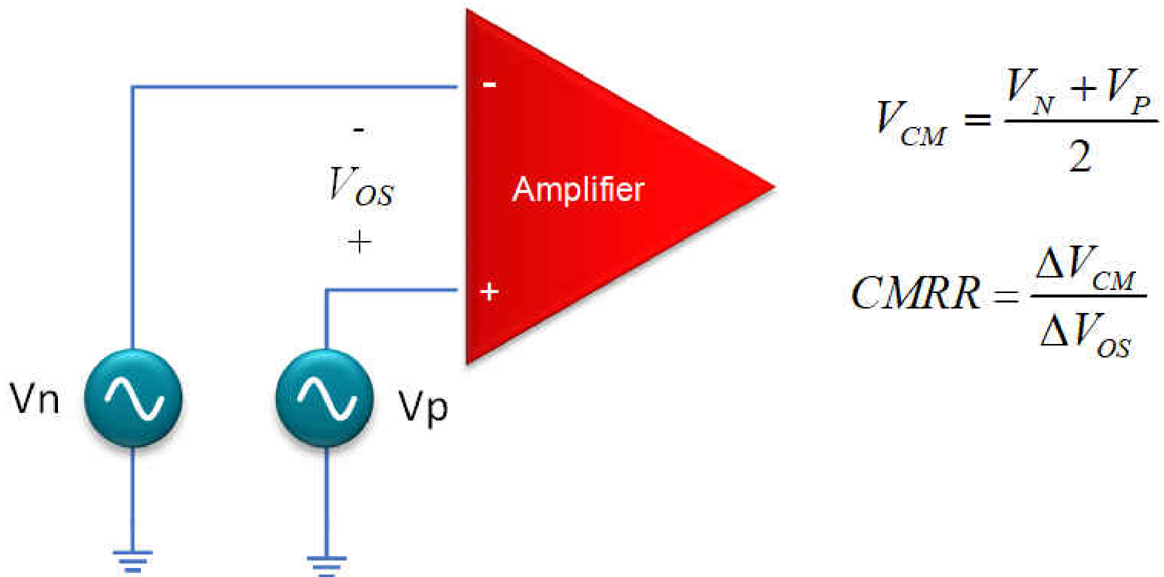

Figure 1-1. Common-Mode Definition

The TLV320ADCx120 and PCMx120-Q1 family of devices has an input architecture that allows it to support a wide range of input configurations while maintaining high performance. For optimal performance the common-mode variation at the device input should be limited to less than 100 mVpp for AC coupled settings. For applications that cannot avoid large common-mode fluctuations, the TLV320ADCx120 and PCMx120-Q1 family offers multiple modes to configure the device for higher common-mode tolerance as shown in Table 2-1

Increasing the common-mode tolerance of the input does require a performance trade-off. This application note details the typical performance for each of the input modes.

2 Common-Mode Tolerance Modes

The TLV320ADCx120 and PCMx120-Q1 family supports three different modes for common-mode tolerance that should be selected based on the maximum expected common-mode variation. Since wider common-mode tolerance does degrade other performance parameters, it is recommended to select the lowest tolerance mode possible.

Table 2-1. Common-Mode Tolerance Mode Selection for Record Channel

P0_R58_D[7:6] : CH1_INP_CM_TOL_CFG[1:0]	CHANNEL 1 INPUT COMMON-MODE TOLERANCE
00 (default)	Channel 1 input common-mode tolerance of: AC-coupled input = 100 mV_{PP}, DC-coupled input = 2.82 V_{PP}.
01	Channel 1 input common-mode tolerance of: AC/DC-coupled input = 1 V_{PP}.
10 (high CMRR mode)	Channel 1 input common-mode tolerance of: AC/DC-coupled input = 0-AVDD (supported only with an input impedance of 10 kΩ and 20 kΩ). For input impedance of 2.5 kΩ, the input common-mode tolerance is 0.4 V to 2.6 V.
11	Reserved (do not use this setting)

It is important to keep in mind that in all modes, the full-scale range of the device is still 2-Vrms. This is especially important for large common-mode signals as they will limit the effective input range. Mode 2, for example, can support a common-mode range of 0-V to AVDD, but there would be no room left for a differential signal to be applied to the input pins at either of these extremes. The PGA gain can be used to amplify the differential signal as needed but the attenuated common-mode signal will be amplified as well.

3 Common-Mode Rejection Performance

Each common-mode tolerance mode will achieve good common-mode rejection up to the limits of that mode. Typical CMRR for each variant in mode 0 is 60dB and typically improves by a few dB in modes 1 and 2 for an equivalent signal amplitude. The higher performance TLV320ADC6120 and PCM6120-Q1 can achieve closer to 80dB CMRR typical in mode 2 and is a good choice for systems that want the best performance possible in applications that require high common-mode tolerance.

Figure 3-1 demonstrates the resulting output level of TLV320ADC5120 and PCM5120-Q1 with a 1kHz common-mode input across the full scale input range of the device in each of the tolerance modes. CMRR would be the difference between the input level (converted to dBFS where full scale is 2-Vrms) and the measured output level shown in the curve.

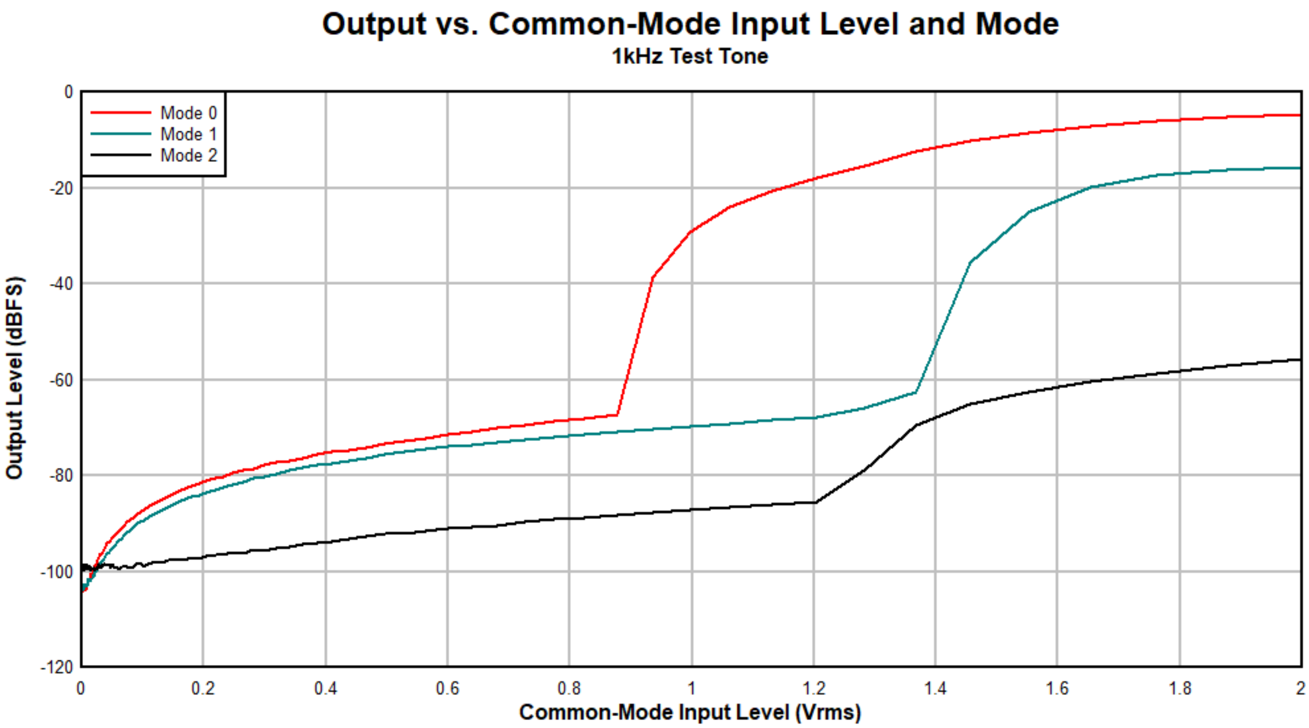

Figure 3-1. Output vs. Common-Mode Input Level and Mode

4 Input Common-Mode Distortion

The following plots demonstrate the CMRR and THD+N performance with different input levels in each of the tolerance modes. These curves are measured on an ADC5120EVM-PDK board configured for AC coupled inputs using an AP2700 and a precision function generator. A 1-kHz, -60-dBFS differential input tone is applied from the Audio Precision and a 750-Hz common-mode tone is applied to the reference node of the AP2700. The -60-dBFS differential tone is not large enough to produce its own distortion products. The 750-Hz common-mode is used to easily differentiate any harmonics resulting from the common-mode variation.

When referring to the figures it is helpful to keep in mind the relationship between output dBFS and the input voltage. The following is an example calculation:

2-Vrms = 2.8-Vpp

100-mVpp = 0.05-Vp

100-mVpp in dBFS = 20*log(0.05/2.8) = -35dBFS

Figure 4-1 shows the output spectrum in mode 0 with a 100-mVpp (-35-dBFS) common-mode tone applied to the input. From this plot we can observe that no significant distortion occurs and the 750-Hz tone is reduced by around 55dB (-35dB - (-90dB) = 55dB). The measured THD+N level for this test was -93-dBFS.

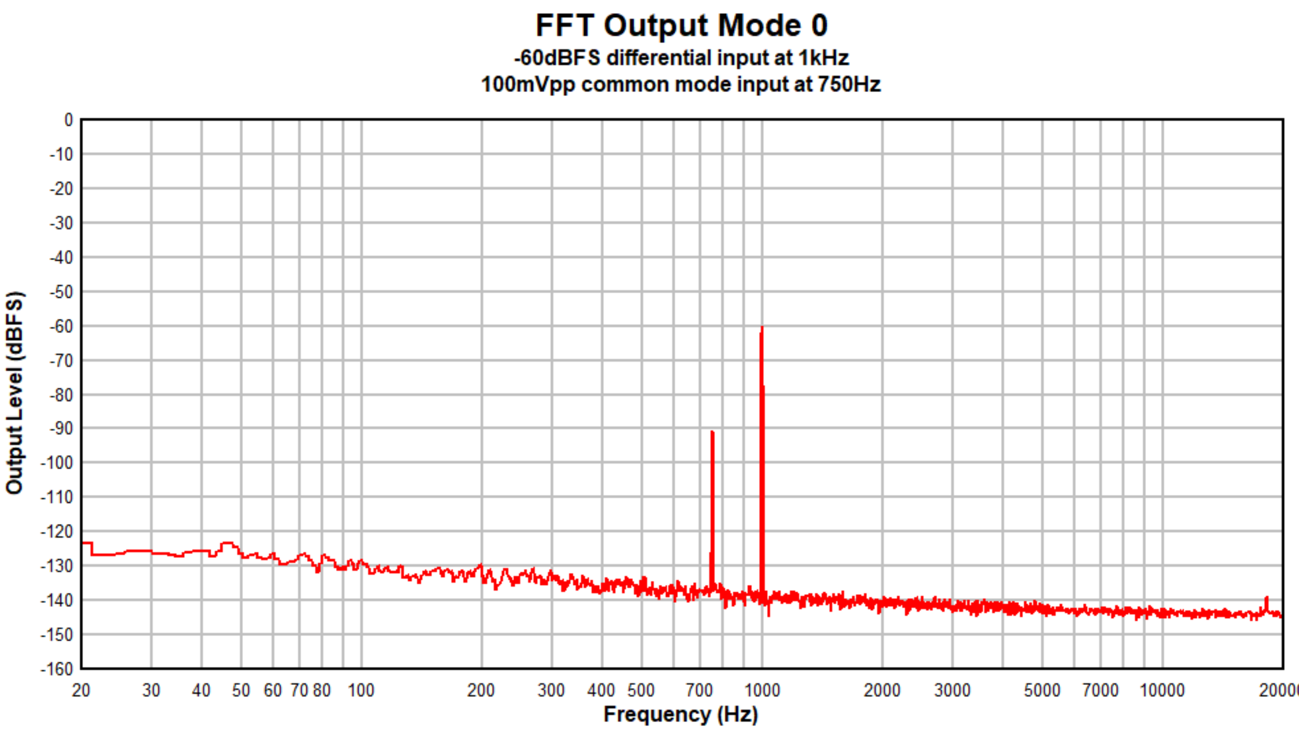

Figure 4-1. Mode 0 Output FFT with 100-mVpp Common-Mode

Figure 4-2 shows the output spectrum in mode 0 with the input common-mode amplitude increased to 1Vpp (-15-dBFS). Note that this is well outside the maximum common-mode tolerance of mode 0 and significant distortion can be seen as expected. The primary 750-Hz tone is at approximately -70dB, so the CMRR is still around 55dB (-15 - (-70) = 55dB), but the THD+N level has degraded to approximately -73-dBFS.

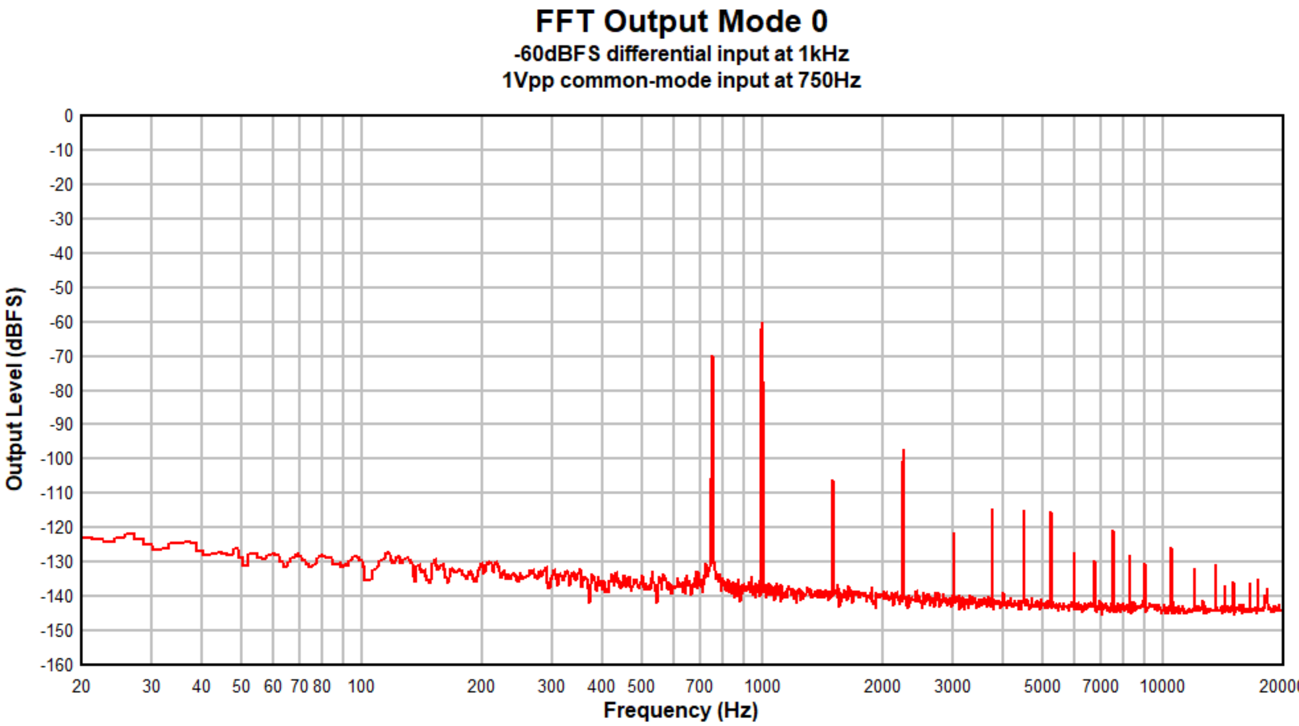

Figure 4-2. Mode 0 Output FFT with 1-Vpp Common-Mode

Figure 4-3 shows the same 1-Vpp common-mode signal applied to the input in mode 1. Mode 1 extends the supported common-mode range, slightly improves the common-mode rejection of the fundamental 750Hz tone, and significantly reduces the distortion introduced from the large common-mode signal.

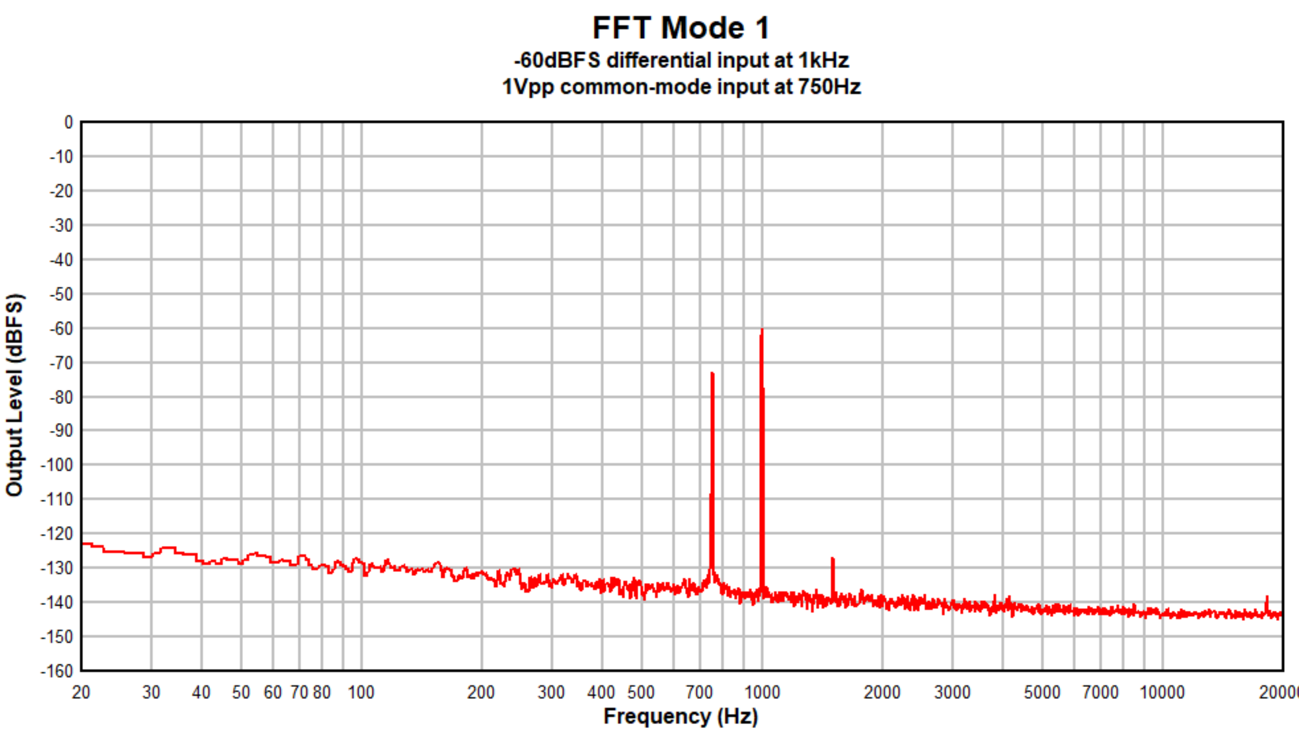

Figure 4-3. Mode 1 Output FFT with 1-Vpp Common-Mode

Figure 4-4 again shows the same 1-Vpp common-mode signal applied to the input in mode 2. Mode 2 further extends the common-mode range, improves the common-mode rejection, and eliminates the distortion produced from the large input common-mode tone.

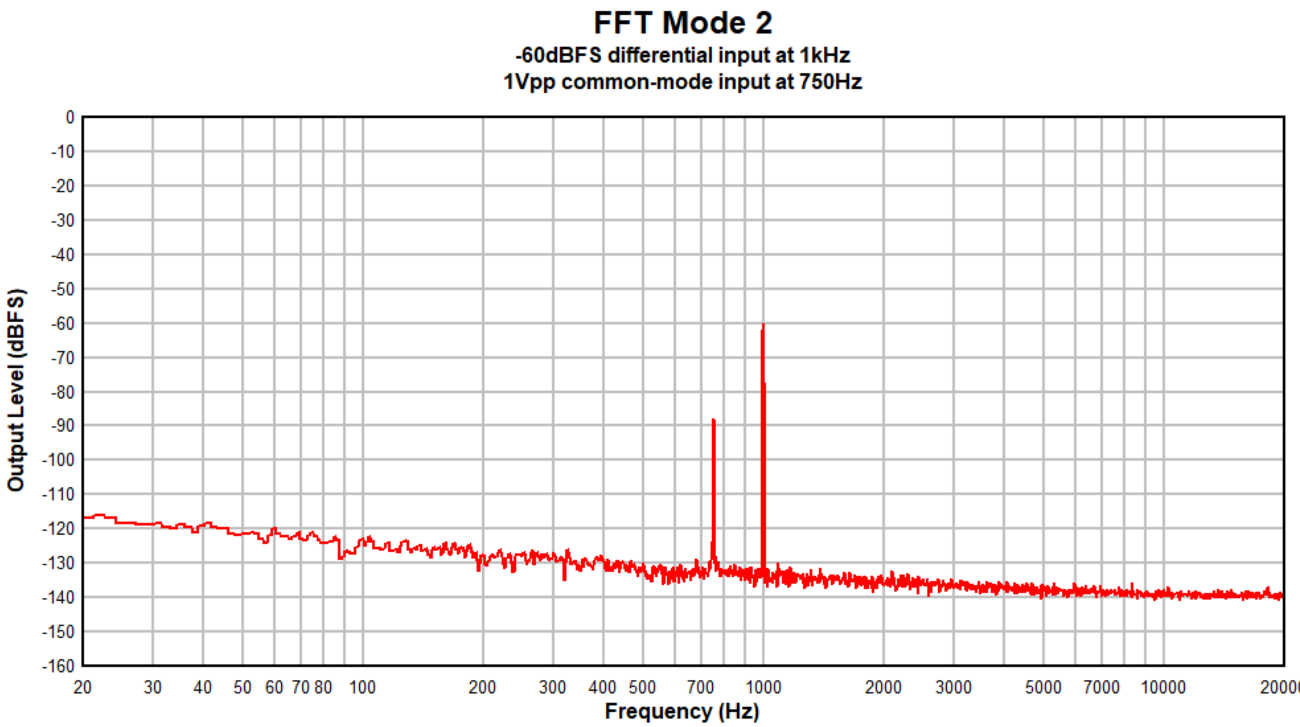

Figure 4-4. Mode 2 Output FFT with 1-Vpp Common-Mode

5 Performance for TLV320ADC3120 and PCM3120-Q1

Each input setting will have an impact on performance. Table 5-1 shows the typical performance of the TLV320ADC3120 and PCM3120-Q1 with differential inputs in each of the modes. For the best noise and distortion performance, it is recommended to use CMRR mode 0, AC coupled input, and 10kOhm input impedance.

Table 5-1. Performance for TLV320ADC3120 and PCM3120-Q1

CMRR mode	Input Coupling	Input Impedance (Ohms)	SNR (dB)	THD+N (dB)
0	AC	10k	107	-95
		20k	106	-94
	DC	10k	106	-94
		20k	105	-94
1	AC	10k	107	-94
		20k	106	-94
	DC	10k	106	-94
		20k	105	-94
2	AC	10k	103	-93
		20k	99	-92
	DC	10k	103	-93
		20k	99	-92

6 Performance for TLV320ADC5120 and PCM5120-Q1

Each input setting will have an impact on performance. Table 6-1 shows the typical performance of the TLV320ADC5120 and PCM5120-Q1 with differential inputs in each of the modes. For the best noise and distortion performance, it is recommended to use CMRR mode 0, AC coupled input, and 2.5kOhm input impedance with DRE enabled.

Table 6-1. Performance for TLV320ADC5120 and PCM5120-Q1

CMRR mode	Input Coupling	DRE	Input Impedance (Ohms)	SNR (dB)	THD+N (dB)
0	AC	Enabled	2.5k	120	-96
			10k	117	-95
			20k	114	-95
		Disabled	2.5k	109	-96
			10k	108	-95
			20k	107	-95
	DC	Enabled	2.5k	Not Supported	Not Supported
			10k	110	-95
			20k	108	-95
		Disabled	2.5k	Not Supported	Not Supported
			10k	106	-95
			20k	105	-95
1	AC	Enabled	2.5k	117	-96
			10k	114	-95
			20k	112	-95
		Disabled	2.5k	108	-96
			10k	107	-95
			20k	106	-95
	DC	Enabled	2.5k	Not Supported	Not Supported
			10k	111	-96
			20k	108	-96
		Disabled	2.5k	Not Supported	Not Supported
			10k	106	-96
			20k	105	-96
2	AC	Enabled	2.5k	114	-96
			10k	106	-95
			20k	100	-93
		Disabled	2.5k	107	-96
			10k	103	-95
			20k	99	-93
	DC	Enabled	2.5k	Not Supported	Not Supported
			10k	105	-95
			20k	100	-93
		Disabled	2.5k	Not Supported	Not Supported
			10k	103	-95
			20k	99	-93

7 Performance for TLV320ADC6120 and PCM6120-Q1

Each input setting will have an impact on performance. Table 7-1 shows the typical performance of the TLV320ADC6120 and PCM6120-Q1 with differential inputs in each of the modes. For the best noise and distortion performance, it is recommended to use CMRR mode 0, AC coupled input, and 2.5-kOhm input impedance with DRE enabled.

Table 7-1. Performance for TLV320ADC6120 and PCM6120-Q1

CMRR mode	Input Coupling	DRE	Input Impedance (Ohms)	SNR (dB)	THD+N (dB)
0	AC	Enabled	2.5k	122	-96
			10k	118	-95
			20k	115	-95
		Disabled	2.5k	112	-96
			10k	110	-95
			20k	109	-95
	DC	Enabled	2.5k	Not Supported	Not Supported
			10k	111	-96
			20k	109	-95
		Disabled	2.5k	Not Supported	Not Supported
			10k	108	-96
			20k	106	-95
1	AC	Enabled	2.5k	120	-96
			10k	116	-95
			20k	113	-95
		Disabled	2.5k	111	-96
			10k	110	-95
			20k	109	-95
	DC	Enabled	2.5k	Not Supported	Not Supported
			10k	112	-96
			20k	109	-96
		Disabled	2.5k	Not Supported	Not Supported
			10k	108	-96
			20k	107	-96
2	AC	Enabled	2.5k	117	-96
			10k	108	-95
			20k	103	-94
		Disabled	2.5k	111	-96
			10k	106	-95
			20k	102	-94
	DC	Enabled	2.5k	Not Supported	Not Supported
			10k	108	-95
			20k	102	-94
		Disabled	2.5k	Not Supported	Not Supported
			10k	106	-95
			20k	102	-94

TLV320ADC6120 and PCM6120-Q1 arethe highest perfomance devices in the TLV320ADCx120 and PCMx120-Q1 family. It is the best choice for applications that require high performance and high common-mode tolerance.

8 Summary

The TLV320ADCx120 and PCMx120-Q1 family of devices offers very flexible input configuration making it suitable for a wide range of applications. Multiple common-mode tolerance modes are provided to allow the system to perform well even in the presence of large amounts of common-mode noise. Since the performance of the devices does change with the input configuration, it is recommended to use the lowest common-mode setting possible that still satisfies the tolerance required by the system. For best performance, AC coupling is recommended with DRE enabled and the lowest input impedance setting that can be used.

9 Related Documentation

For related documentation see the following:

- PCM3120-Q1
  - Texas Instruments, *PCM3120-Q1 2-Channel, 768-kHz, Burr-Brown Audio ADC data sheet*
- PCM5120-Q1
  - Texas Instruments, *PCM5120-Q1 2-Channel, 768-kHz, Burr-Brown Audio ADC data sheet*
- PCM6120-Q1
  - Texas Instruments, *PCM6120-Q1 2-Channel, 768-kHz, Burr-Brown Audio ADC data sheet*
- TLV320ADC6120
  - Texas Instruments, *TLV320ADC6120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet*.
  - Texas Instruments, *TLV320ADC6120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module*.
- TLV320ADC5120
  - Texas Instruments, *TLV320ADC5120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet*.
  - Texas Instruments, *TLV320ADC5120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module*.
- TLV320ADC3120
  - Texas Instruments, *TLV320ADC3120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet*.
  - Texas Instruments, *TLV320ADC3120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module*.
- Texas Instruments, *ADCx120EVM-PDK User's Guide*.
- Texas Instruments, *PurePath™ Console*.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2021) to Revision A (April 2022) **Page**

- Added PCMx120-Q1 devices.. 1

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