

ADC in Automated Test Equipment Applications

The [ADS9813](#) ADC is an eight-channel, 2MSPS per channel, simultaneous sampling data acquisition (DAQ) system based on an 18-bit successive-approximation register (SAR) architecture. The high channel density of the ADS9813 enables more PMU units to run in parallel, reducing test time and cost. The ability of the ADS9813 to simultaneously sample the input signal on all analog input channels is especially useful in measurements that are sensitive to phase delay between input channels caused by sequential sampling.

The integrated complete analog front-end of the ADS9813 device features an overvoltage input clamp, 1MΩ input impedance, independently programmable gain amplifier (PGA), programmable low-pass filter (LPF), and an ADC input driver. The ADC also has a low-drift precision reference, and an input buffer is integrated for external references. These features reduce the size of the signal chain in the ATE application and the lack of additional external components reduces the error contribution between the PMU output and ADC input.

Design Example

When selecting an ADC for an ATE application, determine the following parameters:

Table 1. Design Target Parameters

Parameter	Application Target	ADS9813 ADC
Maximum % Error (example value from AC/DC voltmeter)	0.005%	0.0016%
Settling Time (99.99% of FS) (example value from LCD panel test)	3.0μs	1.73μs

1. Measurement Accuracy

The measurement accuracy of the ADC is calculated using total unadjusted error (TUE).

$$\text{Total Unadjusted Error (TUE)} = \sqrt{(\text{Gain Error})^2 + (\text{Offset Error})^2 + (\text{INL})^2} \quad (1)$$

After system level calibration, offset error and gain error can be ignored, and only offset thermal drift and gain thermal drift needs consideration, as shown in [Table 2](#). To reduce thermal drift errors, use a heat sink to reduce the temperature variation of the PMU and ADC.

Table 2. Measurement Accuracy of ADS9813 Under Various Operating Conditions

Test Condition	INL (ppm)	Offset Error (ppm)	Gain Error (ppm)	TUE (ppm)	Error (%)
TUE at 25°C	15.26	495.90	183.10	528.84	0.053
TUE at 25°C after calibration	15.26	0	0	15.26	0.0015
TUE at 25°C ±5°C after calibration	15.26	2.5	3.5	15.85	0.0016

For increased accuracy, the PMU and ADC can share a common reference voltage, as shown in [Figure 1](#). Configuring the reference voltage in such a ratiometric manner cancels the reference drift error.

2. Fast Channel Selection

VI cards can have each PMU MV_Ix output connected to the ADC channel, as shown in [Figure 1](#). Alternatively, the subsystem can use a multiplexer to connect multiple PMU outputs to one ADC channel. [Figure 2](#) shows an example where each PMU has 8 MV_Ix output channels multiplexed and connected to one ADC input channel. This enables higher channel densities for the VI instrumentation card and reduces cost.

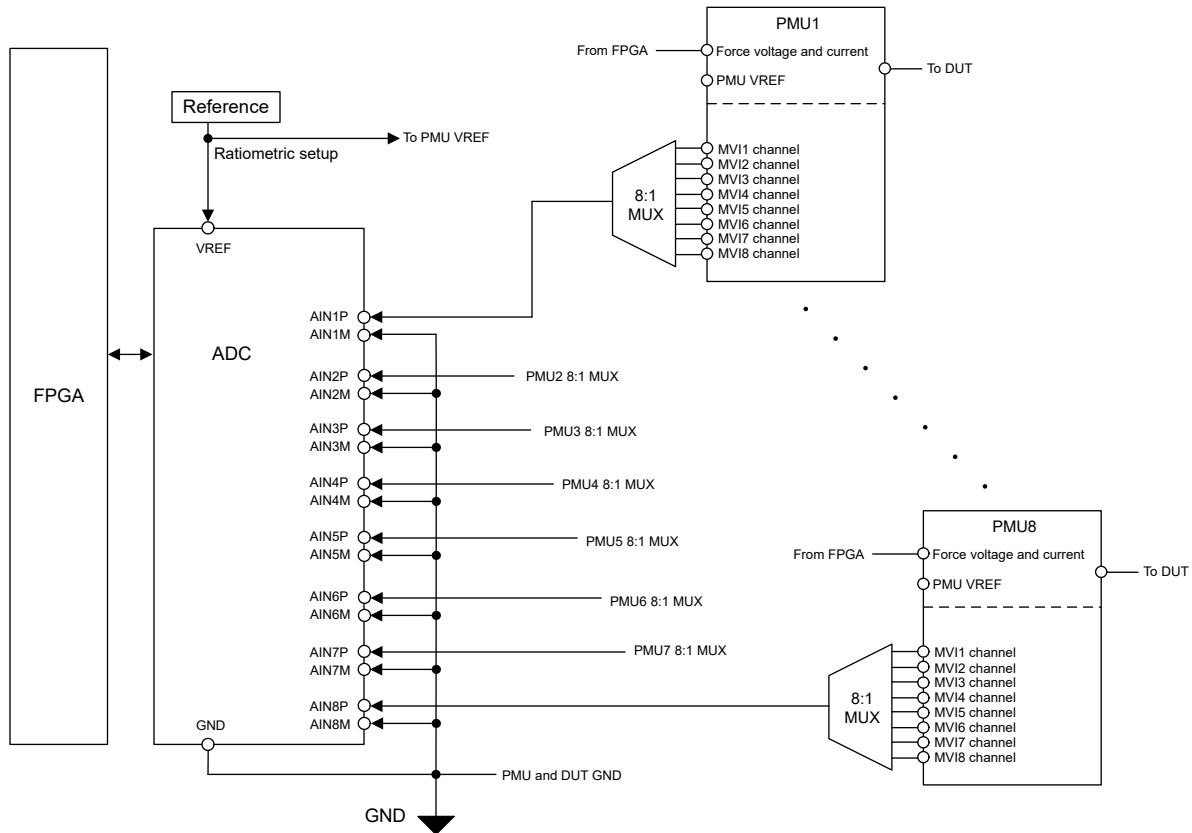


Figure 2. VI Card with 8:1 PMU:ADC Channel Count

The analog input bandwidth of the ADC must be higher when using multiplexers, like in [Figure 2](#), to accurately capture the change in PMU output signals as the multiplexer output is switched. The ADS9813 features two user-selectable analog input bandwidths: Low-noise mode, up to 21kHz, and wide-bandwidth mode, up to 400kHz. The wide-bandwidth mode allows the ADS9813 to sample multiplexed PMU output signals as the device enables step-settling to 99.99% of the full-scale (FS) signal in 1.73μs. The low-noise mode optimizes signal bandwidth versus noise performance in applications which require fewer PMU output measurements, as shown in [Table 3](#).

Table 3. Bandwidth Mode vs Settling Time and Performance

Bandwidth Mode	Settling Time (99.99% of FS)	SNR (typical)
Wide-bandwidth (up to 400kHz)	1.73μs	92dB
Low noise (up to 21kHz)	69.42μs	85.5dB

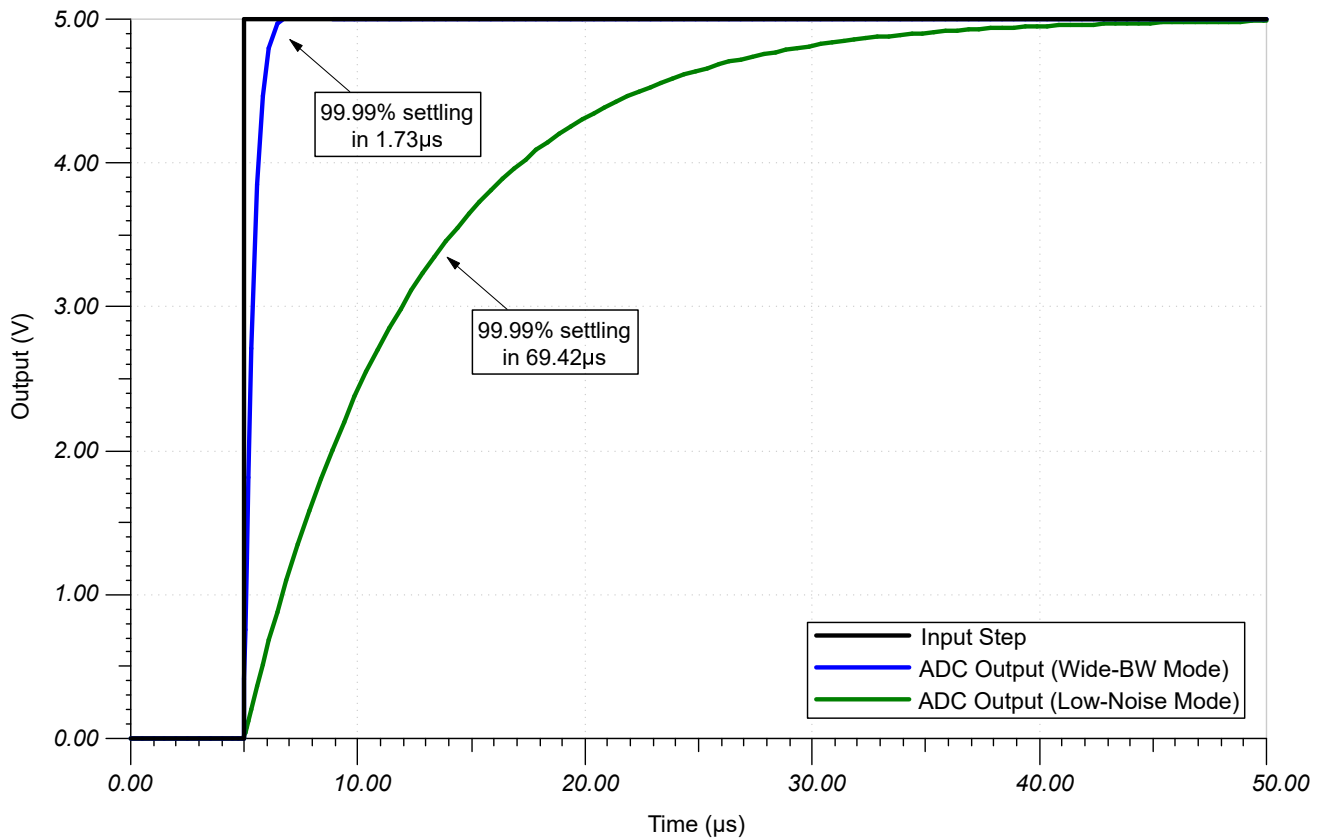


Figure 3. ADS9813 Settling Response of Low-Noise and Wide-Bandwidth Modes

3. Synchronizing Multiple Devices in a System

When using multiple ADS9813 devices to sample data at the same instant, the sampling clock can be shared to provide synchronous acquisition of all PMU outputs, as shown in Figure 4. Meanwhile, the data output and data-clock from each individual ADS9813 must be routed together to a dedicated FPGA input to read the data from all devices in parallel.

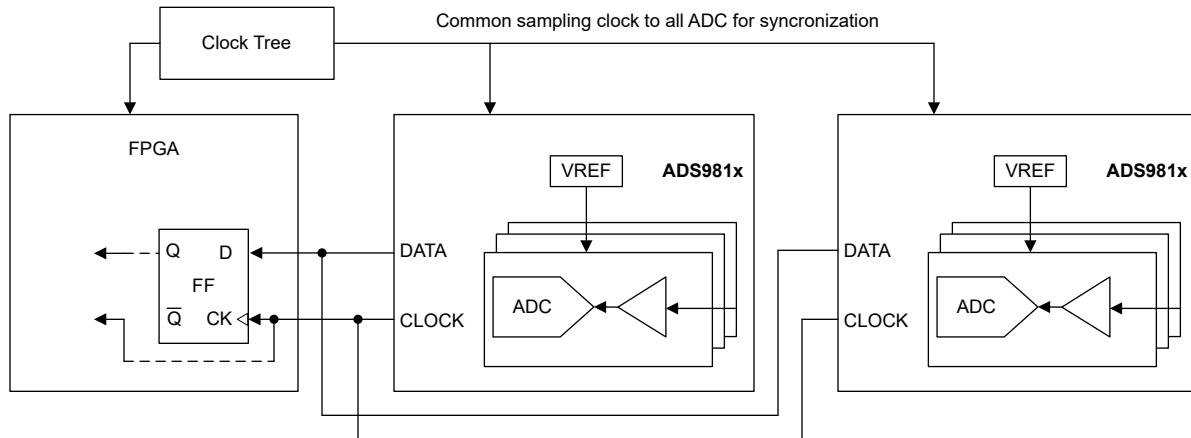


Figure 4. Source-Synchronous High-Speed Data Interface With FPGA

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