Analog Engineer's Circuit

Fast-Settling Low-Pass Filter Circuit

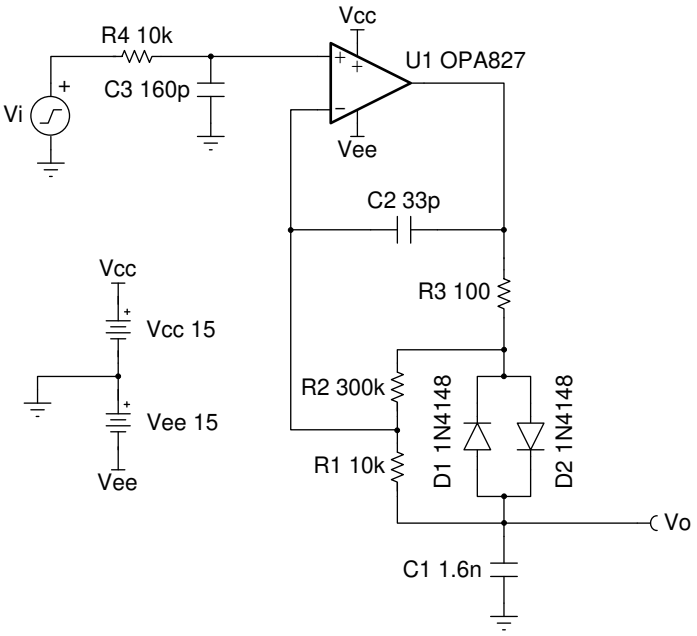
Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–12 V	12 V	–12 V	12 V	15 V	–15 V

Cutoff Frequency (f_c)	Diode Threshold Voltage (V_t)
10 kHz	20 mV

Design Description

This low-pass filter topology offers a significant improvement in settling time over the conventional single-pole RC filter. This is achieved through the use of diodes D_1 and D_2, that allow the filter capacitor to charge and discharge much faster when there is a large enough difference between the input and output voltages.



Design Notes

1. Observe the common-mode input limitations of the op amp.
2. Keeping C_1 small will ensure the op amp does not struggle to drive the capacitive load.
3. For the fastest settling time, use fast switching diodes.
4. The selected op amp should have sufficient output drive capability to charge C_1. R_3 limits the maximum charge current.

Design Steps

1. Select standard values for R_1 and C_1 based on f_C = 10kHz.

$$R_1 = 10k\Omega$$

$$C_1 = \frac{1}{2\pi \times f_C \times R_1} = \frac{1}{2\pi \times 10kHz \times 10k\Omega} = 1.6nF$$

2. Set the diode threshold voltage (V_t). This threshold is the minimum difference in voltage between the input and output that will result in diode conduction (fast capacitor charging and discharging).

$$V_t = \frac{V_f}{1 + \frac{R_2}{R_1}} \approx \frac{0.6V}{1 + \frac{R_2}{R_1}} = 20mV$$

$$R_2 = \left(\frac{0.6V}{20mV} - 1\right) \times R_1 = 290k\Omega \quad \approx \quad 300k\Omega \quad \text{(standard 5\% value)}$$

3. Select components for noise pre-filtering.

$$f_{c2} = 10 \times f_c = 100kHz$$

$$f_{c2} = \frac{1}{2\pi \times R_4 \times C_3}$$

$$\text{Select} \quad R_4 = R_1 = 10k\Omega$$

$$C_3 = \frac{C_1}{10} = 160pF$$

4. Add compensation components to stabilize U_1. R_3 limits the charge current into C_1 and also serves to isolate the capacitance from the op amp output when the diodes are conducting. Larger values will improve stability but increase C_1 charge time.

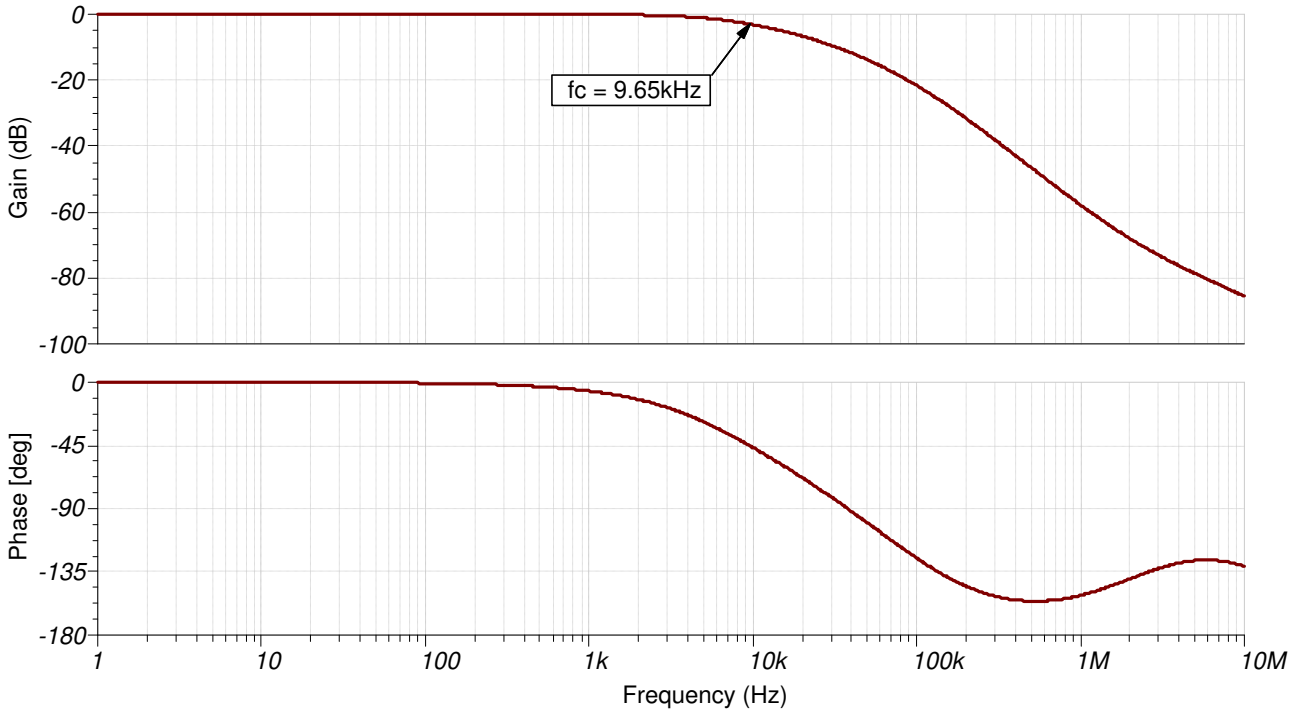
$$\text{Select} \quad R_3 = 100\Omega$$

5. C_2 provides local high frequency feedback to counteract the interaction between the input capacitance with the parallel combination of R_1 and R_2. To prevent interaction with C_1, select C_2 as the following shows:

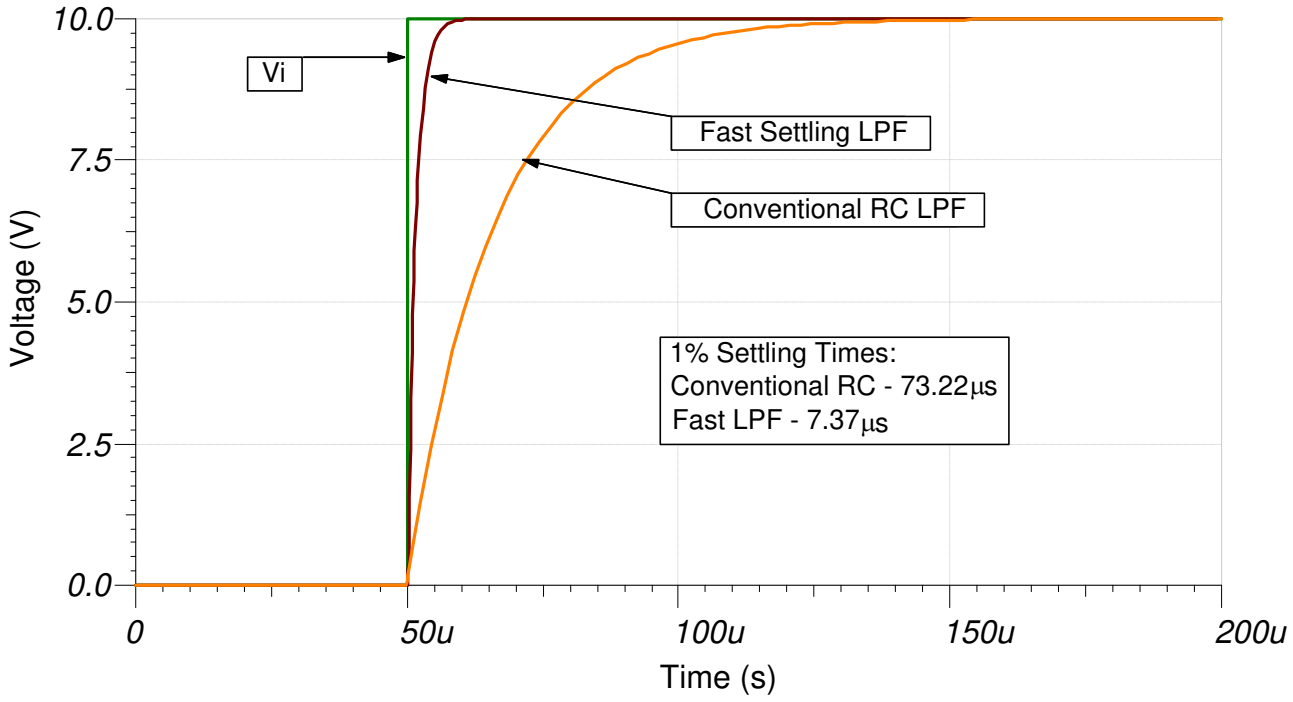
$$\text{Select} \quad C_2 = \frac{C_1}{50} = 32pF \approx 33pF \text{ (standard value)}$$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, SBOMAU1.

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC, see *TI Precision Labs*.

Design Featured Op Amp

OPA827	
V_{ss}	8 V to 36 V
V_{inCM}	V_{ee}+3 V to V_{cc}–3 V
V_{out}	V_{ee}+3 V to V_{cc}–3 V
V_{os}	75 µV
I_q	4.8 mA
I_b	3 pA
UGBW	22 MHz
SR	28 V/µs
#Channels	1
OPA827	

Design Alternate Op Amp

TLC072	
V_{ss}	4.5 V to 16 V
V_{inCM}	V_{ee}+0.5 V to V_{cc}–0.8 V
V_{out}	V_{ee}+350 mV to V_{cc}–1 V
V_{os}	390 µV
I_q	2.1 mA/Ch
I_b	1.5 pA
UGBW	10 MHz
SR	16 V/µs
#Channels	1, 2, and 4
TLC072	

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