Application Report

TLV4314-Q1
Functional Safety FIT Rate, FMD, and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TLV4314-Q1 (TSSOP-14 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

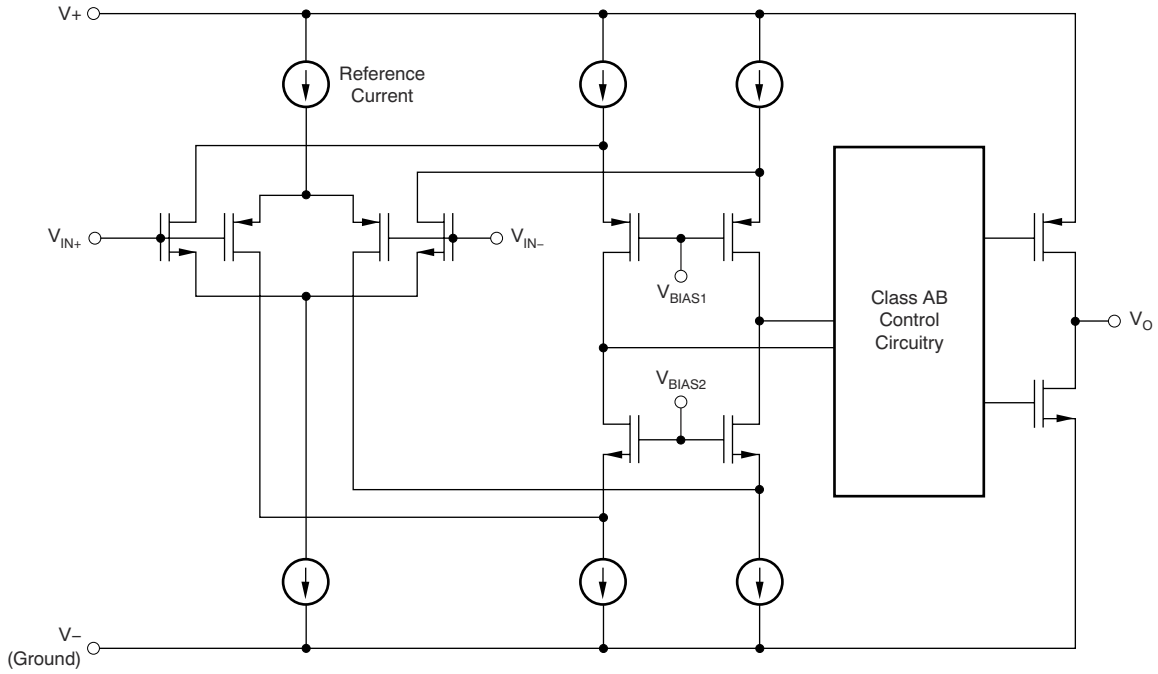

Figure 1-1. Functional Block Diagram

TLV4314-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TLV4314-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	11
Die FIT Rate	3
Package FIT Rate	8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators, Voltage Monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLV4314-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Out open (HIZ)	20%
Out saturate high	25%
Out saturate low	25%
Out functional not in specification voltage or timing	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLV4314-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TLV4314-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLV4314-Q1 data sheet.

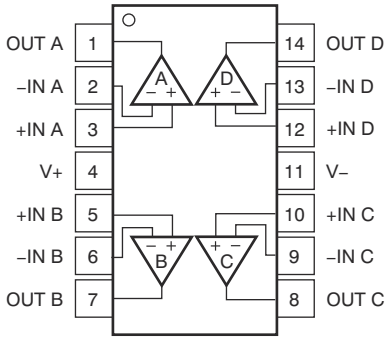

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Single-supply operation is used. For example, V+ = 5V and V- = 0V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
Out A	1	May cause device to overheat.	B
-IN A	2	Input at V- (GND) is valid input, however, desired application result is unlikely. Output goes high if +IN A is greater than zero volts.	C
+IN A	3	Input at V- (GND) is valid input, however, desired application result is unlikely. Output goes low if -IN A is greater than zero volts.	C
V+	4	Diodes from input to V+ may turn on due to input signal and cause electrical overstress (EOS). Main supply shorted. No power to device.	B
+IN B	5	Input at V- (GND) is valid input, however, desired application result is unlikely. Output goes low if -IN B is greater than zero volts.	C

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
-IN B	6	Input at V- (GND) is valid input, however, desired application result is unlikely. Output goes high if +IN B is greater than zero volts.	C
OUT B	7	May cause device to overheat.	B
OUT C	8	May cause device to overheat.	B
-IN C	9	Input at V- (GND) is valid input, however, desired application result is unlikely. Output goes high if +IN C is greater than zero volts.	C
+IN C	10	Input at V- (GND) is valid input, however, desired application result is unlikely. Output goes low if -IN C is greater than zero volts.	C
V-	11	Normal operation.	D
+IN D	12	Input at V- (GND) is valid input, however, desired application result is unlikely. Output goes low if -IN D is greater than zero volts.	C
-IN D	13	Input at V- (GND) is valid input, however, desired application result is unlikely. Output goes high if +IN D is greater than zero volts.	C
OUT D	14	May cause device to overheat.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	Output cannot be used by application.	C
-IN A	2	Floating input, circuit will likely not function as expected. Output may be high or low.	C
+IN A	3	Floating input, circuit will likely not function as expected. Output may be high or low.	C
V+	4	Highest voltage pin will drive V+ pin internally via internal diode.	B
+IN B	5	Floating input, circuit will likely not function as expected. Output may be high or low.	C
-IN B	6	Floating input, circuit will likely not function as expected. Output may be high or low.	C
OUT B	7	Output cannot be used by application.	C
OUT C	8	Output cannot be used by applications.	C
-IN C	9	Floating input, circuit will likely not function as expected. Output may be high or low.	C
+IN C	10	Floating input, circuit will likely not function as expected. Output may be high or low.	C
V-	11	Lowest voltage pin will drive V- pin internally via internal diode.	B
+IN D	12	Floating input, circuit will likely not function as expected. Output may be high or low.	C
-IN D	13	Floating input, circuit will likely not function as expected. Output may be high or low.	C
OUT D	14	Output cannot be used by application.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	-IN A	Negative feedback, creates unity gain buffer.	C
-IN A	2	+IN A	No damage to device. Application circuit will not work.	C
+IN A	3	V+	Input at V+ is a valid input, however, desired application result is unlikely. Output goes high if -IN A is less than V+.	C
V+	4	+IN B	Input at V+ is a valid input, however, desired application result is unlikely. Output goes high if -IN B is less than V+.	C
+IN B	5	-IN B	No damage to device. Application circuit will not work.	C
-IN B	6	OUT B	Op amp configured as unity gain buffer.	C
OUT B	7	OUT C	Depending on output load and circuit, excess current could be drawn.	B
OUT C	8	-IN C	Op amp configured as unity gain buffer.	C
-IN C	9	+IN C	No damage to device. Application circuit will not work.	C
+IN C	10	V-	Input at V- is a valid input, however, desired application result is unlikely. Output goes low if -IN C is greater than zero volts.	C
V-	11	+IN D	Input at V- is a valid input, however, desired application result is unlikely. Output goes low if -IN D is greater than zero volts.	C
+IN D	12	-IN D	No damage to device. Application circuit will not work.	C
-IN D	13	OUT D	Op amp configured as unity gain buffer.	C
OUT D	14	OUT A	Depending on output load and circuit, excess current could be drawn.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	May cause device to overheat.	B
-IN A	2	Input at V+ is valid input, however, desired application result is unlikely. Output goes low if +IN A is less than V+.	C
+IN A	3	Input at V+ is valid input, however, desired application result is unlikely. Output goes high if -IN A is less than V+.	C
V+	4	Normal operation.	D
+IN B	5	Input at V+ is valid input, however, desired application result is unlikely. Output goes high if -IN B is less than V+.	C
-IN B	6	Input at V+ is valid input, however, desired application result is unlikely. Output goes low if +IN B is less than V+.	C
OUT B	7	May cause device to overheat.	B
OUT C	8	May cause device to overheat.	B
-IN C	9	Input at V+ is valid input, however, desired application result is unlikely. Output goes low if +IN C is less than V+.	C
+IN C	10	Input at V+ is valid input, however, desired application result is unlikely. Output goes high in -IN C is less than V+.	C
V-	11	Main supply shorted to V- (GND). No power to device.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
+IN D	12	Input at V+ is valid input, however, desired application result is unlikely. Ouput goes high if -IN D is less than V+.	C
-IN D	13	Input at V+ is valid input, however, desired application result is unlikely. Output goes low if +IN D is less than V+.	C
OUT D	14	May cause device to overheat.	B

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