



## Design Notes

1. This topology is meant for high-side implementation, where the IN+ and IN– pin of the INA901-SP are referenced to  $V_{CM}$  of the application. While this circuit is capable of withstanding the full 65 V common mode of the INA901-SP, a limitation exists on the lower end, and  $V_{CM}$  must be held  $> 2.5$  V. This is due to reference of the TL1431-SP of 2.5 V, and the need for the current flow to sink towards the TL1431-SP for proper offset voltage creation. Therefore, the common-mode voltage of the IN– pin must be  $> 2.5$  V to ensure valid operation.
2. For the presented design, a 24  $V_{CM}$  is considered, and the JANS2N2222A is chosen to complete the design based on these parameters. A BJT possessing greater  $V_{CE}$  capabilities is needed for high-voltage applications  $> 50$   $V_{CM}$ .
3. Care should be taken when designing with the INA901-SP to ensure the full-scale input range of the device remains above 20 mV for best performance. If  $V_{SENSE}$  is allowed below 20 mV, the device may produce additional errors inside of this operating condition. See the [INA901-SP Radiation Hardened, –15-V to 65-V Common Mode, Unidirectional Current-Shunt Monitor](#) data sheet for more information.
4. While this circuit provides the ability to measure in multiple directions, it does not change the fact that the INA901-SP is inherently a unidirectional device. This infers that one direction of current sensing will be more accurate than the other, as one direction will measure towards the offset voltage of the device, leading to increased error in this direction. The effects of this may be mitigated in part by the use of a one-point calibration, and is discussed later in this document.

## Design Steps

- **Design the Offset Current:** The offset current ultimately flows over R1 to create the RTI offset sense voltage, but is determined by resistor R2. Because the default reference voltage of the TL1431-SP is 2.5 V, a 1-k $\Omega$  resistor is chosen, and the offset current is calculated as shown in the following equation:

$$I_{OFFSET} = \frac{V_{REF, TL1431}}{R2} = \frac{2.5 \text{ V}}{1 \text{ k}\Omega} = 2.5 \text{ mA}$$

- **Design RTI Offset Voltage Point:** With  $I_{OFFSET}$  determined in the previous equation, R1 may now be selected to determine the  $V_{REF}$  point of the design. For the given design, a desired  $V_{REF}$  of 2 V was chosen, but resistor selection ultimately led to a 1.96-V design. This point is determined by the following equations:

$$V_{SENSE, RTI} = R1 \times I_{OFFSET} = 39.2 \Omega \times 2.5 \text{ mA} = 98 \text{ mV}$$

$$V_{REF} = V_{SENSE, RTI} \times GAIN = 98 \text{ mV} \times 20 \frac{\text{V}}{\text{V}} = 1.96 \text{ V}$$

- **Choose  $R_{SHUNT}$  to Optimize Input Range:** With the RTI Offset designed, a shunt may now be chosen for the desired sensing range. For the INA901-SP, maintain the lower sensing bound at  $> 20$  mV for optimal performance, this shows that the amount of sensing headroom from  $V_{REF}$  is calculated as in the following equation:

$$V_{SHUNT, max} = 98 \text{ mV} - 20 \text{ mV} = 78 \text{ mV}$$

From the desired  $-7.5$ -A design target, it is calculated that the maximum allowable shunt to achieve this goal is found using the following:

$$R_{SHUNT, max} = \frac{V_{SHUNT, max}}{I_{LOAD, max}} = \frac{78 \text{ mV}}{7.5 \text{ A}} = 10.4 \text{ m}\Omega$$

As the design  $I_{LOAD}$  target in the remaining direction is symmetric about  $V_{REF}$ , 10 m $\Omega$  was selected to complete the design. The final input  $V_{SENSE}$  swing is calculated as:

$$V_{SHUNT, min} + V_{OFFSET, RTI} \leq V_{SENSE} \leq V_{SHUNT, max} + V_{OFFSET, RTI}$$

$$-75 \text{ mV} + 98 \text{ mV} \leq V_{SENSE} \leq 75 \text{ mV} + 98 \text{ mV}$$

$$23 \text{ mV} \leq V_{SENSE} \leq 173 \text{ mV}$$

The expected corresponding output is found using:

$$V_{\text{SENSE, min}} \times \text{GAIN} \leq V_{\text{OUT}} \leq V_{\text{SENSE, max}} \times \text{GAIN}$$

$$23 \text{ mV} \times 20 \frac{\text{V}}{\text{V}} \leq V_{\text{OUT}} \leq 173 \text{ mV} \times 20 \frac{\text{V}}{\text{V}}$$

$$460 \text{ mV} \leq V_{\text{OUT}} \leq 3.46 \text{ V}$$

- **Verify shunt derating is sufficient:** A necessary aspect of proper shunt design is ensuring that the design choice has sufficient margin for power derating. As the device heats in the environment, the amount of power the shunt is capable of dissipating is derated by a certain factor. For continuous sensing, this factor can be as high as 0.6. Taking this into account, for the design, a shunt must be chosen that is rated for at least the following:

$$P_{\text{RATING}} = \frac{P_{\text{LOSS}}}{\text{Derating Factor}} = \frac{I_{\text{LOAD, max}}^2 \times R_{\text{SHUNT}}}{0.6} = \frac{7.5 \text{ A}^2 \times 10 \text{ m}\Omega}{0.6} = 937.5 \text{ mW}$$

So for a successful design, a shunt of at least 1-W rated power is chosen for continuous sensing.

- Choose the correct BJT NPN transistor: Dependent on the common modes expected to be seen by the application, a corresponding BJT must be chosen to be able to withstand this  $V_{\text{CM}}$ . The voltage ultimately seen by the BJT is calculated as in the following equation:

$$V_{\text{CE, max}} = V_{\text{CM}} - V_{\text{REF, TL1431}} = 24 \text{ V} - 2.5 \text{ V} = 21.5 \text{ V}$$

Add some margin for any potential voltage transients on the common mode. For the given design, the JANS2N2222A is chosen, as it is able to withstand a  $V_{\text{CE}}$  of 50 V maximum, and meets the needs of the design. The expected power dissipated through the BJT is found with the following equation:

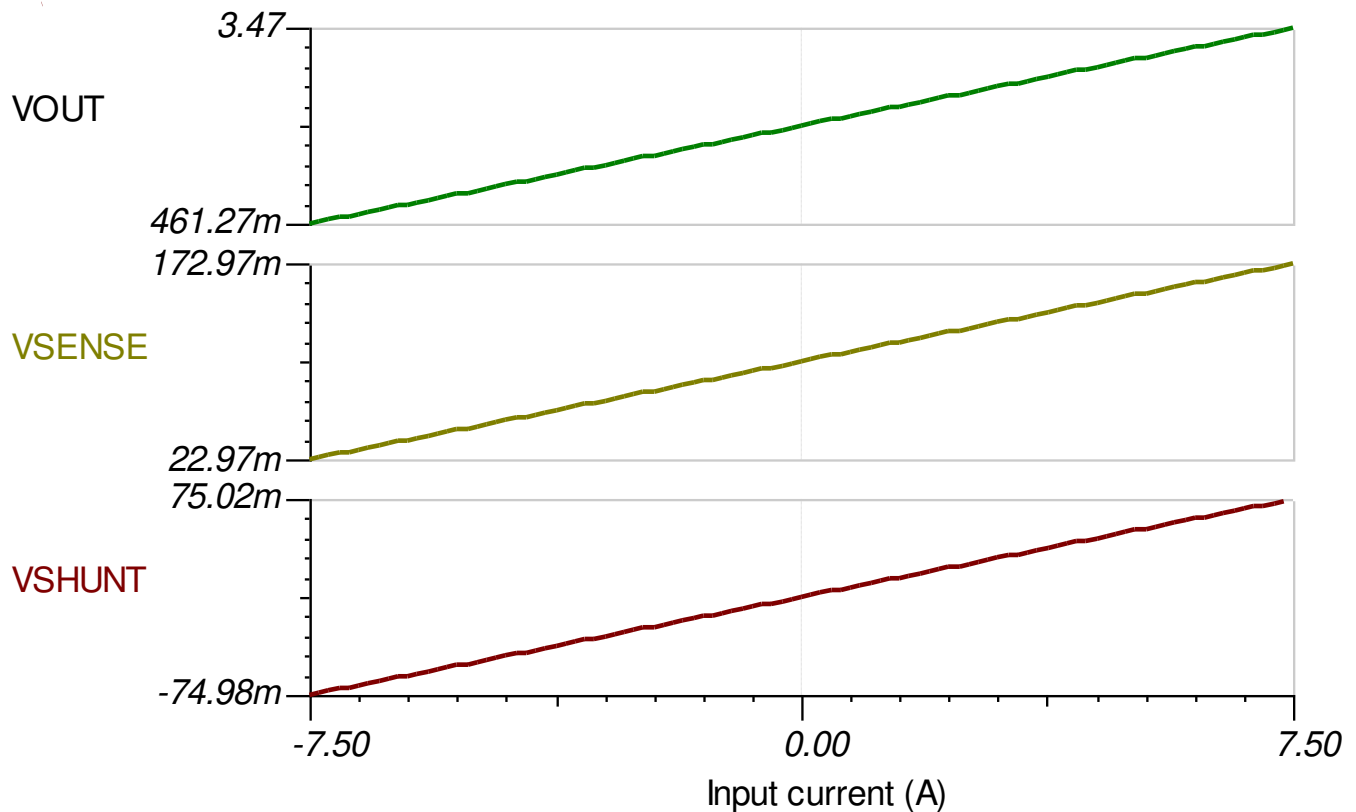
$$P_{\text{LOSS, BJT}} = I_{\text{OFFSET}} \times V_{\text{CE}} = 2.5 \text{ mA} \times 21.5 \text{ V} = 53.75 \text{ mW}$$

- **Examine Error. Calibrate if necessary:** As discussed in previous sections, it is expected that the current sense amplifier will be more accurate in the direction of measurement as the output is driven toward supply. Less accurate measurements are expected as the sense voltage decreases, and errors from the offset voltage begin to have more effect. A remedy for this is to perform a one-point calibration in logic to reduce the effects of the offset voltage.

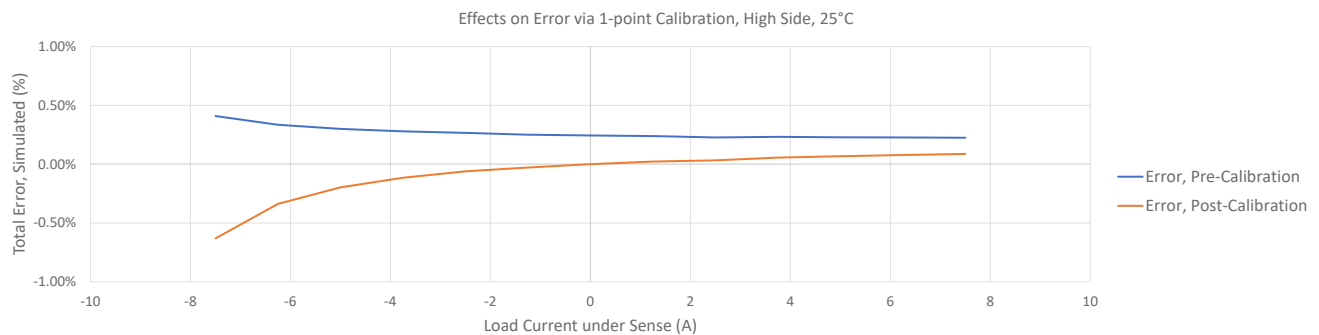
A one-point calibration is performed by applying the condition,  $V_{\text{SHUNT}} = 0 \text{ mV}$  to the system, capturing the actual value output by the INA901-SP, and maintaining the difference between this value and the calculated ideal in memory. The output of the device is then consistently shifted by this amount. An example of the effects of this are shown in the following simulated results.

## Design Simulations

DC Sweep Results,  $-7.5\text{ A} < I_{\text{LOAD}} < 7.5\text{ A}$



### INA901-SP High-Side Bidirectional Circuit Performance Over Load



### Error Curves, Pre- and Post-Calibration From Simulation Data

Calibration of the raw data from simulation results in the  $V_{\text{SENSE}} = 0$  point shifting to an error of 0%, and a  $< 1\%$  error over the full load range, thus meeting the design goal. Note that parameters such as device offset and input bias currents in TINA-TI models reflect typical data sheet parameters, and additional error may be exhibited pre- and post-calibration due to variation in these parameters. For more information, see the [Bidirectional Topologies for the INA901-SP](#) application note.

## Design References

See the TI Precision Labs, [Current Sense Amplifiers](#) video series.

### Design Featured Current Sense Amplifier

INA901-SP	
$V_S$	2.7 V to 16 V
$V_{CM}$	-15 V to 65 V
$V_{OUT}$	GND+3 mV to $V_S - 50$ mV, typical
$V_{OS}$	$\pm 500$ $\mu$ V, typical
$I_q$	350 $\mu$ A, typical
$I_B$	$\pm 8$ $\mu$ A, typical
TID Characterization (ELDRS-Free)	50 krad (Si)
SEL Immune to LET	75 MeV-cm <sup>2</sup> /mg
<a href="#">INA901-SP</a>	

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