

PHASE-NOISE (JITTER) PERFORMANCE OF CDC7005 WITH DIFFERENT VCXOs

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ABSTRACT

The phase-noise performance of the CDC7005 depends on the phase noise of the reference clock, VCXO clock, and the CDC7005 itself. This application report shows the phase-noise performance of the Texas Instruments CDC7005 clock synthesizer with different VCXOs. This application report helps users choose the right clocking solution for their applications. The data shows that the CDC7005 can easily generate clocks with less than 500 fs of jitter. A low-jitter clock is invariably required for many applications.

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1 Introduction

The CDC7005 is a low-phase-noise clock synthesizer with five programmable LVPECL outputs. The CDC7005 with a low-pass loop filter (external or internal) and VCXO complete the phase-locked loop (PLL). So, selecting the optimal VCXO and optimizing the loop bandwidth is critical for achieving the best performance from the CDC7005. The PLL's output phase noise was measured for each VCXO tested alongside the CDC7005. The RMS jitter was calculated from the plot over a frequency band of interest.

2 Test Equipment and Setup

All measurements are taken at nominal power supply, room temperature, and PLL's locked condition (except for the buffer mode). The PN9000 automatic phase-noise test system from Aeroflex was used to measure the phase noise and calculate the jitter from the phase-noise value.

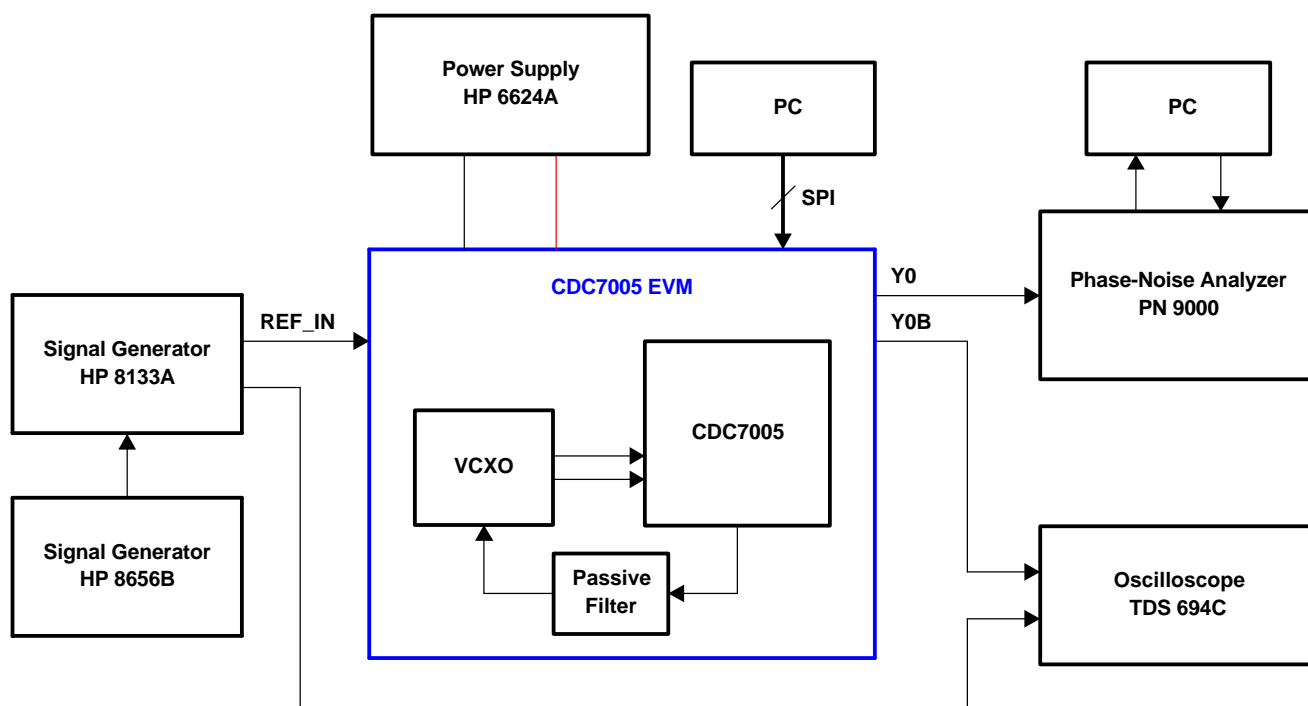
The CDC7005 EVM is used to take the VCXO and PLL's output phase-noise measurement. All five LVPECL outputs are properly terminated.

The following test setup and equipment are used for most of the measurements. Only the characterization of noise performance in the buffer mode has been done differently to maximize the measurement resolution.

The phase noise can be measured up to 40 MHz from the carrier frequency using the available facilities. Some of the measurements are taken up to 10 MHz or 1 MHz from the carrier, depending on the clock frequency.

Every doubling of the frequency causes the phase-noise value to go up approximately 6 dB. So, in some of the phase-noise plots, it can be seen that the output phase noise is more than the input clock phase because the output clock frequency is a multiplied copy of the input clock.

Spurs did not show in the phase-noise plots. The sources of the spurs are the input clock, the power supply, the test equipment, etc. In jitter measurements, spurs are considered.



B0065-01

Figure 1. Test Equipment Setup

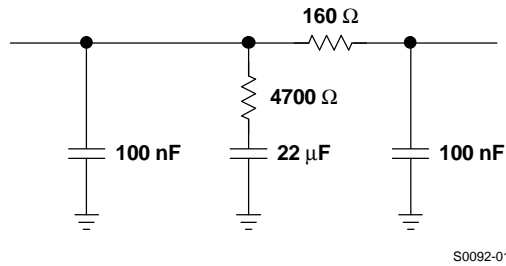


Figure 2. Passive Loop Filter Circuit

3 Test Summary

3.1 Phase-Noise Performance of CDC7005 LVPECL Path (Buffer Mode)

The CDC7005 can be used as a simple 1:5 LVPECL buffer with divider options. In this mode, the signal generators are directly connected to the VCXO inputs of the CDC7005.

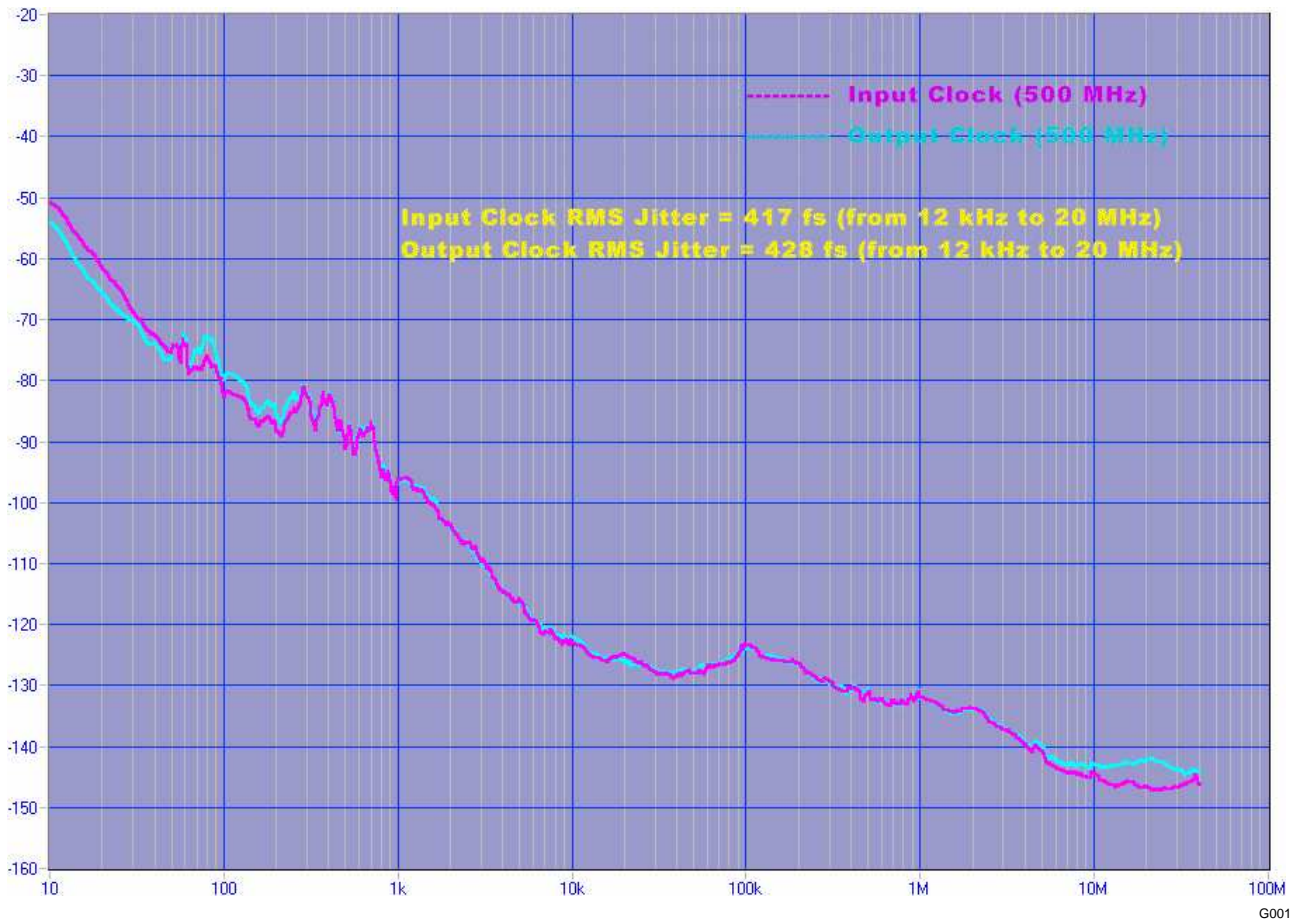


Figure 3. Phase-Noise Performance of the LVPECL Path

This data clearly indicates that as a buffer, the CDC7005 adds a few fs jitter to its input. The added jitter number can vary over frequency.

For more information about the CDC7005 as a buffer, see the *Using the CDC7005 as a 1:5 PECL Buffer With a Programmable Divider Ratio on Each Output* application brief ([SCAA060](#)).

3.2 Phase-Noise Performance of the CDC7005 With High-Jitter Reference Clock and Toyocom 61.44 MHz

A regular PLL has been used to generate a 10-MHz high-jitter reference clock to drive the CDC7005.

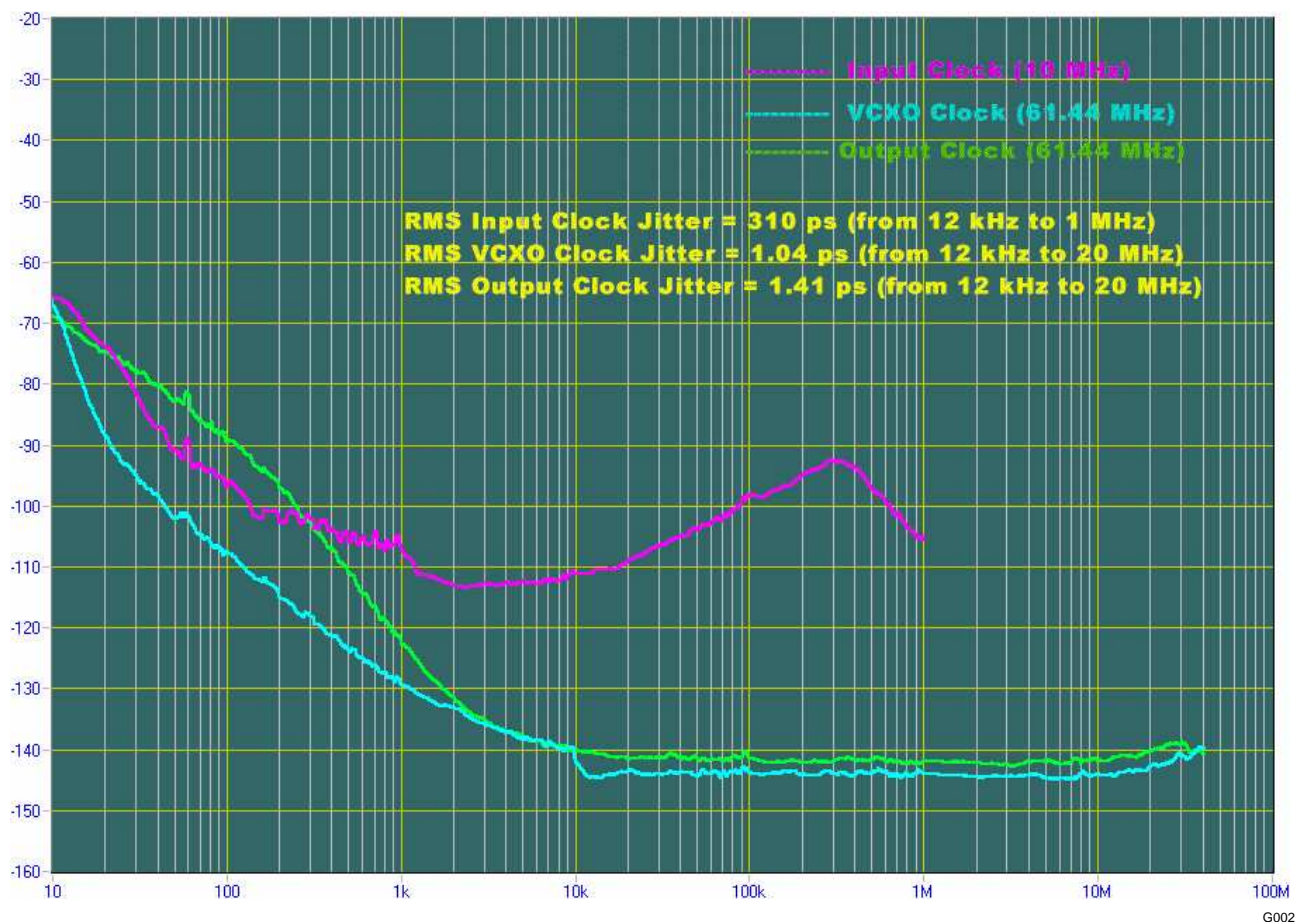


Figure 4. Phase-Noise Plot with High-Jitter Reference Clock

Note:

The output is 6.144 times the multiplied version of the input clock frequency with low jitter. All of the high-frequency input jitters are cleaned; therefore, the CDC7005 provides a low-phase-noise clock.

To compare input and output phase-noise plots, the reference clock plot must be raised by 15.76 dB ($20 \log 6.144$).

3.3 Phase-Noise Performance of the CDC7005 With Toyocom 76.8-MHz VCX

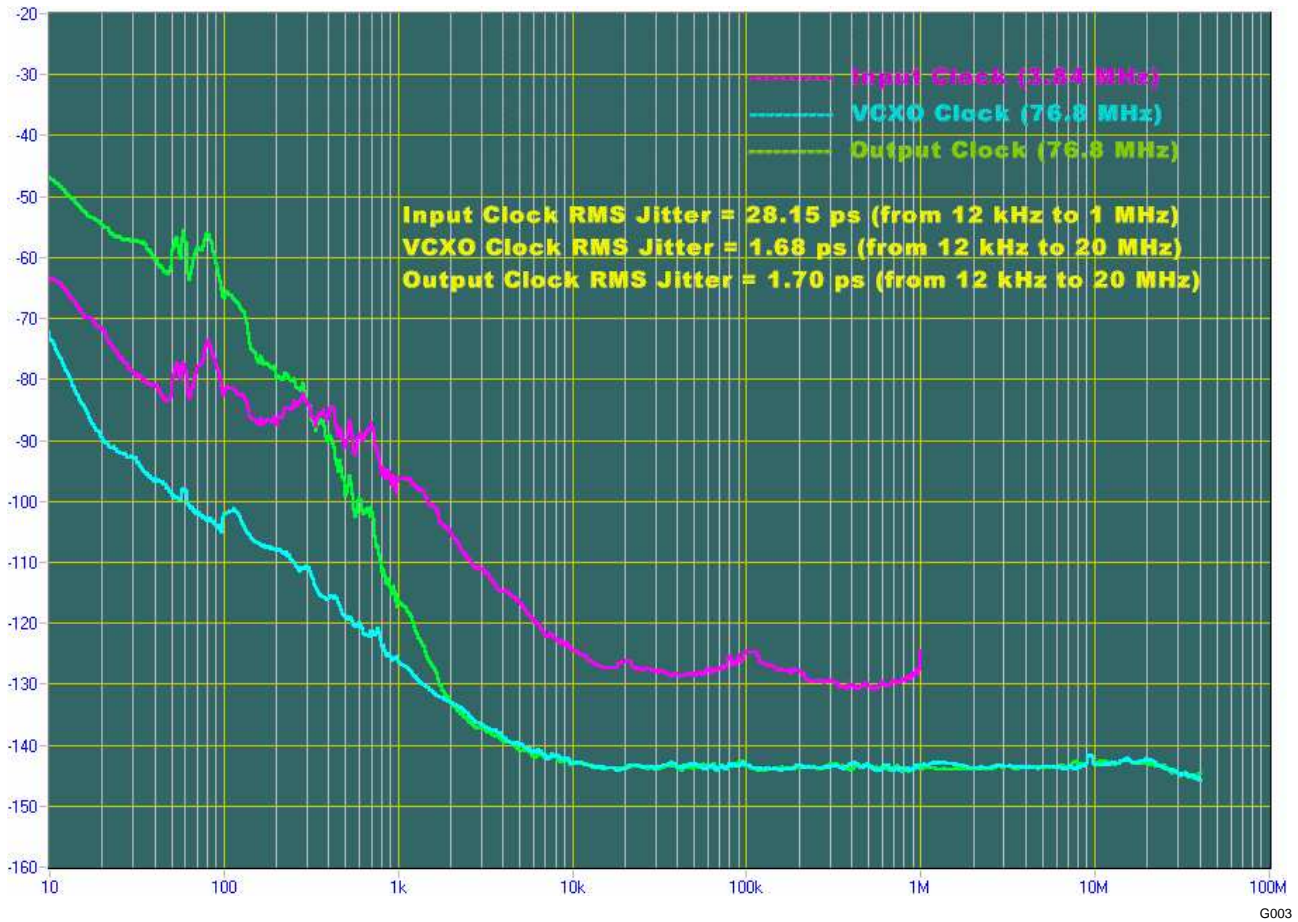


Figure 5. Phase-Noise Performance of the 76.8-MHz Output Clock From the CDC7005

Note:

The output is 24 times the multiplied version of the input clock frequency with low jitter. The output phase noise at lower frequencies is more than the input clock phase noise, because the output is 24 times higher than the input clock frequency.

To compare input and output phase-noise plots, the reference clock plot must be raised by 27.6 dB ($20 \log 24$).

3.4 Phase-Noise Performance of the CDC7005 With Pletronics 92.16-MHz VCXO

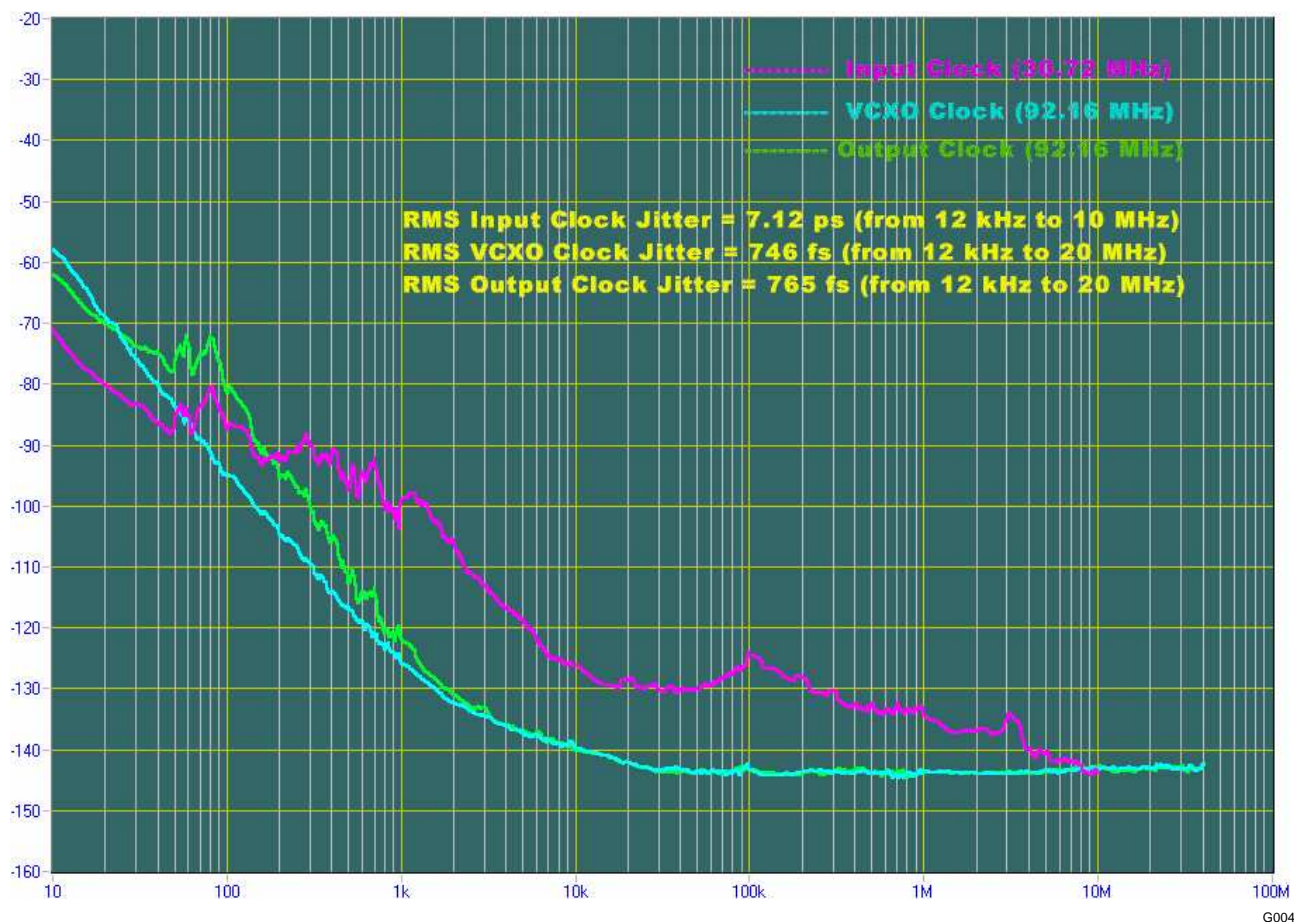


Figure 6. Phase-Noise Performance of the 92.16-MHz Output Clock From the CDC7005

Note:

The output is three times the multiplied version of the input clock frequency with low jitter. Below the loop bandwidth frequency, the output phase noise is approximately 9 dB ($20 \log 3$) higher.

3.5 Phase-Noise Performance of the CDC7005 With Vectron 100-MHz VCXO

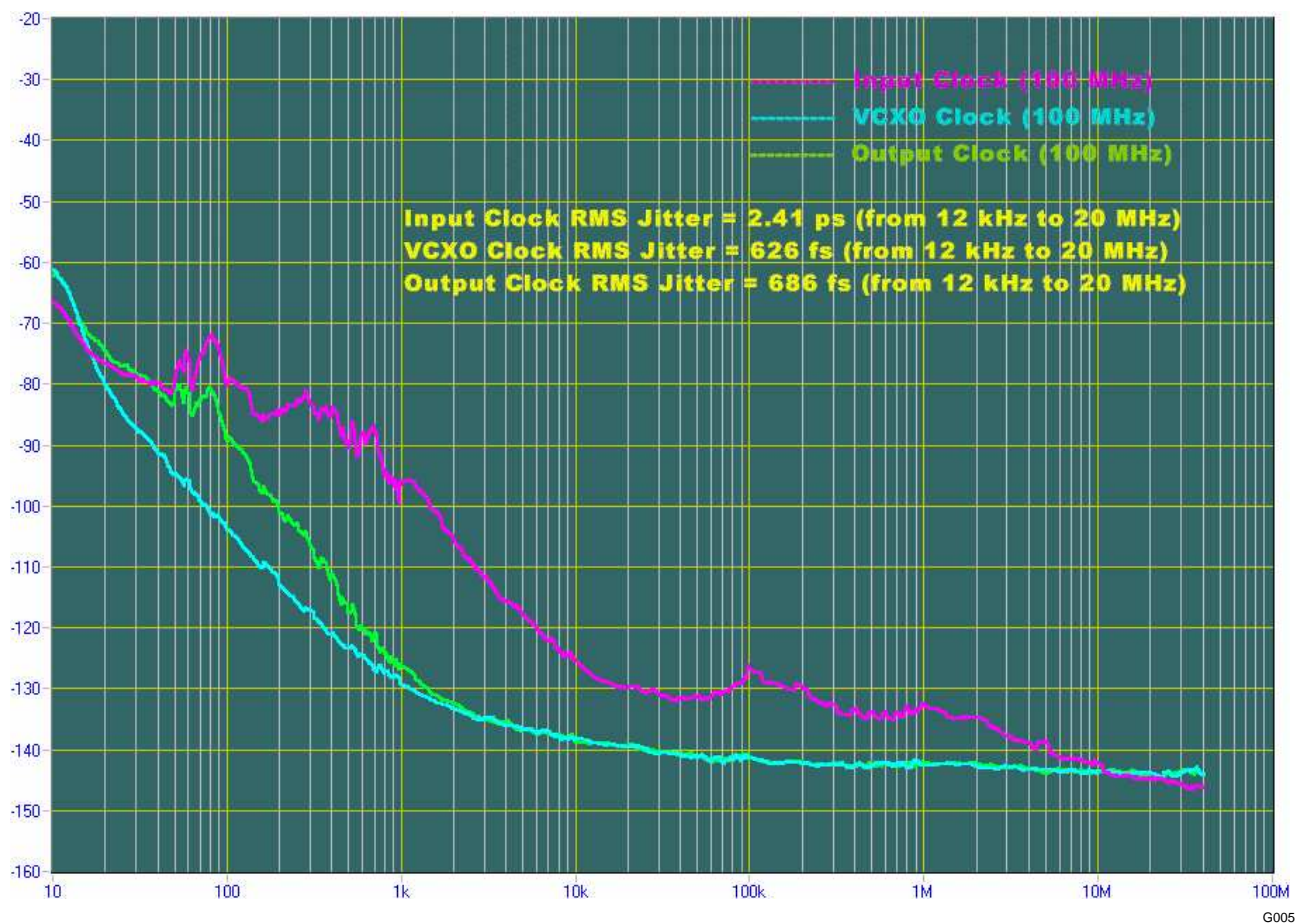


Figure 7. Phase-Noise Performance of the 100-MHz Output Clock From the CDC7005

Note:

The CDC7005 is acting as a jitter cleaner.

3.6 Phase-Noise Performance of the CDC7005 With Toyocom 122.88-MHz VCXO

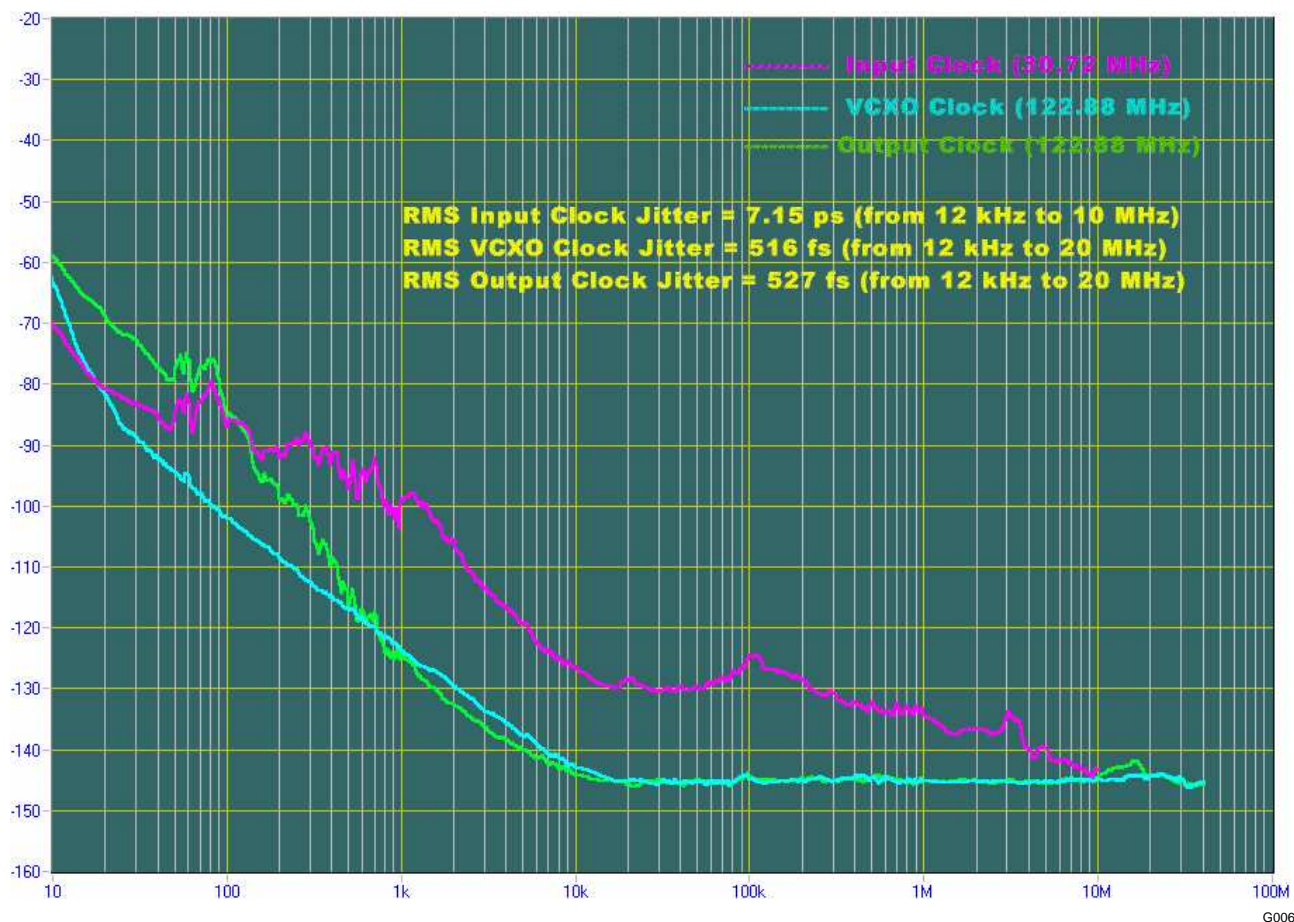


Figure 8. Phase-Noise Performance of the 122.88-MHz Output Clock From the CDC7005

Note:

The output is four times the multiplied version of the input clock frequency with low jitter.

To compare input and output phase-noise plots, the reference clock plot must be raised by 12 dB (20 log 4).

3.7 Phase-Noise Performance of the CDC7005 With Vectron 125-MHz VCXO

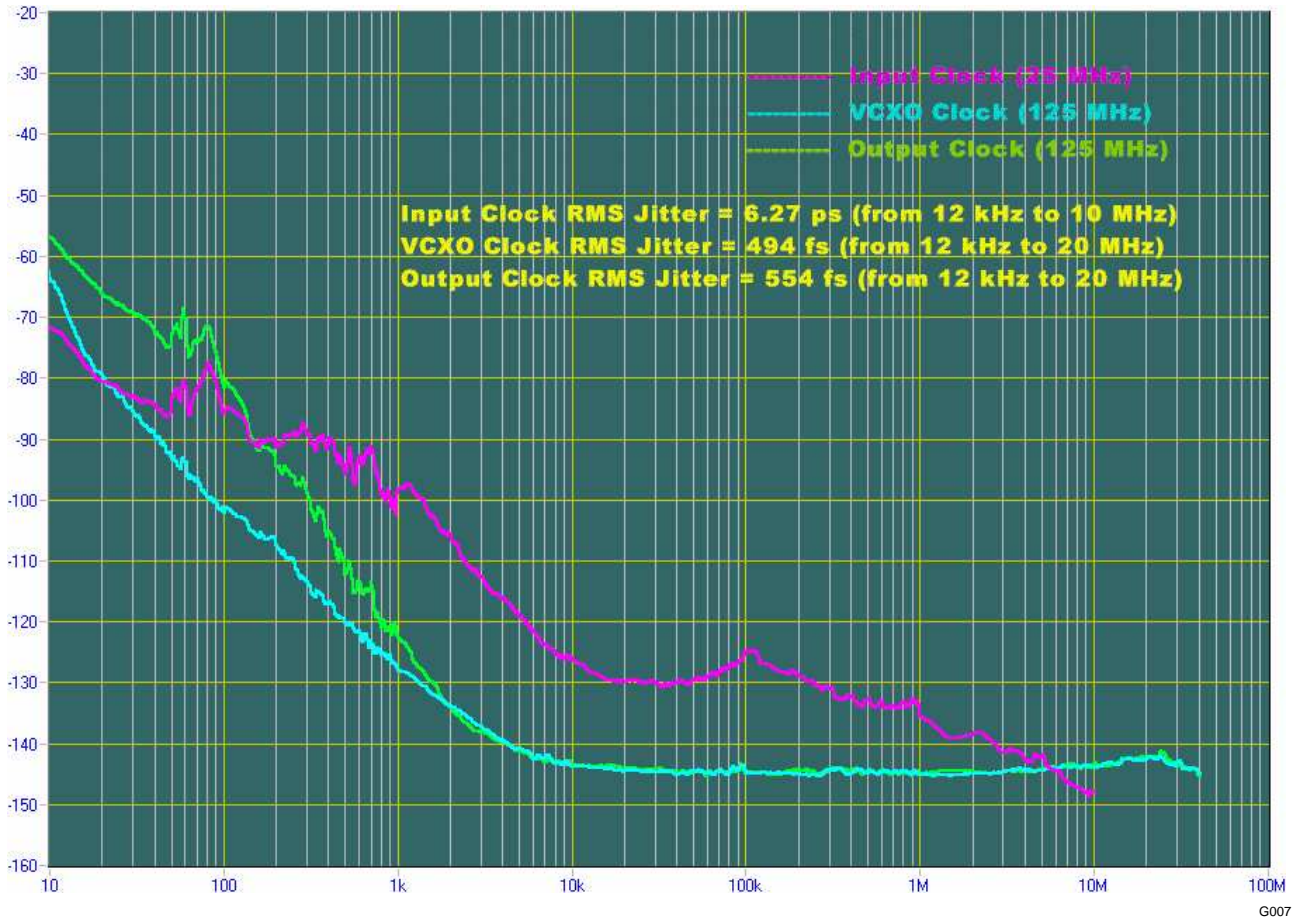


Figure 9. Phase-Noise Performance of the 125-MHz Output Clock From the CDC7005

Note:

The output is five times the multiplied version of the input clock frequency with low jitter.

To compare input and output phase-noise plots, the reference clock plot must be raised by 13.97 dB ($20 \log 5$).

3.8 Phase-Noise Performance of the CDC7005 With Toyocom 153.6-MHz VCXO

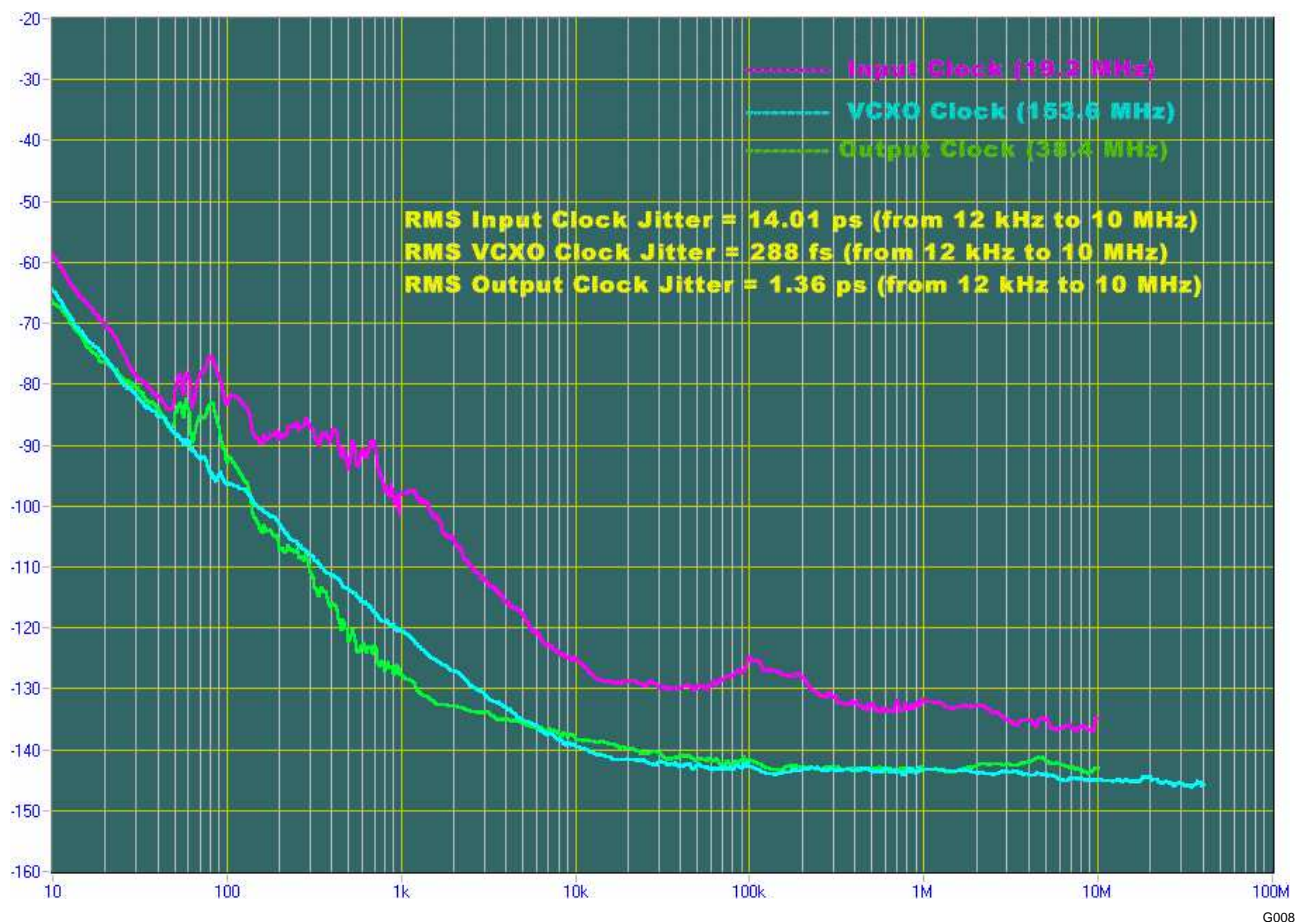


Figure 10. Phase-Noise Performance of the 38.4-MHz Output Clock From the CDC7005

Note:

The output is two times the multiplied version of the input clock frequency with low jitter.

To compare input and output phase-noise plots, the reference clock plot must be raised by 6 dB ($20 \log 2$).

3.9 Phase-Noise Performance of the CDC7005 With Pletronics 155.52-MHz VCXO

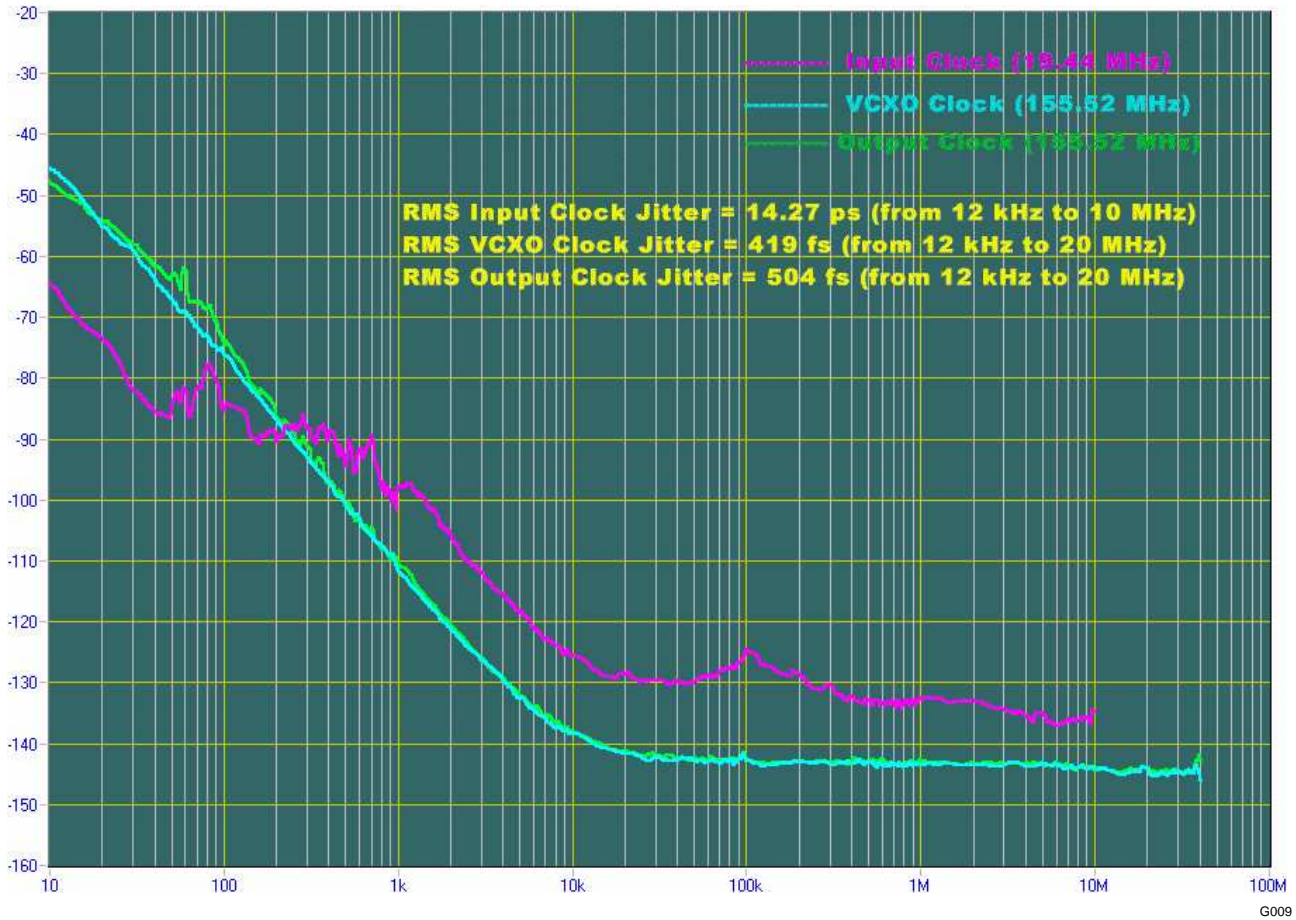


Figure 11. Phase-Noise Performance of the 155.52-MHz Output Clock From the CDC7005

Note:

The output clock is eight times the multiplied version of the input clock frequency with low jitter. The output clock can easily meet the SONNET specifications.

To compare input and output phase-noise plots, the reference clock plot must be raised by 18 dB (20 log 8).

3.10 Phase-Noise Performance of the CDC7005 With Toyocom 245.76-MHz

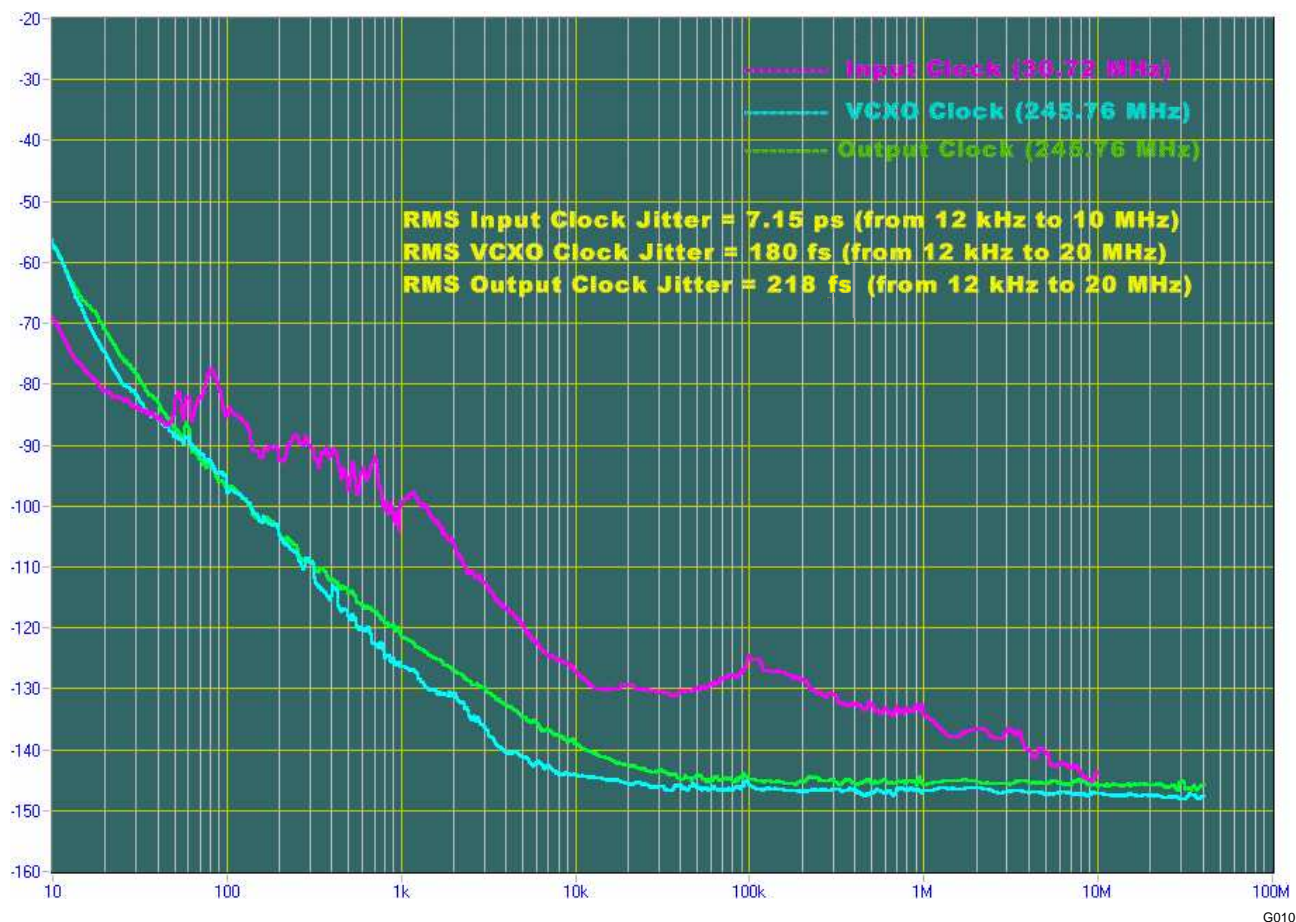


Figure 12. Phase-Noise Performance of the 245.76-MHz Output Clock From the CDC7005

Note:

The output clock is eight times the multiplied version of the input clock frequency with low jitter.

To compare input and output phase-noise plots, the reference clock plot must be raised by 18 dB (20 log 8).

3.11 Phase-Noise Performance of the CDC7005 With Vectron 248.832-MHz VCXO

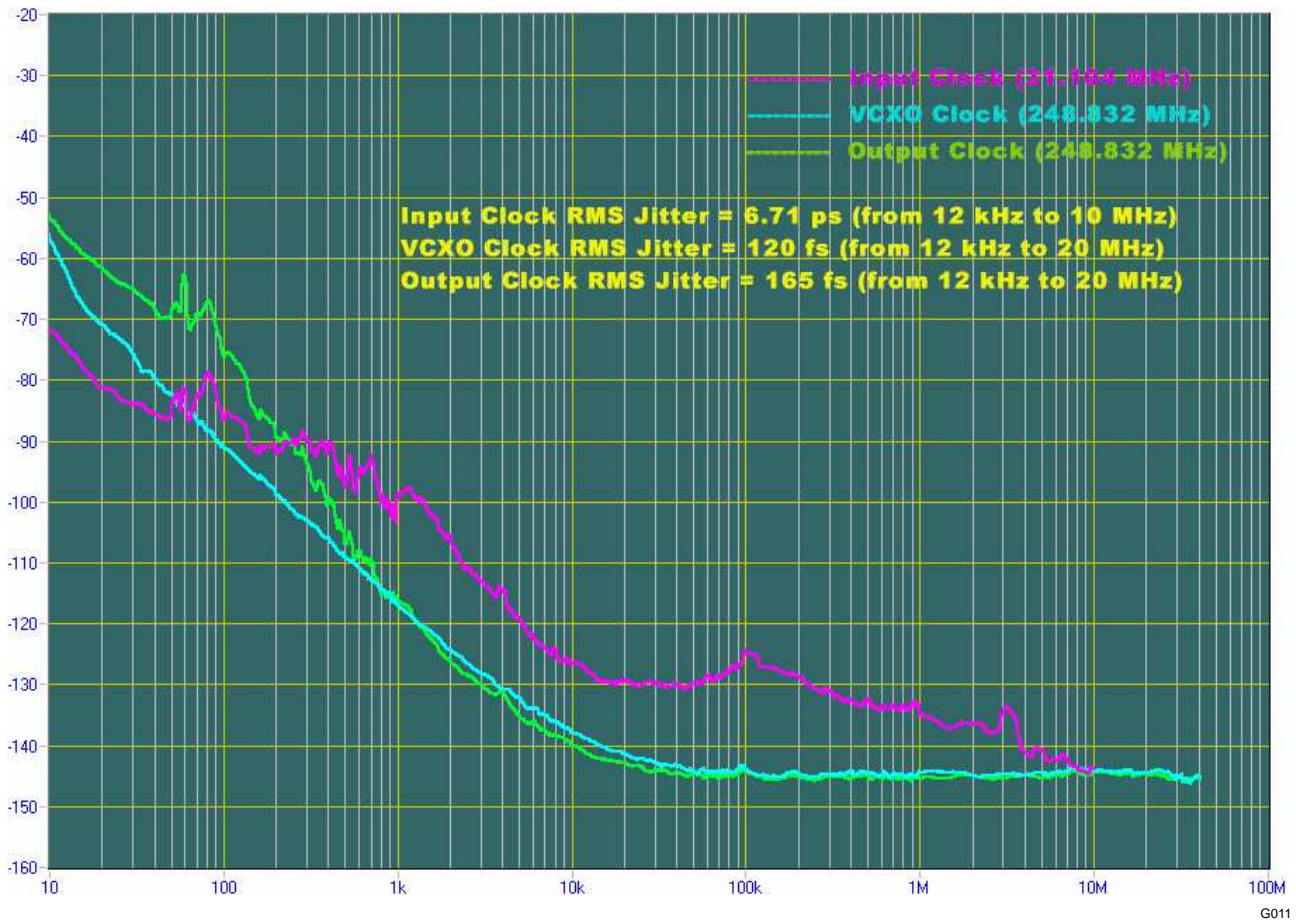


Figure 13. Phase-Noise Performance of the 248.832-MHz Output Clock From the CDC7005

Note:

The output clock is eight times the multiplied version of the input clock frequency with low jitter.

To compare input and output phase-noise plots, the reference clock plot must be raised by 18 dB (20 log 8).

3.12 Phase-Noise Performance of the CDC7005 With Toyocom 491.52-MHz VCXO

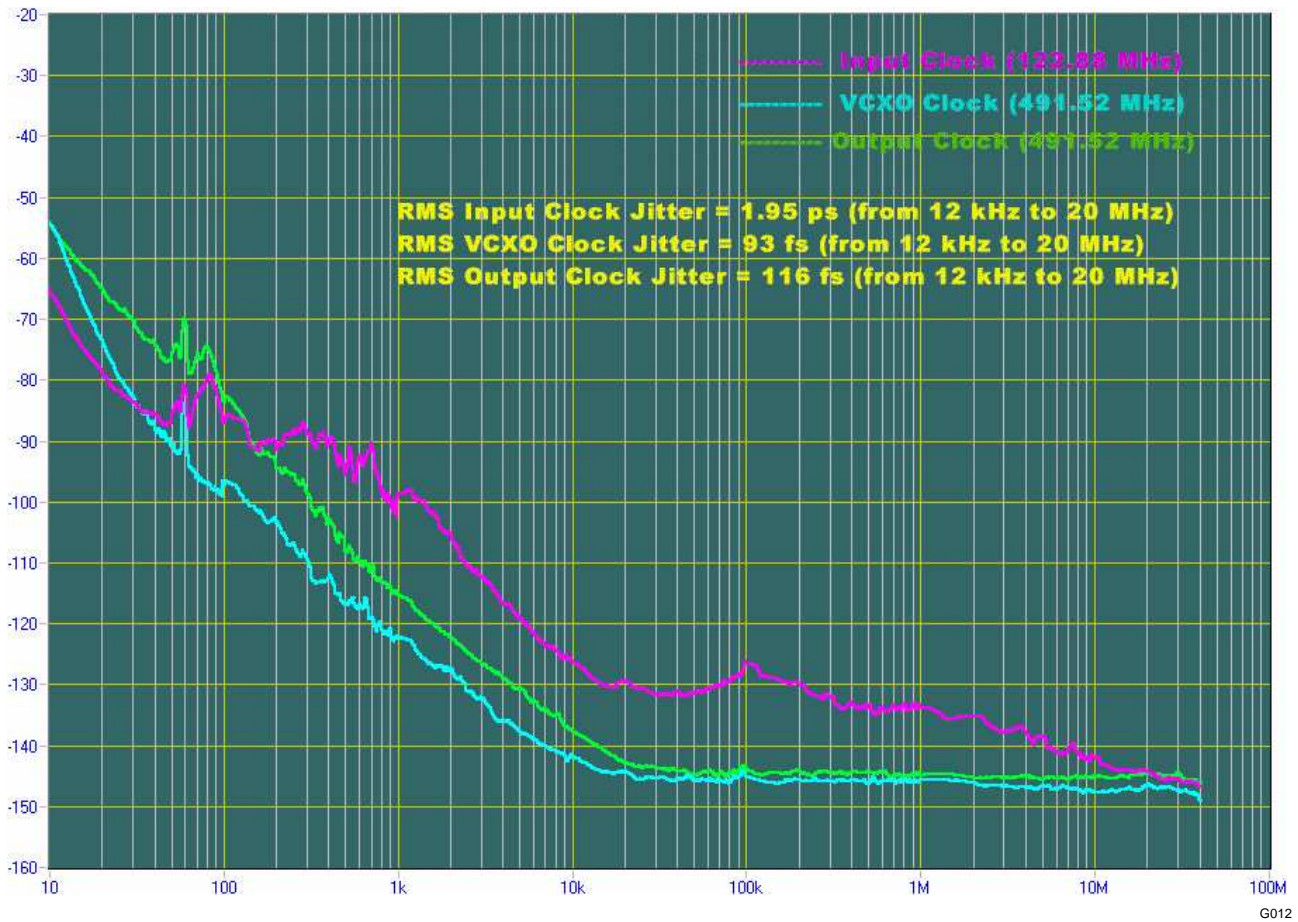


Figure 14. Phase-Noise Performance of the 491.52-MHz Output Clock From the CDC7005

Note:

The output is four times the multiplied version of the input clock frequency with low jitter.

To compare input and output phase-noise plots, the reference clock plot must be raised by 12 dB (20 log 4).

3.13 Phase-Noise Performance of the CDC7005 With Connor Winfield 622.08-MHz VCXO

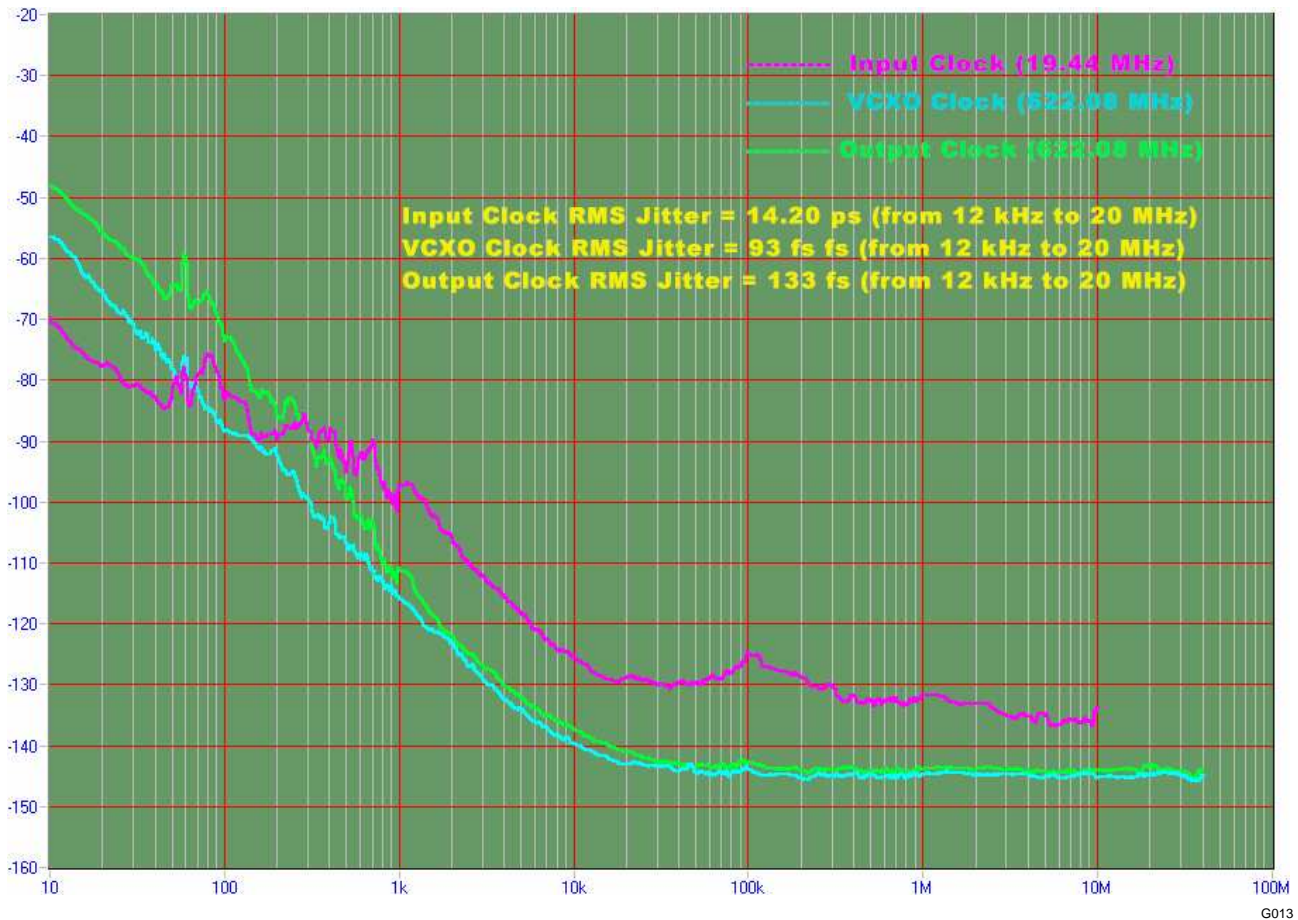


Figure 15. Phase-Noise Performance of the 622.08-MHz Output Clock From the CDC7005

Note:

The output is 32 times the multiplied version of the input clock frequency with low jitter. The output clock can easily meet the SONNET specifications.

To compare input and output phase-noise plots, the reference clock plot must be raised by 30 dB (20 log 32).

4 Conclusion

As a PLL, the CDC7005 follows the VCO (here VCXO) phase-noise floor at frequencies above the loop bandwidth. The VCXO phase-noise performance is critical to achieve good noise performance and meet the system requirements.

The rms jitter was measured from the phase-noise plot over a high-frequency band, as this is important to system performance.

From the preceding data, it is clear that a low-phase-noise clock output is easily achievable from the CDC7005 with the proper VCXO selection.

5 Acknowledgements

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1. Jimmy Hughes (JimH@JimHughesCo.com), Jimmy Hughes Co. (Pletronics VCXO)
2. Rick Kimball (rick@rfkimball.com), R. F. Kimball Company. (Vectron VCXO)
3. Robert Schrage (rs.quartz@toyocom.com), Toyocom USA
4. Sergei Jefremow (jefremow@toyocom.de), Toyocom Europe GmbH. (Toyocom VCXO)
5. Richard Sutliff (rsutliff@conwin.com), Connor Winfield (Connor Winfield VCXO)

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