Application Examples for the CDCUx877x PLL Family

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ABSTRACT

This application report provides examples of how to use the PLLs of the CDCUx877x family.

The CDCUx877x PLLs are designed for use on the DDR2 Registered Dual Inline Memory Modules (RDIMM). A differential input clock is required. The PLLs distributes 10 differential clock outputs to DDR2 DRAMs or Registers.

This report provides information on the use of the PLL as zero delay buffer, as a simple 1:10 buffer, and on how to handle the differential output signal if only a single-ended clock signal is needed.

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1 Application as Zero-Delay-Buffer

The CDCUx877x PLL family is used as a zero-delay-clock buffer on RDIMM modules.

It receives a differential clock from a Memory Controller, and distributes 10 differential clock outputs to 9, 18, or 32 DRAMs and 1, 2, or 4 Registers. In custom designs, any other combination is possible. This principle use is shown in Figure 1.

To get a Zero delay buffer, the delay of all the differential clock outputs (to DRAMs and Registers) and the delay of the Feedback path must be matched. If this is the case, there is ZERO DELAY between Point 1), 2), 3) and 4) in Figure 1. Then, the clock signals at these points have the same phase.

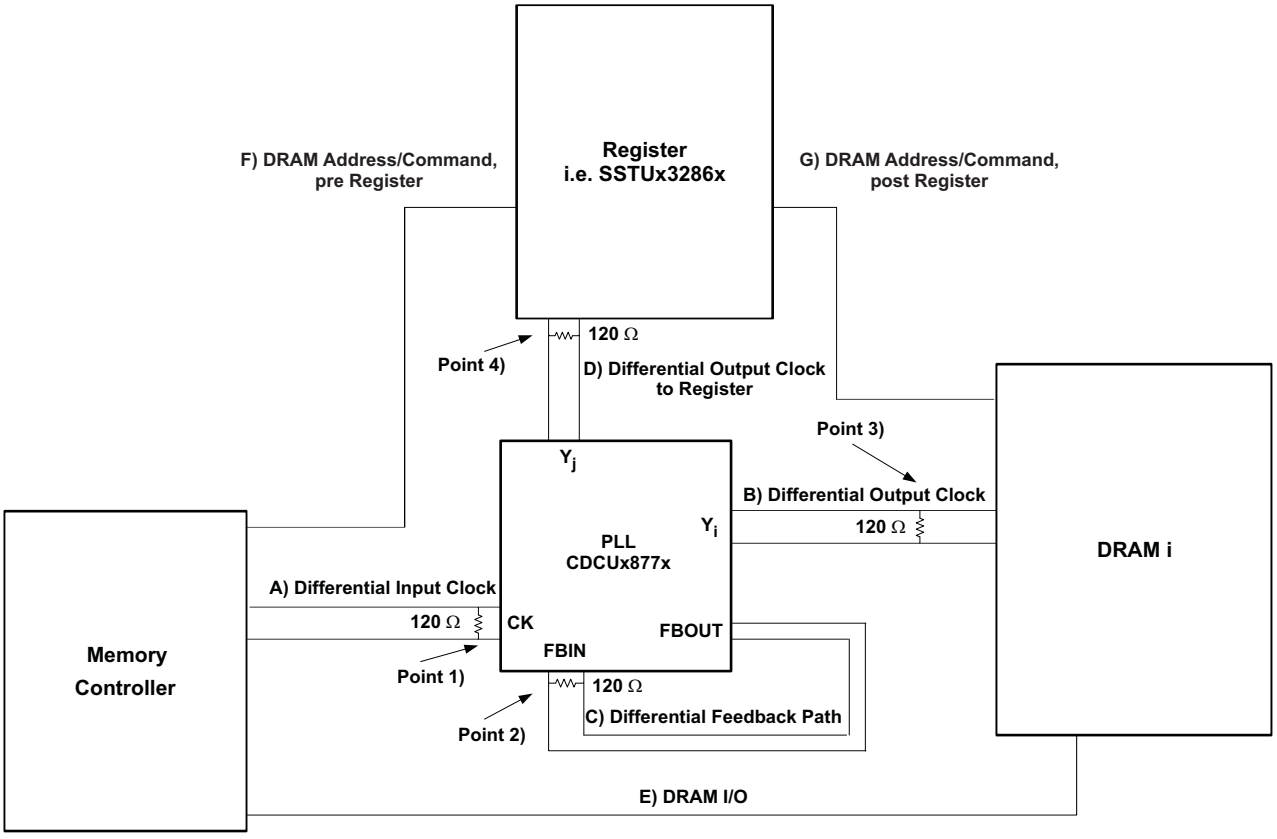
To avoid violating the setup and hold timings at the register inputs, the delay of the differential input clock (A in Figure 1) and the pre register Address/Command signals (F in Figure 1) must also be matched.

Note: Align the delay of different signals by aligning the trace length or/and using tuning capacitors.

CAUTION

When using the PLL as zero delay buffer, the user must take care that the delays of the following Signals from Figure 1 are matched:

B = C (= D) and **A = F**



Note: Clock at Points 1), 2), 3) and 4) have the same phase.

Figure 1. Principle Use of the CDCUx877x PLL on RDIMM Modules

2 Application as 1:10 Clock Buffer

When AVDD is tied to GND, the PLL is in bypass mode. Now, it behaves like a differential 1:10 clock Buffer (see Figure 2).

CAUTION

When using the CDCUx877x as a 1:10 Buffer, the parameters specified in the data sheet are no longer valid. In this mode, the PLL is turned off, so the user has no jitter cleaning or lock functionality.

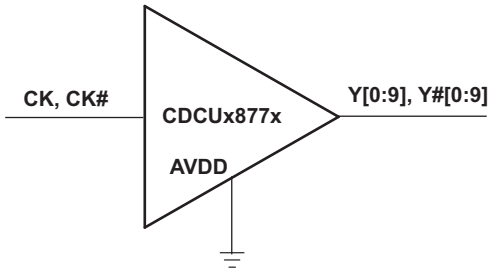


Figure 2. The CDCUx877x Used as 1:10 Clock Buffer

3 Switching Into Bypass Mode

To switch into bypass mode during operation, a circuit like the one shown in Figure 3 is recommended. For this example an analog SPDT switch TS5A6542 is used.

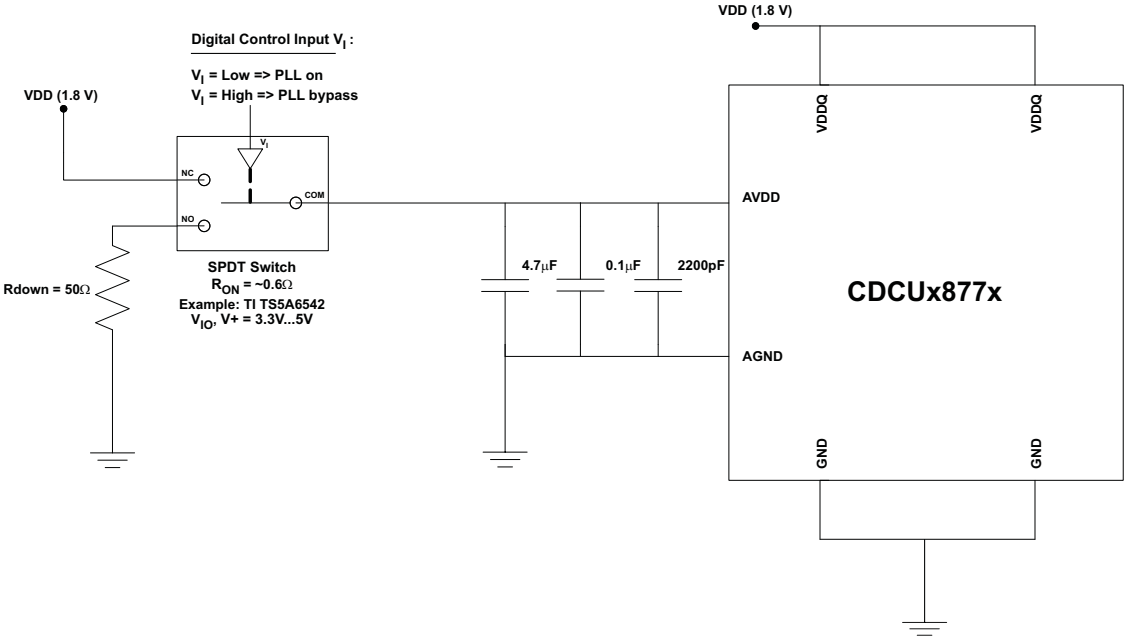


Figure 3. Example Circuit for Switching PLL Into Bypass Mode

4 Using Differential Outputs for Single Ended Inputs

The output stages of the CDCUx877x PLLs are designed for differential use. However, to drive a single-ended clock input, use of a load as shown in Figure 4 is recommended. Terminate the differential Signal with 120 Ω (if the trace impedance is 60 Ω), and connect one side of the termination to the single-ended input. Connect the other end of the termination to a dummy load. This should be a R/C load that equals the load of the input stage. If the R value of the input stage load is not known, use only a capacitor for the dummy load.

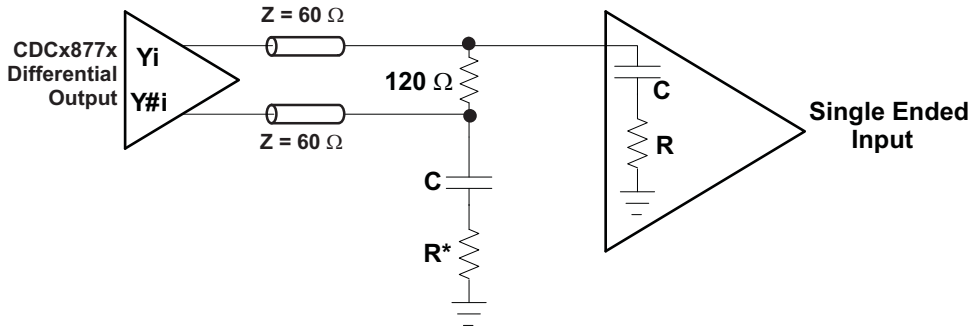


Figure 4. Example Termination for Differential Signal That Drives a Single-Ended Input Stage

5 References

1. *CDCU877/A 1.8V Phase-Lock Loop Clock Driver for DDR2 SDRAM Applications*, Data sheet (SCAS688)
2. *CDCU877B 1.8V Phase-Lock Loop Clock Driver for DDR2 SDRAM Applications*, Data sheet (SCAS801)
3. *CDCUA877 1.8V Phase-Lock Loop Clock Driver for DDR2 SDRAM Applications*, Data sheet (SCAS769)
4. *CDCU2A877 1.8V Phase-Lock Loop Clock Driver for DDR2 SDRAM Applications*, Data sheet (SCAS827)
5. JEDEC Solid State Technology Association, Registered DIMM Design Specification (JESD21)
6. TS5A6542 SPDT Analog Switch With Input Logic Translation, Data sheet (SCDS211)

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