

# Improving Analog Input Modules Reliability Using Fault Protected Multiplexers



## ABSTRACT

Programmable Logic Controllers (PLC's) are widespread in many industrial applications. Industrial applications can be operated in harsh environments that could potentially expose to the front end of the system, the Analog Input Module (AI), to damaging fault conditions. Fault Protected Switches and Multiplexers can be implemented to provide the system with protection without much cost to overall system performance thereby increasing the systems reliability. This report will cover potential fault conditions on PLC AIO's, then look how TI's Fault Protected Switches and Multiplexers can protect against these faults, and finally look into how to implement one of TI's Fault Protected Switches or Multiplexers successfully into a system.

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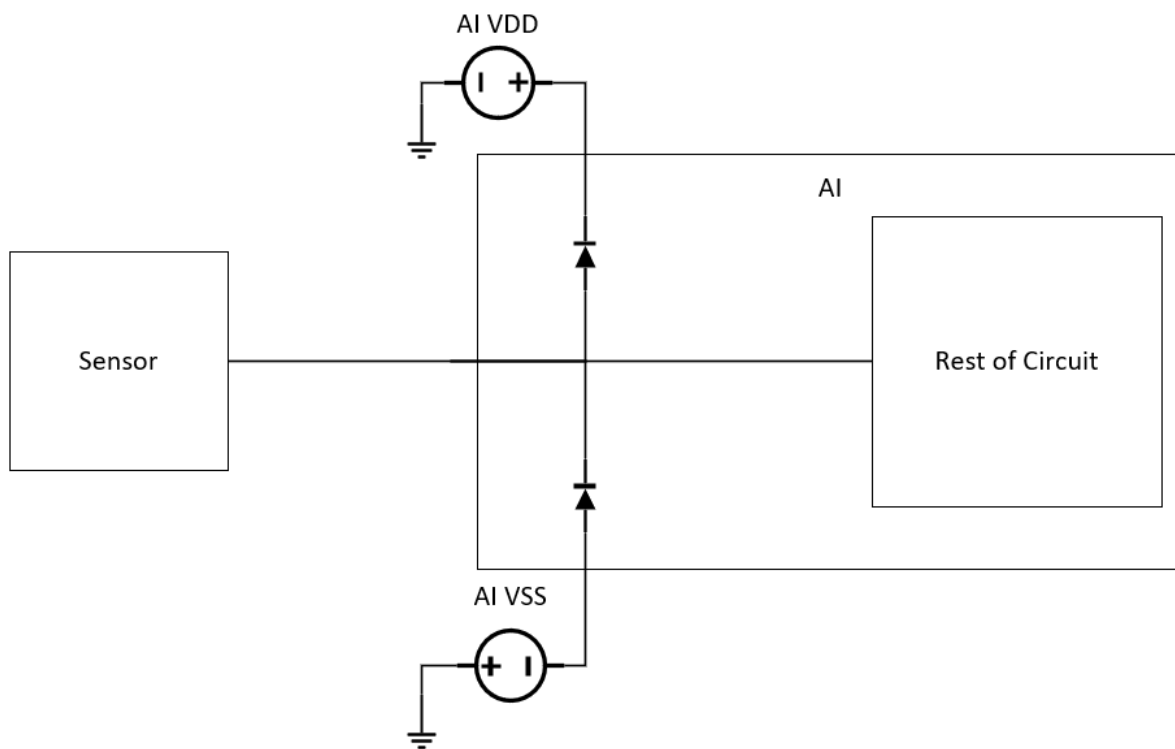
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## 1 Potential Fault Conditions on PLC Analog Input Modules

A list of common, but not exhaustive, fault conditions on the AI Module can be broken down into two broad categories: voltage Electrical Overstress and Latch Up failures. Electrical Overstress can be broken down into four general categories: voltage transients that cause input voltages to go above or below supply rails of the system; an input signal appearing before the system is powered; ground shifting currents which can cause the system to see input voltages beyond supply rails due to differences in ground potential; mis-wiring can cause unexpected voltage rails and/or signal inputs to appear at the front end of the system which could cause inputs being beyond the power rails. While Electrical Overstress and Latch-Up do have some commonalities between them; these events will be examined individually.

The first case to examine is that of Electrical Overstress – focusing on transient signals causing either an undervoltage event or overvoltage event. The causes of voltage transients vary, but transients are common in harsh industrial environments. If the input system includes ESD diodes, example shown in [Figure 1-1](#), a voltage transient can cause one of the diodes to become forward biased if the voltage drop across the diode is less than or equal to the diode's voltage threshold.



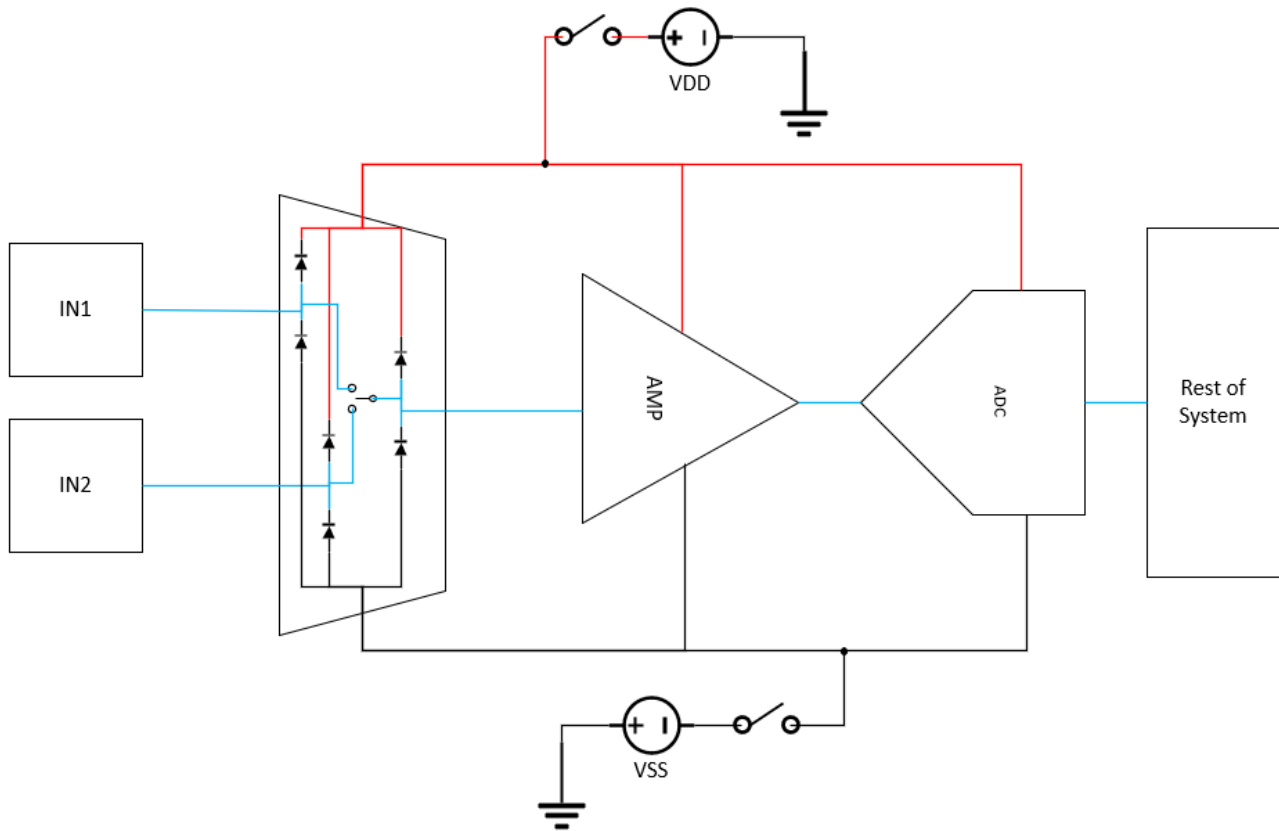
**Figure 1-1. Generalized Analog Input Module with Input ESD Diodes Shown**

After the diode becomes forward biased, the current through the diode is given by the Shockley Equation shown in [Equation 1](#)

$$I_d(V_D) = I_S \left( e^{\frac{V_D}{nV_T}} - 1 \right) \quad (1)$$

where  $I_S$  is the saturation current of the diode,  $V_D$  is the voltage drop across the diode,  $n$  is the emission coefficient, and  $V_T$  is the thermal voltage. The ESD diodes are not designed to handle large sustained currents and with the large currents possible when the voltage ratings are exceeded these diodes are apt to be damaged. When these diodes are damaged they will short either VDD or VSS to the input line depending on the polarity of the transient event.

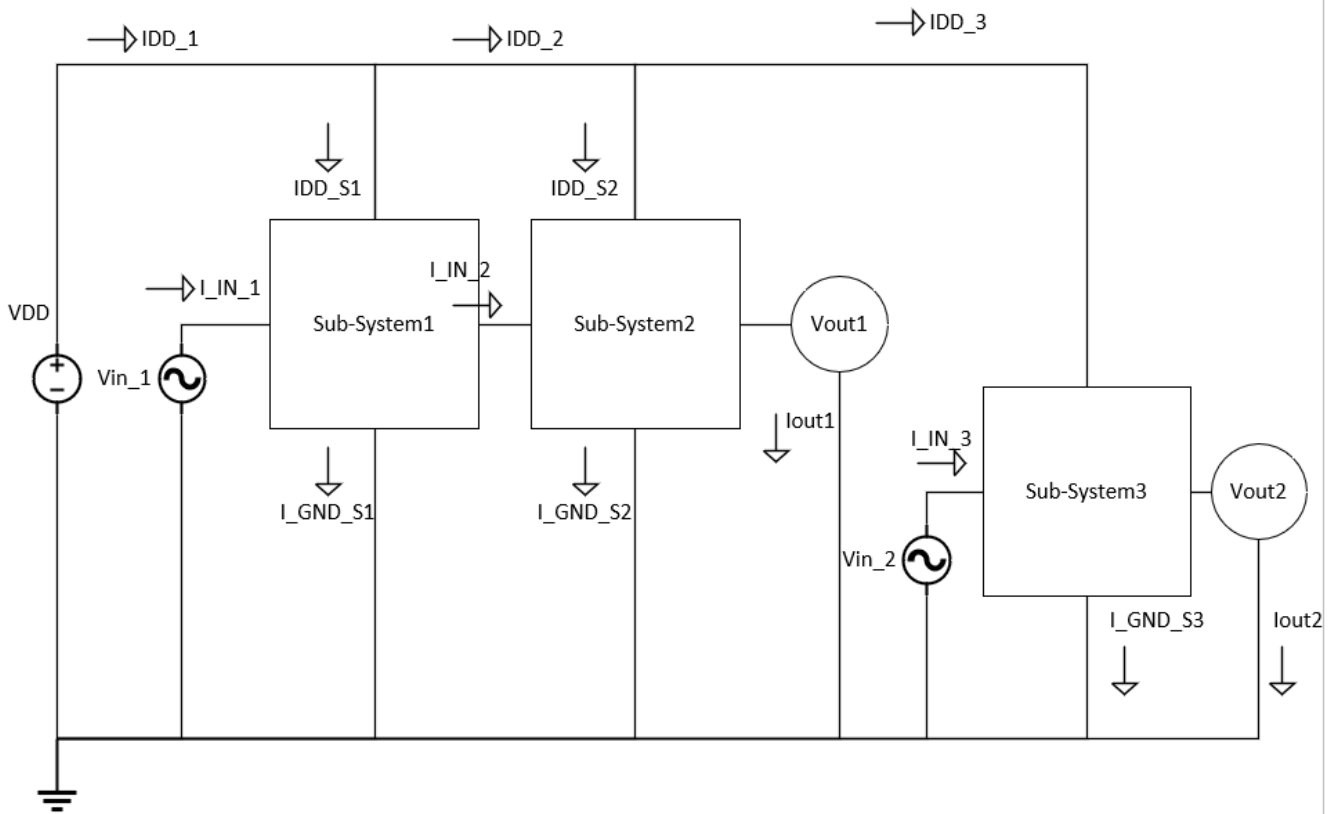
The next issue that deals with electrical overstress on the system is the case when a signal appears on the input when the system is unpowered. In systems with traditional ESD structures, the input signal wouldn't have to be that large to cause a diode to become forward biased. While the same issues apply as mentioned with voltage transients during operation – another issue that could show up is that of back-powering. Not only are the ESD diodes subject to damage but the input signal could potentially feed back to any other device on that power rail causing systems to become active prematurely and/or damage systems from having incorrect supplies on more sensitive components. [Figure 1-2](#) shows a simplified analog input module with 2 input sources, a 2:1 multiplexer, an amplifier, and an ADC. The system is unpowered. The red lines represent VDD connections, blue lines for signal pathway, and black lines for VSS connections.



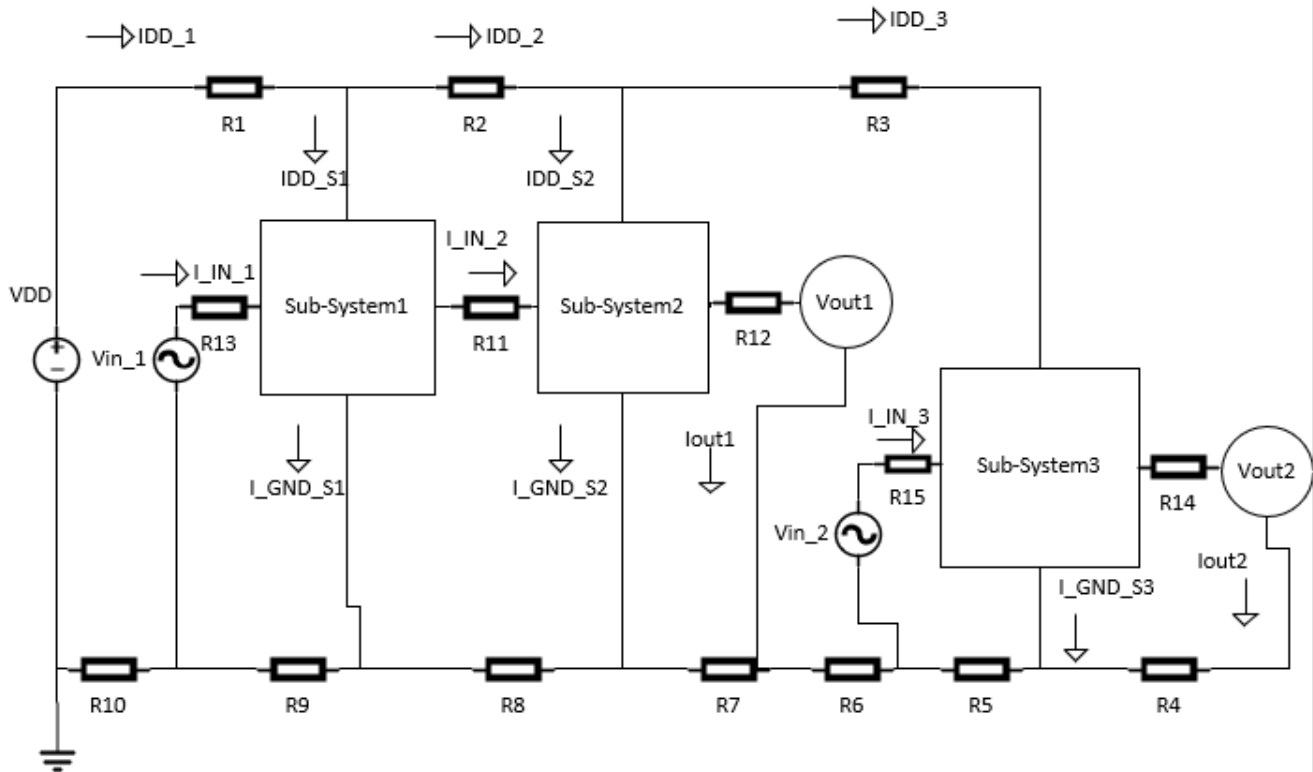
**Figure 1-2. Simplified ASC for Analog Input Module with Front End Multiplexer that has ESD Diode Connections to Power Rails**

For a quick example, assume the system power is off, the diodes have a threshold voltage of 0.5 V, IN1 has a signal of 5 V, and IN2 has a signal of -6V . This will cause the diodes from VDD to IN1 to become forward biased while creating a VDD voltage of 4.5 V (input – diode drop). While the diodes on the second input will be forward biased from VSS to IN2 and creating a VSS voltage of -4.5 V (input + diode drop). Now both the amp and ADC have voltages on their power rails, which can cause unexpected operation and potential damage.

The next issue, ground shifting, is a bit more complex. In PLC systems many different components are going to be directly connected via a ground pin or indirectly for devices with no ground pin as the devices power supplies are still referenced to a ground node. With many potential devices return current pathway emptying into this node, ground reference points can be shifted causing different ground nodes to be at different voltages w.r.t. to the input power's ground connection. The reason why this happens can be explained by looking at the ideal case of a system – see [Figure 1-3](#) – versus the real version of the system – see [Figure 1-4](#).



**Figure 1-3. Ideal Generalized System Diagram**



**Figure 1-4. Generalized System Diagram with Trace Resistance Shown**

From the previous two images it can be shown that the ideal case (Figure 1-3) has no impedance between different ground connections. This is not technically true due to the fact that even the low impedance ground trace / ground plane still is not 0 ohms, but it is low. However, in certain industrial and automotive applications this small impedance in the ground plane starts to make a difference. If the return current running through ground is high enough, the ground connection points can be lifted above ground. For example, imagine Iout2 is 3 A and all the other currents are << 3 A and all the resistances are equal to 0.2 Ohms. This will create ground references that are not equal to zero volts with respect to the system ground which can cause input signals to be outside of the operating range of the device which can lead to system damage. Table 1-1 shows the new ground potentials with the above example.

**Table 1-1. Reference Potential's During Ground Shift w.r.t. Power Ground**

| Device / Source | Ground Potential (w.r.t. VDD's Ground) |
|-----------------|--|
| VDD             | 0 V                                    |
| Vin_1           | 0.6 V                                  |
| Sub-System1     | 1.2 V                                  |
| Sub-System2     | 1.8 V                                  |
| Vout1           | 2.4 V                                  |
| Vin_2           | 3.0 V                                  |
| Sub-System3     | 3.6 V                                  |
| Vout2           | 4.2 V                                  |

At first glance this may not seem like a large problem, but these shifts can cause the subsystems to become out of spec. Assume that VDD = Vin\_1 = Vin\_2 = 44V, and look to Table 1-1, Table 1-2, Table 1-3, and Table 1-4 to see the issues that are possible from ground shifting, for simplicity the output voltages have been ignored for this specific example. All voltages shown are with respect to system ground, which is located at the negative terminal of VDD in this example.

**Table 1-2. New Input Voltage Ranges During Ground Shift w.r.t. Power Ground**

| Device/Source | Nominal Voltage | Ground Shift | New Max | New Ground |
|---------------|-----------------|--------------|---------|------------|
| VDD           | 44 V            | 0 V          | 44 V    | 0 V        |
| Vin_1         | 44 V            | 0.6 V        | 44.6 V  | 0.6 V      |
| Vin_2         | 44 V            | 3.0 V        | 47 V    | 3.0 V      |

**Table 1-3. New Voltage Ranges for Sub-Systems During Ground Shift w.r.t. Power Ground**

| Sub-System  | Upper Limit | Lower Limit After Ground Shift |
|-------------|-------------|--------------------------------|
| Sub-System1 | 44 V        | 1.2 V                          |
| Sub-System2 | 44 V        | 1.8 V                          |
| Sub-System3 | 44 V        | 3.6 V                          |

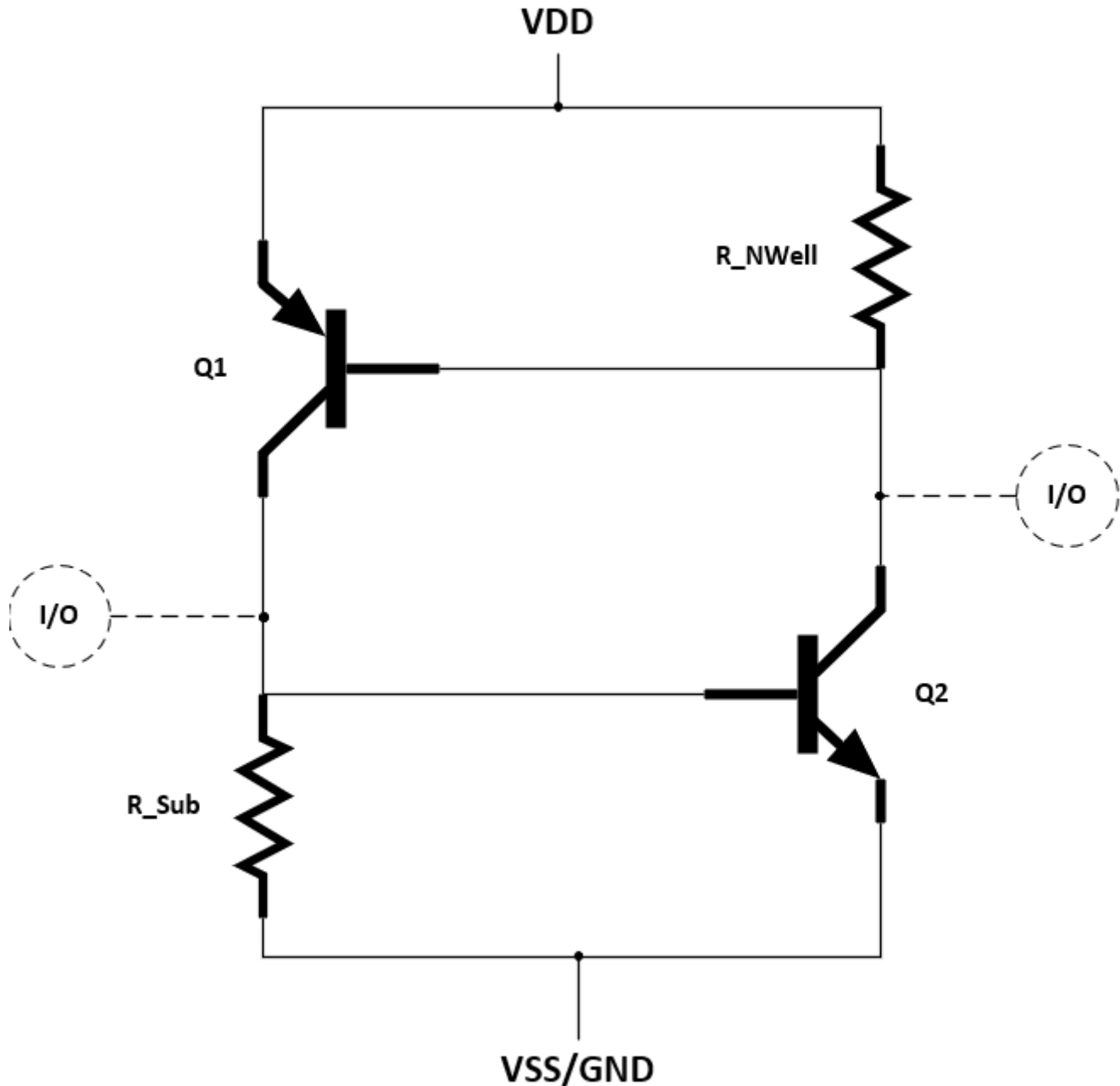
**Table 1-4. Electrical Overstress Due to Ground Shift Matrix**

|       | Sub-System1 Undervoltage | Sub-System1 Overvoltage | Sub-System2 Undervoltage | Sub-System2 Overvoltage | Sub-System3 Undervoltage | Sub-System3 Overvoltage |
|-------|--------------------------|-------------------------|--------------------------|-------------------------|--------------------------|-------------------------|
| Vin_1 | Yes<br>0.6 V < 1.2 V     | Yes<br>44.6 V > 44 V    | Yes<br>0.6 V < 1.8 V     | Yes<br>44.6 V > 44 V    | No<br>No Connection      | No<br>No Connection     |
| Vin_2 | No<br>No Connection      | No<br>No Connection     | No<br>No Connection      | No<br>No Connection     | Yes<br>3 V < 3.6 V       | Yes<br>47 V > 44 V      |

From the previous tables it is shown that the Sub-Systems don't have an increase in the max voltage that can be accepted but the lowest signal accepted has increased in value. Now when Vin\_1 hits its max or min voltage Sub-System1 and potentially Sub-System2 are going to experience overvoltage and/or undervoltage events. The same can be seen with Vin\_2 and Sub-System3. During events where a large ground shift is possible the signal chain can experience electrical overstress and therefore erroneous results and/or system damage.

The final broad category of electrical overstress has to deal with miswiring. When the input of a system is miswired the biggest concern is potential electrical overstress. This can occur due to connecting a power supply to an input, or connecting an input to a pin/port that isn't able to handle the prescribed voltage. These human mistakes when prepping systems can cause electrical overstress which ultimately can damage/destroy the system.

While the other issues all dealt directly with electrical overstress there is one more outlier than can be disastrous for system designers – this is CMOS Latch Up. Latch up failures occur when VDD is shunted to VSS/GND and the issue doesn't resolve until the power is cycled or system failure occurs. The cause of latch up is a parasitic silicon-controlled rectifier (SCR) that exists in traditional CMOS manufacturing processes. The SCR is shown in Figure 1-5 – analyzing this circuit gives intuition on how failure occurs.



**Figure 1-5. Parasitic SCR Equivalent Circuit**

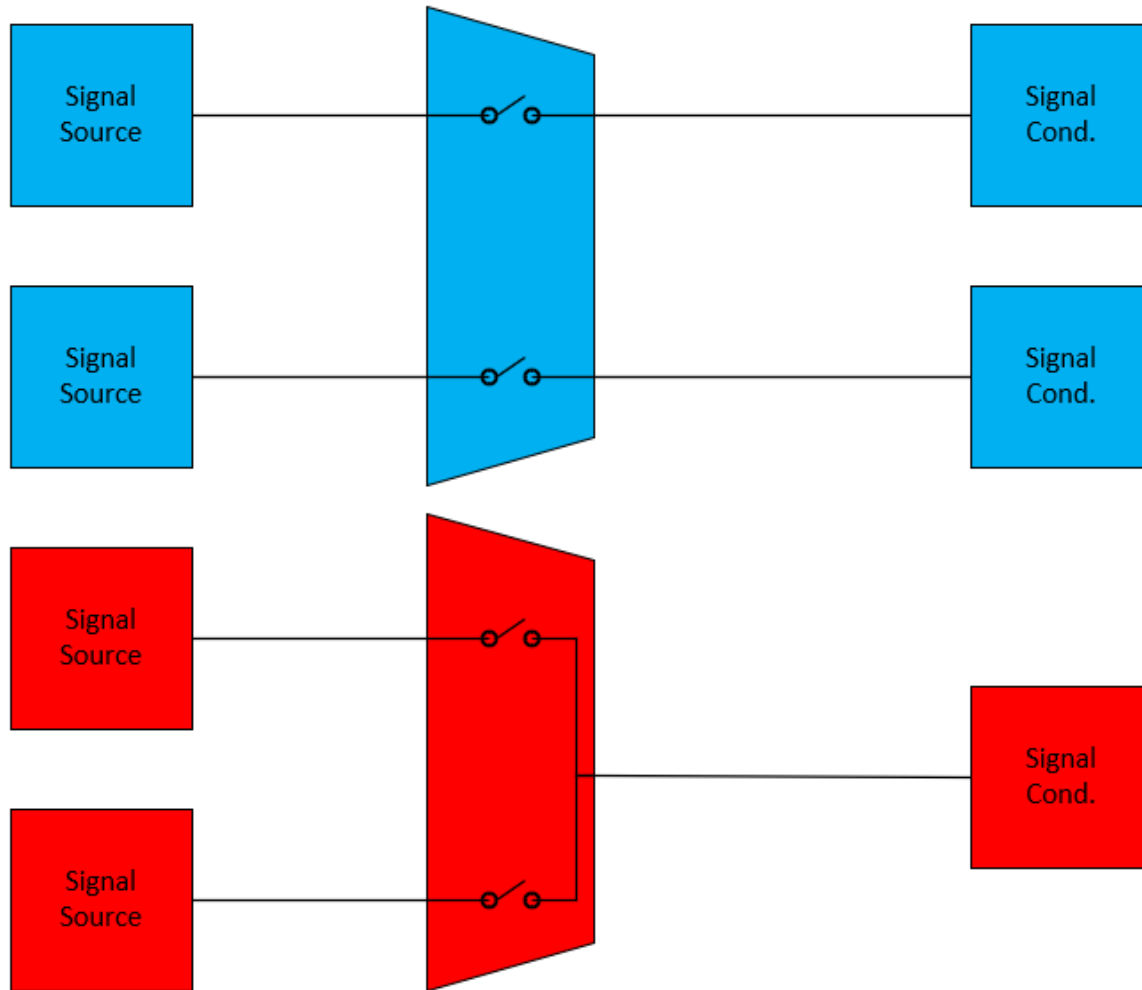
Examining the SCR, two potential fail scenarios are shown – an injected current or a signal that is greater than VDD or less VSS/GND will cause the BJT's to conduct. However, there is one other and that is a fast transient can also cause the BJT's to conduct and trigger a latch-up event – these are often referred to as transient induced latch-up. This poses a serious risk to the system. If any of the three main causes of latch up exist on the input of a system that is vulnerable to latch-up events the device will shunt VDD to VSS/GND. This process will not only potentially damage the IC experiencing the latch-up, but can cause the power rails to sag potentially damaging more sensitive components on the signal chain.

These fail categories provide an insight to failure mechanisms of Analog Input Systems used in a PLC. These issues must be overcome to have reliable and accurate operation of the PLC which is critical in industrial applications. In the past this has been done in a variety of ways including discrete components; however, in many situations the most optimal solution for cost, solution size, and performance is to integrate protection features into the first elements of the analog input system – the analog switch/multiplexer.

## 2 How Does a Fault Protected Multiplexer Protect the System

In the first section of this report some common issues are discussed that plague designers when they are designing Analog Input Modules for PLC's. This section will delve into a potential solution for the protection needs of the Analog Input Module – Fault Protected Switches/Multiplexers from TI. To understand the benefits of using a Fault Protected Switch/Multiplexer in a system's Analog Input Module each of the aforementioned problems will be compared to TI's Fault Protected Switch/Multiplexers features to see how these devices will be able to protect the system from possible fault conditions.

The Fault Protected Multiplexer or Switch is implemented into an Analog Input Module by placing the IC between the signal input, such as a sensor or external connector, and the signal conditioning/ signal processing blocks. The Switch/Mux IC can either connect one input to one signal conditioning block or connect multiple inputs into the same signal conditioning block. This is shown in [Figure 2-1](#) where the blue diagram shows a multi-channel 1:1 switch and the red diagram shows a single channel 2:1 multiplexer as an example of how the signal chain + mux/switch look in general.



**Figure 2-1. Generalized Analog Input Module With Switch/Multiplexer**



Using the basic architecture from [Figure 2-1](#) the fault conditions can be analyzed. The first fault condition that will be examined is the case where there is a generalized voltage transient on the input of the analog input module. The transient is characterized by voltages that exceed the rated input range with either an undervoltage or overvoltage event. TI's Fault Protected Switches and Multiplexers are built with voltage protection for both over and under voltage events. For example, the TMUX7308F, an 8:1 multiplexer, has the following specifications, with fault protection features bolded:

- +/-5 V to +/-22 V Dual Supplies
- 8 V to 44 V Single Supply
- Passes Rail to Rail Signals
- 8:1 Multiplexer
- **Latch-Up Immune**
- **+/- 60 V Voltage Protection Under Powered Off Conditions**
- **+/- 60 V Voltage Protection w.r.t. Ground**
- **+/- 85 V Voltage Protection from Source to Supply**
- **+/- 85 V Voltage Protection from Source to Drain**
- **Non-Fault Channels Will Operate Normally**

The five fault protection characteristics are shared by many faults protected multiplexers – although actual rating may change – so be sure to verify with the specific devices' data sheet. Each of these specs are important in understanding max ratings for the device in a specific use case.

With respect to the fault condition of a generalized transient event – this fault specifically is dealing with overvoltage and undervoltage protection. For Fault Protected Switches and Multiplexers there are three ratings to pay attention to. The first is voltage rating with respect to ground and the second is voltage rating from source to supply/ source to drain. For the ratings there is a simple process that you can do to calculate the protection boundaries with these two specs.

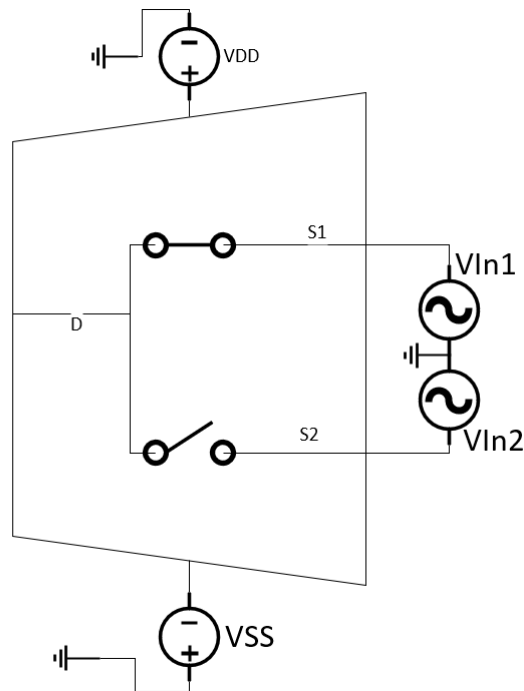
Find Minimum Voltage with [Equation 2](#).

$$f(VDD) = \begin{cases} -60V, & VDD - 85V < -60V \\ VDD - 85V, & VDD - 85V \geq -60V \end{cases} \quad (2)$$

Then the maximum can be found in a similar way as shown in [Equation 3](#).

$$f(VSS) = \begin{cases} 60V, & VSS + 85V > 60V \\ VSS + 85V, & VSS + 85V \leq 60V \end{cases} \quad (3)$$

This will give a good idea of overall bounds of protection for the part – however, there is one more condition that needs to be understood which is the Source to Drain voltage measurement. A simplified example is shown in [Figure 2-2](#).



**Figure 2-2. Multiplexer with Two Inputs (S1 Closed, S2 Opened)**

For this 2:1 multiplexer there are a few things to note – the source pins (S1, S2) are connected to Vin1 and Vin2 respectively. The supplies are VDD and VSS. The drain pin is D and is connected to S1 which means that the voltage at the drain and S1 are the same. This puts a limit on the voltage that can be on S2 as the +/-85V spec applies from source to drain as well. Using Equation 4, will determine whether or not there will be an issue:

$$f(V_{Source}, V_{Drain}) = \begin{cases} In\ Spec, & |V_{Drain} - V_{SourceN}| \leq 85V \\ Out\ of\ Spec, & |V_{Drain} - V_{SourceN}| > 85V \end{cases} \quad (4)$$

As a quick recap of the information a couple quick examples can be shown to help build understanding.

**Example 2.1** What are the protection bounds when VDD = 20V and VSS = -10V?

Using Equation 5

$$f(VDD = 20V) \rightarrow 20V - 85V = -65V < -60V \rightarrow Min = -60V \quad (5)$$

Using Equation 6

$$f(VSS = -10V) \rightarrow -10V + 85V = 75V > 60V \rightarrow Max = 60V \quad (6)$$

In example 2.1 the min and max bounds for the protection circuitry on the IC is **-60V to 60V**.

**Example 2.2** What are the protection bounds when VDD = 30V and VSS = -5V?

Using Equation 7

$$f(VDD = 30V) \rightarrow 30V - 85V = -55V > -60V \rightarrow Min = -55V \quad (7)$$

Using [Equation 8](#)

$$f(V_{SS} = -5V) \rightarrow -5V + 85V = 80V > 60V \rightarrow Max = 60V \quad (8)$$

In example 2.2 the min and max bounds for the protection circuitry on the IC is **-55V to 60V**.

**Example 2.3** Using Figure 2.2 as reference what are the bounds on Vin2 (V\_Source2) when VDD = 40V, VSS = 0V and Vin1 (V\_Source1) = 35V.

Using [Equation 2](#)

$$f(V_{DD} = 40V) \rightarrow 40V - 85V = -45V > -60V \rightarrow Min = -45V \quad (9)$$

Using [Equation 10](#)

$$f(V_{SS} = 0V) \rightarrow 0 + 85V = 85V > 60V \rightarrow Max = 60V \quad (10)$$

When in spec the following equation is valid because  $V_{Source1}$  is connected to the output.:

$$V_{Drain} = V_{Source1} = 35V \quad (11)$$

Using [Equation 12](#) to solve for  $V_{Source2}$  yields the following two equations:

$$\begin{aligned} V_{Drain} - V_{Source2} &= -85V \rightarrow 35V - V_{Source2} = -85V \rightarrow V_{Source2} = 85V + 35V = 120V \\ V_{Drain} - V_{Source2} &= 85V \rightarrow 35V - V_{Source2} = 85V \rightarrow V_{Source2} = 35V - 85V = -50V \end{aligned} \quad (12)$$

This gives a preliminary range of Vin2 to be from **-50V to 120V**. However, since the device has other limits on min and max inputs this range will be shrunk down to **-45V to 60V** to keep in line with the other device specifications.

These examples show that TI's Fault Protected Switches and Multiplexers can handle a wide range of over/under voltages that can change based on a few designer choices. This is not the full story though. While it has been shown how to calculate protection boundaries, the next step to discuss is how and when these devices react. This comes down to three simple concepts: fault levels, fault thresholds, and output state during fault. Fault levels are set in two ways depending on device. If the device has a VFN and VFP pin, the fault levels can be set by placing supplies between these pins and ground such as with the TMUX7462F (4 channel, 1:1 channel protector which has its switches closed unless  $V_{DD} = 0V$  or a fault condition is detected). If the device does not have VFN and VFP pins the fault levels are set to VDD and VSS voltages as is the case with devices like the TMUX7308F. These devices will not react until the input signal is either above or below a set fault level by a threshold voltage  $V_t$  (typically  $\sim 0.7V$ ). When a fault level has been exceeded by the threshold voltage or more the device will react. How it reacts depends on device. Some devices such as the TMUX7308F will disconnect the fault channel and "open" the output and provide no overshoot on the output – a block diagram of this concept can be seen in [Figure 2-3](#) and an oscilloscope capture of the output of the TMUX7308F is shown in [Figure 2-4](#).

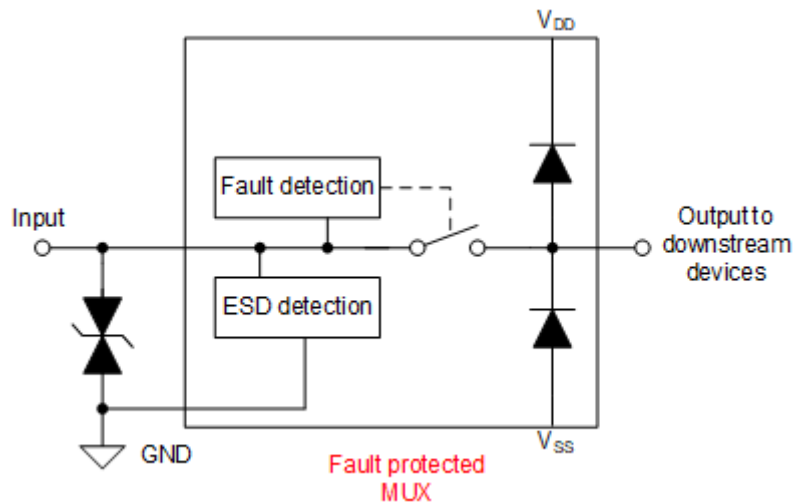
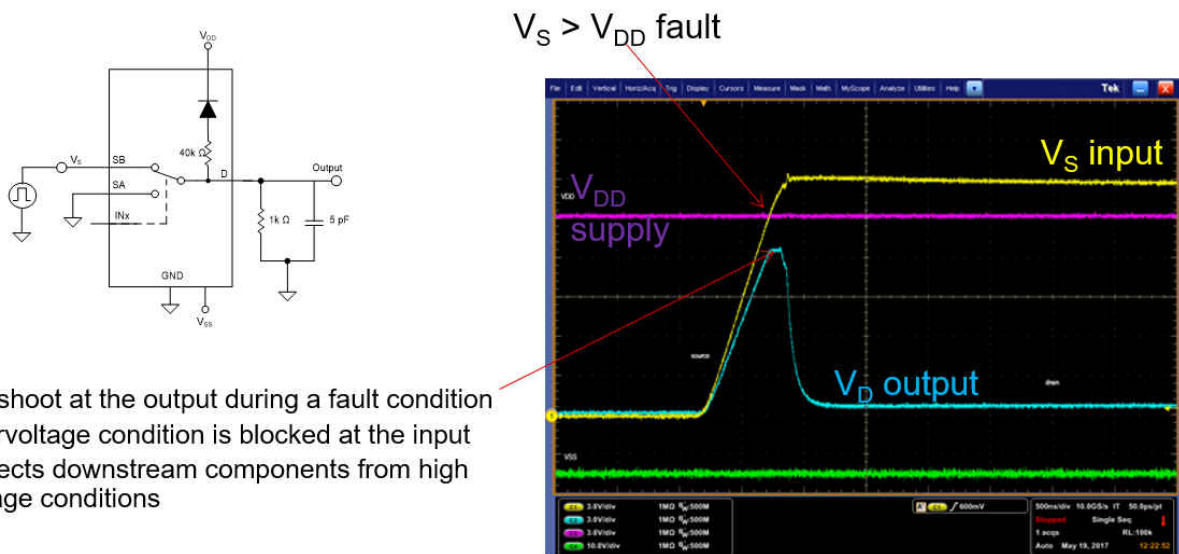


Figure 2-3. TI Fault Protected Multiplexer, Open when Fault Occurs Shown



- No overshoot at the output during a fault condition
  - Overvoltage condition is blocked at the input
  - Protects downstream components from high voltage conditions

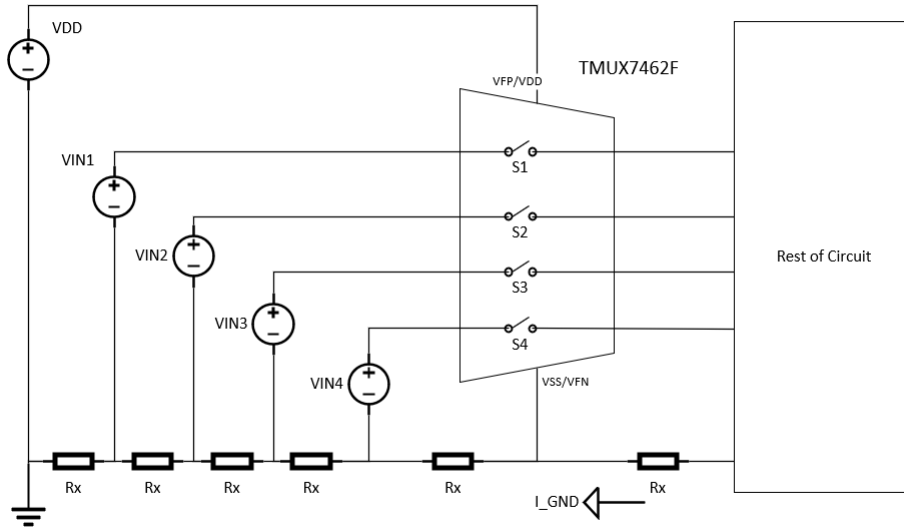
Figure 2-4. No Overshoot on Output When Fault Detected

However, some devices such as the TMUX7462F provide a DR pin that allows a choice of output states during a fault condition. While also being able to open the channel with a fault the device can also be used to clamp the output to the supply. These two parts match the two patterns that emerge in TI's Fault Protected Switches and Multiplexers which include the TMUX73XXF and TMUX74XXF families.

The next protection feature needed is that of protection against live signals into a system that is unpowered. This is simply a matter of getting a multiplexer/switch with powered off protection as a feature. This means the switch will be high-impedance until an active VDD is present – this will be rated within a range of voltages – for the TMUX7308F for example this is +/-60V which means that when VDD = 0V a signal of +/-60V on the input pin will not cause damage. However, there is still some leakage current that will conduct through the switch and these values can be found in the respective IC's data sheet, however there will be no current that leaks through either VDD or VSS as there is no direct connection from inputs to VSS or VDD, so there shouldn't be an issue of back-powering when using devices with powered-off protection.

Another need from a fault protected front end mux or switch is to be able to protect from overvoltage's and undervoltage's that can occur due to a shifting ground reference from excess ground current – this is also called ground shifting. An analog input system can have multiple IC's connected to the same ground, commonly referred as the system ground. Ideally these ground connections all form one node that has 0V between any

ground connection. This is not the case in reality – as there is a small impedance between ground connections. Under normal operating conditions it is generally safe to assume that these are all at the same potential – but in the case of a large ground current, these references can shift. However much in how TI’s Fault Protected Switches and Multiplexers protect against voltage transients it also protects against electrical overstress due to ground shifting. The best way to show this is with a quick example.



**Figure 2-5. TMUX7462F in Generalized Analog Input Module**

**Example 2.4:** Find the States of S1, S2, S3, and S4 in [Figure 2-5](#) with the following Parameters:  
Using the TMUX7462F as the switch with the following parameters.

$$\begin{aligned}
 V_{in1} &= 6V; V_{in2} = 16V; V_{in3} = 44V; V_{in4} = 1.5V; \\
 V_{DD} &= V_{FP} = 44V; V_{SS} = V_{FN} = 0V; V_T = 0.7V \\
 R_x &= 0.1\Omega; I_{GND} = 4A;
 \end{aligned}$$

### TMUX7462F Fault State = Open Switch When Fault Is Detected

(13)

First, the TMUX7462F’s VSS/GND voltage w.r.t. system ground voltage needs to be found. This can be done by multiplying the current  $I_{GND}$  by the series resistance between VSS/GND and the system ground. For this example,  $R_x$  is  $0.1\Omega$  and  $I_{GND}$  is assumed to be  $4A$  this leads to the equation  $5 \cdot R_x \cdot I_{GND} = 5 \cdot 0.1\Omega \cdot 4A = 2V$ . With this value the TMUX7462F’s VDD to VSS voltage can be calculated to be  $42V$  w.r.t. to system ground and can accept values between  $2V$  and  $44V$  w.r.t. system ground.

Now that VDD-VSS has been found for the TMUX7462F the ground nodes for the input voltages need to be found. Using the same process as for VSS it can be seen that  $V_{INX\_GND}$  w.r.t. GND =  $X \cdot R_x \cdot 4$ . Which result in the following:  $V_{in1\_GND} = 0.4V$ ;  $V_{in2\_GND} = 0.8V$ ;  $V_{in3\_GND} = 1.2V$ ; and  $V_{in4\_GND} = 1.6V$ . This now allows for the max and min  $V_{in}$  which has results in [Table 2-1](#).

**Table 2-1. TMUX7462F Input Voltage Ranges During Ground Shift w.r.t. Power Ground**

| Input | Max    | Min   |
|-------|--------|-------|
| VIN1  | 6.4 V  | 0.4 V |
| VIN2  | 16.8 V | 0.8 V |
| VIN3  | 45.2 V | 1.2 V |
| VIN4  | 3.1 V  | 1.6 V |

Now to figure out what each of the switch states are the fault boundaries will be tested. Using [Equation 14](#).

$$\text{Fault}(V_{in}, V_{FP}, V_{FN}, V_T) = \begin{cases} \text{Case 1: } \text{MAX}(V_{in}) - V_{FP} \geq V_T \rightarrow \text{Fault} \\ \text{Case 2: } V_{FN} - \text{MIN}(V_{in}) \geq V_T \rightarrow \text{Fault} \\ \text{Case 3: No Fault} \end{cases} \quad (14)$$

Based on the above equation the switch states are reflected in [Table 2-2](#).

**Table 2-2. TMUX7462F Switch States During Ground Shift**

| Switch | State  | Case    | Equation  |
|--------|--------|---------|---|
| S1     | Opened | 2       | $V_{FN} - \text{MIN}(V_{in}) \geq V_T \rightarrow 2V - 0.4V = 1.6V \geq 0.7V$                       |
| S2     | Opened | 2       | $V_{FN} - \text{MIN}(V_{in}) \geq V_T \rightarrow 2V - 0.8V = 1.2V \rightarrow 1.2V \geq 0.7V$      |
| S3     | Opened | 1 and 2 | $V_{FN} - \text{MIN}(V_{in}) \geq V_T \rightarrow 2V - 1.2V = 0.8V \rightarrow 0.8V \geq 0.7V$      |
|        |        |         | $\text{MAX}(V_{in}) - V_{FP} \geq V_T \rightarrow 45.2V - 44V = 1.2V \rightarrow 1.2V \geq 0.7V$    |
| S4     | Closed | 3       | $V_{FN} - \text{MIN}(V_{in}) \geq V_T \rightarrow 2V - 1.6V = 0.4V \rightarrow 0.4V \leq 0.7V$      |
|        |        |         | $\text{MAX}(V_{in}) - V_{FP} \geq V_T \rightarrow 3.1V - 44V = -40.9V \rightarrow -40.9V \leq 0.7V$ |

During the ground shifting event the reference points of VIN1, VIN2, VIN3, VIN4, and the multiplexer will all be shifted to be greater than 0 V. This causes VIN1 and VIN2 to go below the reference potential of the switch – creating a fault condition and opening the switches S1 and S2. VIN3 not only violates the minimum voltage accepted into the channel protector, but also exceeds the maximum fault threshold causing the switch, S3, to either be opened due to over or under voltage. Finally, S4 is closed because the fault level + threshold was not met by VIN4 keeping the switch in a closed position and operating normally.

Next, the topic of miss-wiring. This is handled in very much the same way as the other fault protection features. Miss-wiring will often lead to too large of voltages on the incorrect pins. The previous fault protections still apply. If a miss-wiring creates an over or under voltage on one of the input pins and the signal is within the protection specs then TI's Fault Protected Switches and Multiplexers will treat the miss-wiring as any other fault by detecting it and dealing with it by opening the switch or clamping the output or by keeping the switch high impedance when VDD is floating or 0V.

The final issue that was discussed in section one is that of latch-up events. These are prevented by using Latch-Up Immune Multiplexers and Switches – which TI's Fault Protected Switches and Multiplexers are all Latch-Up Immune by Construction. In general, using buried oxide trench layers along with proper layout and guard rings latch up immunity is achieved by breaking the formation of the SCR with trenches and absorbing extra injected charge through guard rings or other similar structures. This means if a latch up causing event (injected current or voltage transient) is input to the Fault Protected Switch/Multiplexer the device will not latch up. This has two benefits – the first being that the VDD and VSS/GND pins will not be shorted as latch up will not happen and the second is that more sensitive parts are protected from latch up causing signals – as not every electronic component is built latch up immune. TI's Fault Protected Switches and Multiplexers not only will prevent latch up, but since most latch up causing events are related to electrical overstress the fault protected multiplexer or switch can isolate the fault channel further preventing latch-up events down-stream from the input of the system.

### 3 Key Care Abouts when Implementing a Fault Protected Multiplexer into an Analog I/O Module

Now that it has been shown the fault protection features on TI's Fault Protected Switches and Multiplexers can help prevent system damage during multiple types of fault conditions it is now time to focus the attention on the impact the device has on the signal chain during normal – non-fault condition- operation. This topic is discussed in detail in TI's application note, [Discrete ADC Input Expansion Using Precision Multiplexers](#) which greatly mimics the analog input module scheme of either Op Amps or ADC's following the multiplexer/switch. While the parts discussed in that app note are labeled precision – TI's Fault Protected Switches and Multiplexers are also precision. Following is a brief synopsis of the key care abouts in these systems as well as a look into some fault protected specific parameters.

Ideally a multiplexer or switch will have no effect on the signal chain when the switch is closed and it acts a perfect open circuit when the switch is open. This is not the case as in reality there are multiple parameters that affect switch operation that deviate from the ideal case.

The first deviation is that of the switch channel itself – ideally it is assumed to a be perfect conductor. In reality the switch, when closed, acts as a RC filter with the resistance being the channel resistance and the C being the parasitic capacitance to ground. The load can then add to the output capacitance and change the channel parameters as well. If the RC were constant the only real worry would be attenuation of higher frequencies – however the channel resistance ( $R_{on}$ ) will vary with input voltage, so for a variable voltage signal the RC time delay to the output of the switch/mux will be different depending on what input voltage was applied – this can cause distortion to the system. This is mitigated by using multiplexers and switches with a flat on resistance and a flat on capacitance response. Where flatness means how much the values vary due to input signal levels. A system that has a variable R and C can create distortion by creating different propagation delays for different input voltages. The flatter these responses are the more constant of a propagation delay will be observed which in turn results in very little to no added distortion. Using a device with a low on resistance response also helps alleviate any signal attenuation across the switch/multiplexer. For a quick example the TMUX7462F at supplies of +/-15V has a typical on resistance flatness of  $0.6\Omega$  with a worst case of  $1\Omega$  and has an on capacitance of 16pF. Assuming 0pF of additional capacitance from the system – the prop delay differences can be typically around 9.6ps to 16ps. These are very small differences and when compared to the input signal generally these differences will be negligible showing that precision multiplexers like TI's Fault Protected Switches and Multiplexers. However large output capacitances can greatly increase these delays and therefore distortion.

Besides the channel impact there are other errors that can result in issues for the system. Multiplexers and Switches will have leakage current associated with them – these are currents that ideally don't exist. Off leakage is current that is being sourced/sunk by a pin when it is unselected or opened – this is specifically leakage during normal conditions with no faults and VDD is active. On leakage is leakage current through an on channel – essentially this causes the current going into the switch to not equal the current coming out of the switch – this can cause offsets and errors at the output of the multiplexer. These leakage currents are worst at high temperatures and to mitigate the effects devices with low leakage should be utilized. The TMUX7308F for example at +/-15 V supplies has typical off leakages of 100pA and worst case off leakage peaking at +/-8nA for source pins and +/- 15nA for the drain pin. While typical on leakages of 300pA with the on leakage worst case peaking at +/-25nA. With low currents and low on resistances offset and voltage errors can be kept low.

On the topic of leakage currents there are three other values – the leakage under powered off conditions, leakage when supply pins are floating, leakage during fault condition. These are all called leakage currents under fault – the TMUX7462F data sheet is shown in [Figure 3-1](#) to see how these specs are reported.

| FAULT CONDITION |   |   |                 |           |               |
|-----------------|---|---|-----------------|-----------|---------------|
| $I_{S(FA)}$     | Input leakage current under overvoltage | $V_S = \pm 60\text{ V}$ , $GND = 0\text{V}$ , $V_{DD} = V_{FP} = 16.5\text{ V}$ , $V_{SS} = V_{FN} = -16.5\text{ V}$                    | -40°C to +125°C | $\pm 100$ | $\mu\text{A}$ |
| $I_{S(FA)}$     | Input leakage current under overvoltage | $V_S = \pm 60\text{ V}$ , $GND = 0\text{V}$ , $V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0\text{ V}$ , $V_{DR} = 0\text{ V}$ or floating      | -40°C to +125°C | $\pm 125$ | $\mu\text{A}$ |
| $I_{S(FA)}$     | Input leakage current under overvoltage | $V_S = \pm 60\text{ V}$ , $GND = 0\text{V}$ , $V_{DD} = V_{SS} = V_{FP} = V_{FN} = \text{floating}$ , $V_{DR} = 0\text{ V}$ or floating | -40°C to +125°C | $\pm 125$ | $\mu\text{A}$ |

Figure 3-1. TMUX7462F Fault Condition Leakage Table

## 4 Summary

In this application note a few ideas were explored. First, some common fault conditions for Analog Input Modules were examined and how they can impose a risk to a system's reliability. Then using the fault protection features offered by TI's Fault Protected Switches and Multiplexers it was shown that these common fault conditions can be handled by a Fault Protected Switch or Multiplexer. Finally, the key care-about's to when implementing a TI Fault Protected Switch or Multiplexer to optimize not only protection but system performance, cost, and solution size. [Table 4-1](#) shows devices available now built with integrated fault protection features.

**Table 4-1. Fault Protected Multiplexers and Switches On TI.com**

| Device    | Configuration | Channel Count | Single Supply Range | Dual Supply Range   |
|-----------|---------------|---------------|---------------------|---------------------|
| TMUX7308F | 8:1           | 1             | 8 V to 44 V         | +/- 5 V to +/- 22 V |
| TMUX7412F | 1:1           | 4             | 8 V to 44 V         | +/- 5 V to +/- 22 V |
| TMUX7462F | 1:1           | 4             | 8 V to 44 V         | +/- 5 V to +/- 22 V |



## 5 References

- Texas Instruments, [Discrete ADC Input Expansion Using Precision Multiplexers](#), application report.
- Texas Instruments, [Using Latch-Up Immune Multiplexers to Help Improve System Reliability](#), application report.
- Texas Instruments, [Latch Up, ESD, and Other Phenomena](#), application report.
- Texas Instruments, [Latch Up](#), white paper.
- Texas Instruments, [TMUX730xF  \$\pm 60\$ -V Fault-Protected, 8:1 and Dual 4:1 Multiplexers with 1.8-V Logic](#), data sheet.
- Texas Instruments, [TMUX741xF  \$\pm 60\$  V Fault-protected, 1:1 \(SPST\), 4-Channel Switches with 1.8-V Logic](#), data sheet.
- Texas Instruments, [TMUX7462F  \$\pm 60\$  V Fault-Protected, Latch-Up Immune, Quad Channel Protector with Adjustable Fault Threshold and 1.8-V Logic](#), data sheet.

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