Application Report
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Low-Power Support Using Texas Instruments SN74SSTV16857 and SN74SSTV16859 DDR-DIMM Registers

Stephen M. Nolan *Standard Linear & Logic*

ABSTRACT

The Texas Instruments SN74SSTV16857 and SN74SSTV16859 registers support the low-power mode of the DDR-DIMM. This application report explains the low-power mode and the features of the registers that support the low-power mode. Also, the considerations that the system designer must be aware of when implementing the low-power state of a registered memory module are explained. The sequence that must be followed to utilize the register properly is detailed, including the interpretation of the associated register timing specifications. Finally, the different static- and dynamic-current specifications are analyzed, along with examples of how to calculate the dynamic operating current requirement of the registers.

Contents

List of Figures

Introduction

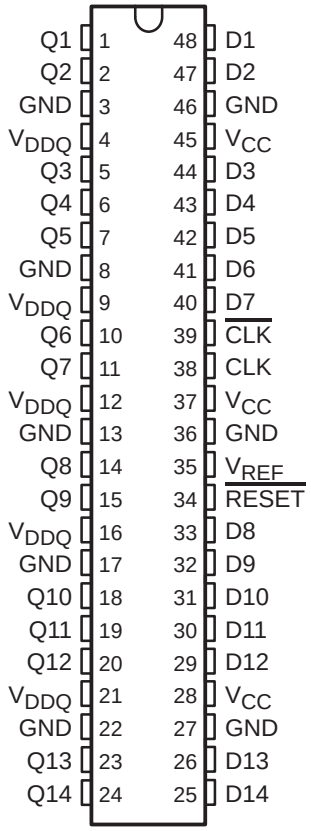
The widespread demand for more main-memory capacity and bandwidth in computer systems has lead to the development of the JEDEC standard for DDR-SDRAM-based, 184-pin, registered memory modules. These DDR DIMMs provide twice the data-bus bandwidth of previous-generation single-data-rate (SDR) memory systems. To meet the demands of stable functionality over the broad spectrum of operating environments, meet system timing needs, and support data integrity, the loads presented by the large banks of SDRAMs on the DIMM modules require the use of registers in the address and control signal paths.

Texas Instruments offers the SN74SSTV16857 and SN74SSTV16859 registers to support DDR memory modules. The SSTV16857 (see Figure 1) is a 14-bit input to 14-bit output device to support planar DDR memory modules. The SSTV16859 (see Figure 2) is a 13-bit input to 26-bit output device to support stacked DDR memory modules.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or floating	X or floating	X or floating	L

DGG PACKAGE
(TOP VIEW)



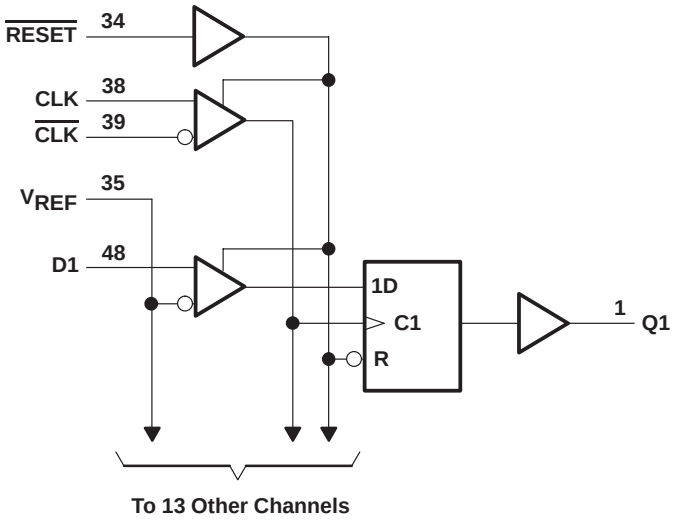


Figure 1. SN74SSTV16857

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or floating	X or floating	X or floating	L

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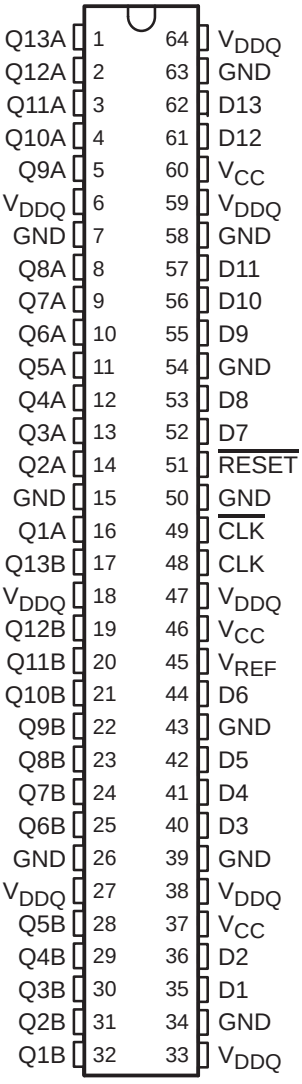


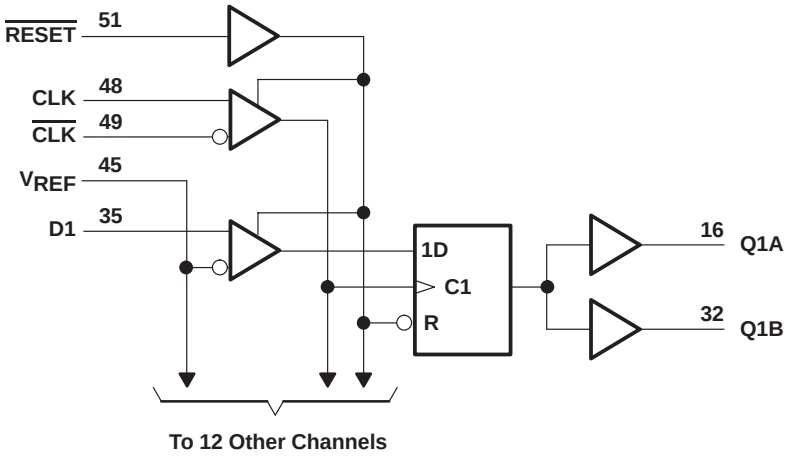


Figure 2. SN74SSTV16859

Background and Features of Registers

DDR-DIMMs can support up to two banks of ×4 SDRAMs, for a maximum of 36 memory integrated circuits (IC) per module. These SDRAM ICs, along with the necessary support components, can present a large power demand. To reduce the power-consumption requirements of main-memory systems, the SDRAM ICs have an idle-state self-refresh mode that provides significant power savings.

After the ENTER SELF-REFRESH MODE command is given to the SDRAM, the SDRAM CKE input must be held at an LVCMOS low level to keep the SDRAM IC in the self-refresh mode. When CKE is low, the SDRAM input buffers, output drivers, and internal DLL are disabled. Data is maintained in the SDRAM, even if the rest of the system is powered down and no external clock signals are applied.

The JEDEC-standard PLL component supports the low-power mode of the memory module by taking advantage of the fact that the SDRAM IC does not require external clocking during self-refresh mode and powers down its inputs and outputs when the clock input signal drops below 20 MHz.

The JEDEC-standard registers, SN74SSTV16857 and SN74SSTV16859, also support low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential-input receivers are disabled, and undriven (floating) register data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input always must be held at a valid logic high (V_{CC}) or low (GND) level. To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

Sequence of Entering and Exiting the Low-Power State

Considerations of Register

The SN74SSTV16857 and SN74SSTV16859 registers can be used to support the low-power states of the memory system by properly asserting the $\overline{\text{RESET}}$ signal. There are some factors that must be considered when implementing the low-power state.

Prior to entering reset, all the data lines and the clock lines must be at valid logic levels. Then, when the $\overline{\text{RESET}}$ line goes from high to low, the differential input amplifiers begin to shut off. The designer expects that, upon entering reset, the chipset is able to float the command/address bus and clock signals to the differential inputs of the registers. Of course, the differential receivers do not shut down instantaneously. They take approximately 22 ns to shut off. The chipset *must* continue to hold valid data and clock signals on the register inputs until the differential receivers are powered down completely. This time is called t_{inact}, the time it takes for the differential receivers to become inactive after $\overline{\text{RESET}}$ goes low. After t_{inact} has elapsed, following the assertion of $\overline{\text{RESET}}$ low, the chipset can float the register data and clock inputs.

Before exiting reset, the chipset must apply valid clock inputs and valid data to the register inputs. There is no critical setup time for valid data inputs prior to $\overline{\text{RESET}}$ high. As long as the designer understands that the memory controller must apply valid logic levels before taking $\overline{\text{RESET}}$ high, that is adequate. It is not necessary to specify how long before $\overline{\text{RESET}}$ is taken high. The memory controller applies valid data first, then raises $\overline{\text{RESET}}$ high. If data and clock are applied to the register inputs prior to taking $\overline{\text{RESET}}$ high, operation is correct.

Then, with valid clock inputs and valid data (all lows) applied, $\overline{\text{RESET}}$ goes from low to high. It takes about 22 ns for the differential receivers to come up. That time is called t_{act}. During that time, the chipset must hold all lows on the data inputs. The register outputs must stay low (no glitches allowed) to ensure that the CKE input of the SDRAM is held low. After t_{act} has elapsed, all the differential inputs are powered up, and the chipset can begin to clock data through the register.

Sequence to Enter the Low-Power Mode and Interpretation of t_{inact}

The DIMM application enters the standby state as follows:

1. When the part is functional ($\overline{\text{RESET}}$ = high), the chipset issues a command to the SDRAM for it to enter self-refresh (low-power) mode. The command is clocked through the register to the SDRAM.

2. The chipset then puts the register into standby mode ($\overline{\text{RESET}}$ = low). The transition of $\overline{\text{RESET}}$ from high to low is specified as a fully asynchronous signal. There is no relationship between the $\overline{\text{RESET}}$ transition and the timing of the clock signal.

3. The register drives all outputs low, so the SDRAM sees all of its command and address inputs as low. The self-refresh state then is held by the SDRAM as long as the SDRAM receives its CKE input at an LVCMOS low.

4. The register disables the differential inputs, and t_{inact} must elapse from $\overline{\text{RESET}}$ low until the inputs are fully disabled.

5. After the specified 22 ns has elapsed, the chipset puts its command/address outputs (the data inputs to the register) in the high-impedance state. The command/address bus can be terminated to V_{TT} through SSTL_2 standard termination resistors. If the bus is terminated when it is in the high-impedance state, V_{TT} is equal to V_{REF}. When $V_{TT} = V_{REF}$, each differential data-input receiver has the same voltage applied to both inputs. That explains the need to disable the data input receivers during $\overline{\text{RESET}}$ low.

6. The motherboard then disables the clock signal to the DIMM. The CDCV857 PLL clock-driver chip on the DIMM senses that the input has dropped, enters a low-power state, and puts its outputs in the high-impedance state. The CLK and $\overline{\text{CLK}}$ inputs to the register are driven by the CDCV857 and are parallel terminated by a resistor. Therefore, when the CDCV857 disables its outputs, the CLK and $\overline{\text{CLK}}$ inputs are pulled to the same voltage by the parallel-termination resistor between them. This explains the need to disable the CLK and $\overline{\text{CLK}}$ input receivers during $\overline{\text{RESET}}$ low.

7. The entire DDR-DIMM now is in a standby state. The PLL component is in a low-power state, due to the absence of a clock signal at its inputs. The register device is in a low-power state due to the low input to $\overline{\text{RESET}}$. The SDRAM is being held in self-refresh by the low outputs of the register, which keeps the CKE input of the SDRAM at an LVCMOS low.

Sequence to Exit the Low-Power Mode and Interpretation of t_{act}

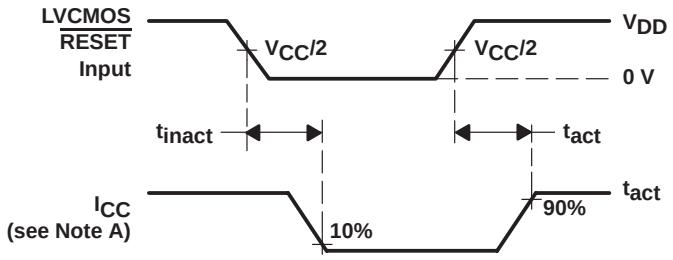
The DIMM application leaves the standby state as follows:

1. With the DIMM in standby state, the motherboard initially must supply a clock signal. The CDCV857 PLL device on the DIMM recognizes a stable clock signal on its inputs, locks the PLL, and enables the outputs. The PLL requires 100 μs to stabilize after receiving a valid clock. After this time, the register sees a stable clock at its clock inputs.
2. During the stabilization of the PLL, the memory-controller chipset must enable its command/address bus and apply valid logic levels to the data inputs of the register. The chipset should apply all low logic levels, so that the SDRAM still sees its CKE input low and remains in the self-refresh mode while the register is enabled.
3. While holding the register data inputs low, the chipset then changes the $\overline{\text{RESET}}$ input of the register from low to high. The transition of $\overline{\text{RESET}}$ from low to high is specified as a fully asynchronous signal. There is no relationship between the time of the $\overline{\text{RESET}}$ transition and the timing of the clock signal.
4. During the time from the transition of $\overline{\text{RESET}}$ from low to high, until the input receivers are stable, the register must ensure by design that, as long as the data inputs are low and the clock signal is valid, it does not glitch the outputs. The device must hold the outputs low during this time or the SDRAM may begin to prematurely exit self-refresh mode.
5. The time from $\overline{\text{RESET}}$ high until the inputs are fully enabled is specified on the data sheet as t_{act}. The chipset designers have to know how long the register takes to become stable.
6. After the specified 22 ns has elapsed, the chipset issues the NOP command. This command is clocked through the now fully operational register to the SDRAM. The chipset then takes the CKE line high, and the SDRAM exits self-refresh mode. This is clocked through the register as well.
7. Then, the chipset can begin the JEDEC-defined exit self-refresh procedure, after which the DDR SDRAM is ready for normal operation.

The sequence for entering and exiting the standby state on the DIMM is not a fast sequence. The response time of the register to the $\overline{\text{RESET}}$ input is 22 ns, but it still does not significantly impact the overall time of the complete operation. However, it is necessary to specify fully the required times on the data sheet, so that chipset designers can accommodate them. Also, it is imperative that, by design, the outputs are stable (low) during the transition into and out of the reset state, and that it is comprehended that the $\overline{\text{RESET}}$ signal can be applied asynchronously to the clock signal.

How t_{inact} and t_{act} Are Characterized

Except for the change in I_{CC}, there is no externally testable signal that responds to the input receivers being powered up or powered down in response to the $\overline{\text{RESET}}$ signal. The only way to test t_{act} and t_{inact} in the laboratory is to measure the change in I_{CC} due to the powering up and powering down of the differential amplifiers. The response time from an externally applied input to the change in power-supply current is not a typical production-test parameter, so t_{act} and t_{inact} can be expected to be specified by design and characterization, but not by production testing (see Figure 3).



VOLTAGE AND CURRENT WAVEFORMS
INPUT ACTIVE AND INACTIVE TIMES

NOTE A: I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

Figure 3. Parameter Measurement Information (V_{DD} = 2.5 V ± 0.2 V)

Dynamic- and Static-Current Specifications

The dynamic and static supply currents are measured at the V_{CC} pins only, not at the V_{DDQ} pins. Also, the tests are specified with I_O = 0 mA. The I_{CCD} (dynamic current) measurements are dominated by the internal clock and data paths, because the output current is 0 mA and the I_{DDQ} current is not added. Power (at the output) is very small, except for the effects of switching the final output, which causes through current in the output totem-pole driver as it transitions through threshold.

I_{CC} Static Standby Current

The fundamental current term I_{CC} (static standby) is the lowest power state of the device. The $\overline{\text{RESET}}$ input is low (GND), which disables all of the other (differential) inputs. The states of the other inputs are a “don’t care” as long as $\overline{\text{RESET}}$ is low. The device is static because the clock input is being ignored. I_{DDQ} (current into the V_{DDQ} pin) is *not* included in the I_{CC} current specifications; however, I_O (output current) is specified to be 0 mA (no load) during these tests to ensure that there is no effect due to leakage paths. This is the current you can expect to see when the DIMM is in standby (SDRAMs in self-refresh mode, clock driver shut off). This term is a maximum and has guardband built in to ensure production testability.

I_{CC} Static Operating Current

The next highest current term, with everything enabled, but static (not switching), is I_{CC} (static operating). Therefore, the $\overline{\text{RESET}}$ input is high (V_{CC}) and all the differential inputs are enabled. *All* differential inputs are held static at the SSTL_2 $V_{IH(AC)}$ or $V_{IL(AC)}$ levels. Of the levels that hold the inputs, these are the worst case, with respect to I_{CC}. If all the inputs are held at the rails (V_{CC} or GND), we can expect a reduction in I_{CC} of probably two orders of magnitude. In the application space where registered DIMMs are to be used, the use of terminated address/control bus and clocks on the inputs of the register are common. Again, in this test condition, as in all others, I_O (output current) is specified at 0 mA (no load), even though I_{DDQ} is not included. This term is a maximum and has guardband built in to ensure production testability. The I_{CC} (static operating) term provides the intercept point on the Y axis (current) at 0 MHz for calculating dynamic current. It is not the current into the device you would expect to see during normal system operation because it is *static*. Certain combinations of CLK high or low, $\overline{\text{CLK}}$ low or high, and D inputs high or low, might give higher maximum currents. All possible legal input conditions (CLK and $\overline{\text{CLK}}$ *must* be complementary) must be tested in characterization to ensure that the maximum is found.

I_{CCD} Dynamic Operating Current – Clock Only

I_{CCD} (dynamic operating, clock only) comprehends the dynamic current consumed by the device due to the switching of the CLK/$\overline{\text{CLK}}$ input pair (clock). It is specified as μA/MHz. Again, $\overline{\text{RESET}}$ is held high (V_{CC}) to enable the inputs. The data (D) inputs are held at SSTL_2 $V_{IH(AC)}$ or $V_{IL(AC)}$ levels, and the clock input is switching at 50% duty cycle (clock input is switching at its specified worst-case minimum peak-to-peak differential voltage of 360 mV and tested at all specified crossing points from 0.97 V to 1.53 V). Again, I_O = 0 mA and I_{DDQ} is not included. I_{CCD} (dynamic operating, clock only) is characterized only and not production tested. It is specified as a typical value only and should not have any guardband added because it is a slope. This value adds to the I_{CC} (static operating) term. The additional current into the V_{CC} pin due to switching the clock is:

$$I_{CC}\text{ (clock)} = I_{CCD}\text{ (clock)} \times \text{frequency (clock)}$$

If, for example, the I_{CCD} (clock) was 52 μA/MHz, and you are operating at 125 MHz, the dynamic current due to clock switching is:

$$52\ \mu\text{A/MHz} \times 125\ \text{MHz} = 6.5\ \text{mA}$$

This current is added and is in addition to the specified maximum static operating current. For example, if the clock input is switching and none of the data inputs are switching, the total maximum current into the V_{CC} pin of the device is:

$$I_{CC}\text{ (total)} = I_{CC}\text{ (static operating)} + I_{CC}\text{ (clock)}$$

Substituting:

$$I_{CC}\text{ (total)} = I_{CC}\text{ (static operating)} + [I_{CCD}\text{ (clock)} \times \text{f (clock)}]$$

Using our hypothetical example, if I_{CC} (static operating) was 56 mA, the total current into the V_{CC} pin of the device, with only clock switching is:

$$I_{CC}\text{ (total)} = 56\ \text{mA} + (52\ \mu\text{A/MHz} \times 125\ \text{MHz}) = 62.5\ \text{mA}$$

I_{CCD} Dynamic Operating Current – Each Data Input

I_{CCD} (dynamic operating, per data input) is the dynamic current consumed by the device due to the switching of each data input, and is specified as μA/MHz. The MHz in this term is the switching frequency of the *clock* input pair. The command/address bus and, therefore, this device, does not operate at double data rate. If the data through this device are at the same speed as the clock, the maximum frequency still is one-half the clock frequency. Again, $\overline{\text{RESET}}$ is held high (V_{CC}) to enable the inputs. One data (D) input is switching between SSTL_2 $V_{IH(AC)}$ and $V_{IL(AC)}$ levels, 50% duty cycle, one-half clock frequency. All other D inputs are held at SSTL_2 $V_{IH(AC)}$ or $V_{IL(AC)}$ levels, and the clock input is switching at 50% duty cycle (clock input is switching at its specified worst-case minimum peak-to-peak differential voltage of 360 mV and tested at all specified crossing points from 0.97 V to 1.53 V). Again, I_O = 0 mA and I_{DDQ} is not included. I_{CCD} (dynamic operating, per each data input) is characterized only, and not production tested. It is specified as a typical value only, and should not have any guardband added because it is a slope. This value adds to the I_{CC} (static operating) term and to the I_{CCD} (clock) term. The additional current into the V_{CC} pin due to switching the data inputs is:

I_{CC} (total data) = I_{CCD} (each data) × frequency (clock) × number data inputs switching

For example, if the I_{CCD} (data) was 9-μA/clock MHz/D input, with all 14 bits switching and a clock frequency of 125 MHz, the I_{CC} (data) current would be:

I_{CC} (total data) = 9 μA × 125 MHz × 14 = 15.75 mA

Calculating Power Consumption in the Application

The formula for calculating the total maximum current into the device is:

I_{CC} (total) = I_{CC} (static operating) + I_{CC} (clock) + I_{CC} (total data)

Substituting:

I_{CC} (total) = I_{CC} (static operating) + [I_{CCD} (clock) × f (clock)]
+ [I_{CCD} (each data) × frequency (clock) × number data inputs switching]

Following the hypothetical examples given above, the total maximum dynamic current into the device at 125 MHz, with all bits switching is:

I_{CC} (total) = 56 mA + (52 μA/MHz × 125 MHz) + (9 μA × 125 MHz × 14) = 78.25 mA

Note that the values used in the examples are *hypothetical* and are not intended to reflect the actual characterized values of the TI devices. Please refer to the latest TI data sheet for actual values.

Summary

The TI SN74SSTV16857 and SN74SSTV16859 registers support the low-power mode of the DDR-DIMM. This application report explains the low-power mode and the features of the registers that support the low-power mode. Also explained are the considerations that the system designer must be aware of when implementing the low-power state of a registered memory module. The operational sequence that must be followed to properly utilize the register is detailed, including the interpretation of the associated register timing specifications. Finally, the different static- and dynamic-current specifications are analyzed, along with examples of how to calculate the dynamic operating current requirement of the registers.

Glossary

CKE	Clock-enable input to SDRAM
DDR	Double data rate
DIMM	Dual inline-pin memory module
DLL	Delay locked loop
IC	Integrated circuit
I_{CC}	Power-supply current consumption
I_{CCD}	Dynamic power-supply current consumption
JEDEC	Joint Electron Device Engineering Council (http://www.jedec.org)
LVCMOS	Low-voltage CMOS
PLL	Phase-locked loop, zero-delay clock buffer IC
SDRAM	Synchronous dynamic random-access memory (JEDEC-standard memory IC)
SSTL_2	2.5-V stub series-terminated logic, JEDEC-specified power-supply and interface-level standard
t_{act}	Differential inputs active time. Data inputs must be held low for a minimum time of t_{act} max after $\overline{\text{RESET}}$ is taken high.
t_{inact}	Differential inputs inactive time. Data and clock inputs must be held at valid levels (not floating) for a minimum time of t_{inact} max after $\overline{\text{RESET}}$ is taken low.

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265