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Interface Logic

TI Programmable Logic Devices (TPLD) can be used to drive indicator light-emitting diodes (LED), and can be programmed to provide simple or complex LED control in a single package. The application pictured in [Figure 1](#) uses the internal oscillator, counter, and DFF modules included in the TPLD1201 to drive an LED. The counter and DFF divide down the oscillator frequency so that the LED blinks at a frequency detectable by the human eye.

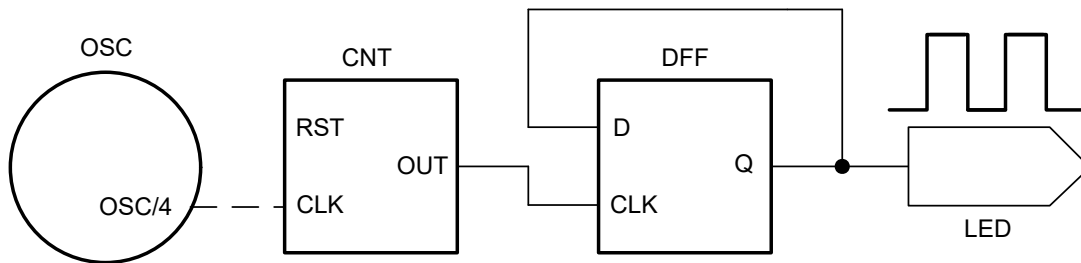


Figure 1. Blinking LED Schematic

Example Configuration

The 25kHz oscillator is given a pre-division of 8, outputting a 3125Hz square wave. The counter module CLK input is sourced from the 25kHz oscillator output further divided by 4, such that the input CLK frequency to the counter becomes 781.25Hz. The counter data is set to 255 (meaning the counter outputs a pulse after 255 rising edges are provided on the CLK input), causing the counter to output a pulse at a frequency of 3Hz. This 3Hz pulse output is fed into a (DFF) with the inverted output option enabled, allowing the DFF to further divide the frequency by half. This 1.5Hz output pulse is then connected to a pin configured to be a push-pull digital output with 2 × drive strength. This pin can be used to drive an LED with a maximum drive strength of 17mA without damaging the device.

OSCILLATOR

Name	OSC
Label	
Power Mode	Force Power On
Clock Source	Internal RC Oscillator
Frequency	25 kHz
Clock Pre Divider	/8
OUT0 Second Stage Divider	/1
OUT1 Second Stage Divider	/1
Power Control Source Select	From register
PDWN Control	Power down
Device MacroCell Allocated	OSC0

COUNTER

Name	CNT
Label	
Clock Source	OSC/4
Control Data	255
Reset Mode	Both falling and rising e...
Device MacroCell Allocated	LUT4_0_CNTDLY2

Figure 2. Oscillator and Counter Configurations












D FLIP FLOP 		PIN 	
Name	DFF	Name	LED
Label		Label	
Mode	DFF 	Output Mode	Push Pull 
Generate Inverted Output	<input checked="" type="checkbox"/>	Output Strength	2X 
Invert Clock Input	<input type="checkbox"/>	Enable As GPI Reset	<input type="checkbox"/>
Initial Polarity	Low 	Pin Type	Digital Output 
Reset/Set Select	No Reset or Set 	Add Simulated Load to Output	<input type="checkbox"/>
Device MacroCell Allocated	Any(LUT2_0_DFF0) 	Device Pin Allocated	I07/12  

Figure 3. DFF and Pin Configurations

Design Considerations

- Indicator LEDs typically need 1mA to 20mA of drive current to illuminate. The resistive load at the output pins driving the LEDs must be greater than $(V_{CC} \div I_{DC})\Omega$ to prevent the absolute maximum current output ratings being violated. These current ratings depend on the type of output structure the output pins are programmed for (TPLD1201 pins can be programmed as push-pull or open-drain outputs, with drive strength gains of 1 × or 2 ×). Choose LEDs with forward currents that do not exceed I_{DC} for the chosen output pin configuration at the appropriate VCC.
- Different LED colors require different forward voltages

Common LED Forward Voltages by Color

Red	Orange	Yellow	Green	Blue	White
1.8V	2.0V	2.2V	3.5V	3.6V	4.0V

- Series resistors are used to limit the current through the LEDs and can be estimated with [Equation 1](#):

$$R_{\text{limiting}} = \frac{V_{\text{supply}} - V_{\text{LED}}}{I_{\text{desired}}} \quad (1)$$

- If the output pins of the device are configured as open-drain, NMOS, or PMOS, choose appropriate pulldown or pullup resistors of 10kΩ in Interconnect Studio (ICS) to avoid floating signals on the outputs.
- The output voltage of a logic gate (V_{OH} or V_{OL}) is specified at a given test current only
- [\[FAQ\] How do I determine the output voltage or output current of a CMOS logic device?](#)
- Need additional assistance? Ask our engineers a question on the [TI E2E™ logic support forum](#)

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