Functional Safety Information

TPS61088-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS61088-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

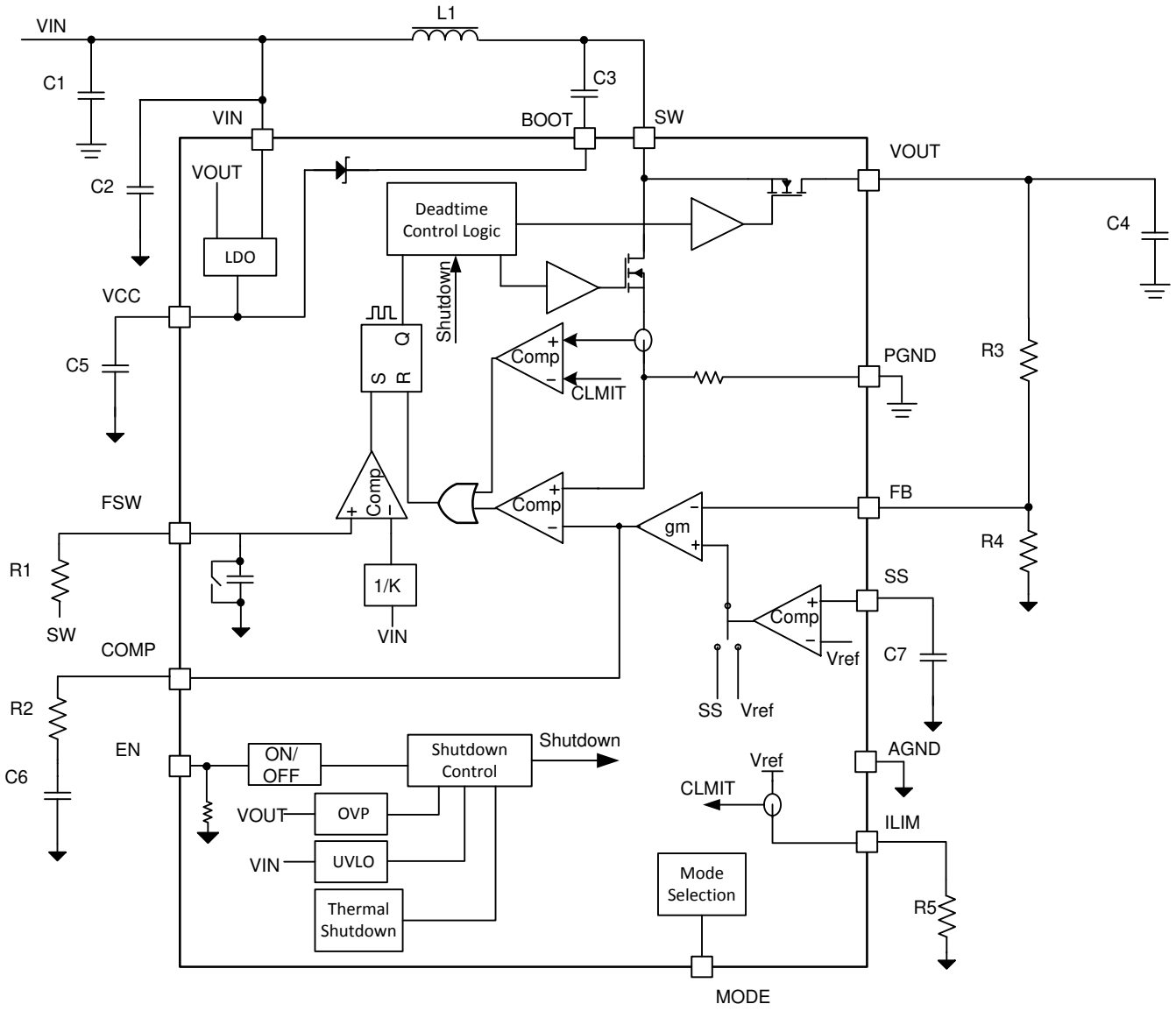

Figure 1-1. Functional Block Diagram

The TPS61088-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS61088-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	17
Die FIT rate	8
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 1000 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS61088-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VO No output GND or HIZ	25
VO output not in specification voltage	25
VO/VIN short to GND	40
Functional, out of spec	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS61088-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS61088-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS61088-Q1 data sheet.

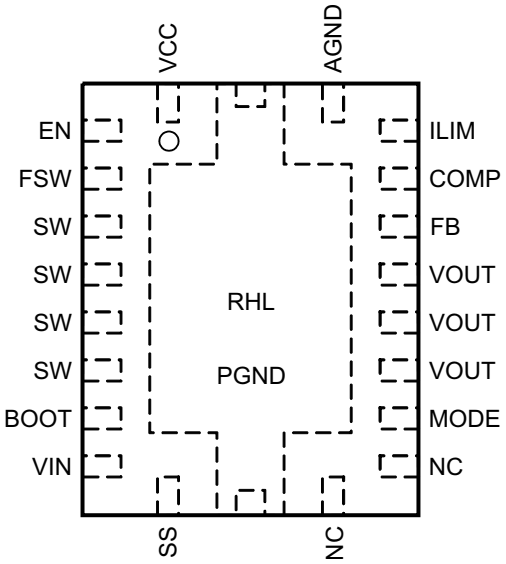

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the 'Recommended Operating Conditions' and the 'Absolute Maximum Ratings' found in the TPS61088-Q1 data sheet.
- Configuration as shown in the 'Application and Implementation' found in the TPS61088-Q1 data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	Output voltage out of regulation	B
EN	2	Loss of ENABLE functionality. The device remains in shutdown mode.	B
FSW	3	The device does not operate.	B
SW	4	Potential damage to inductor and pin	A
SW	5	Potential damage to inductor and pin	A
SW	6	Potential damage to inductor and pin	A
SW	7	Potential damage to inductor and pin	A
BOOT	8	Potential damage to device	A
VIN	9	The device does not operate. The power supply is short.	B
SS	10	The device does not operate.	B
NC	11	No effect	D
NC	12	No effect	D
MODE	13	The device remains in PWM, PFM is lost.	C
VOUT	14	Potential damage to device	A
VOUT	15	Potential damage to device	A
VOUT	16	Potential damage to device	A
FB	17	OVP is triggered and output voltage is out of regulation.	B
COMP	18	No output voltage	B
ILIM	19	Correct output voltage. No current limit	C
AGND	20	No effect	D
PGND	21	No effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	High ripple on the VCC pin. Efficiency is lower.	C
EN	2	Loss of ENABLE functionality. Device remains in shutdown mode.	B
FSW	3	The device does not operate.	B
SW	4	Potential damage to inductor and pin	A
SW	5	Potential damage to inductor and pin.	A
SW	6	Potential damage to inductor and pin.	A
SW	7	Potential damage to inductor and pin.	A
BOOT	8	Possible device damage	A
VIN	9	The device does not work. V_{OUT} = 0 V	B
SS	10	Loss of soft start functionality	C
NC	11	Worse thermal dissipation	C
NC	12	Worse thermal dissipation	C
MODE	13	The device remains in PFM, PWM is lost.	C
VOUT	14	Potential damage to inductor and pin	A

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VOUT	15	Potential damage to inductor and pin	A
VOUT	16	Potential damage to inductor and pin	A
FB	17	Output voltage is out of regulation	B
COMP	18	Output voltage is out of regulation	B
ILIM	19	Triggers minimum on time. The output voltage cannot be set.	B
AGND	20	Possible device damage	A
PGND	21	Possible device damage	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	EN	Loss of ENABLE functionality. The device remains in operating mode.	C
EN	2	FSW	Unstable working frequency	C
FSW	3	SW	Maximum working frequency	C
SW	4	SW	No effect	D
SW	5	SW	No effect	D
SW	6	SW	No effect	D
SW	7	BOOT	Bad thermal performance	C
BOOT	8	IN	Possible device damage	A
VIN	9	SS	The SS pin is damaged if supply voltage is higher than 7 V.	A
SS	10	NC	The device does not operate if NC is grounded.	B
NC	11	NC	No effect	D
NC	12	MODE	The device remains in PWM. PFM is lost if NC is grounded.	C
MODE	13	VOUT	The MODE pin damaged if output voltage is higher than 7 V.	A
VOUT	14	VOUT	No effect	D
VOUT	15	VOUT	No effect	D
VOUT	16	FB	The FB pin damaged if VOUT voltage is higher than 3.6 V.	A
FB	17	COMP	Triggers minimum on time. The output voltage is out of regulation.	B
COMP	18	ILIM	Triggers minimum on time. The output voltage is out of regulation.	B
ILIM	19	AGND	Correct output voltage. No current limit	C
AGND	20	PGND	No effect	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	The VCC pin damaged if supply voltage is higher than 7 V.	A
EN	2	The EN pin damaged if supply voltage is higher than 7 V.	A
FSW	3	Maximum working frequency	C
SW	4	Damage to internal power FETs	A
SW	5	Damage to internal power FETs	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	6	Damage to internal power FETs	A
SW	7	Damage to internal power FETs	A
BOOT	8	Possible device damage	A
VIN	9	No effect	D
SS	10	The SS pin is damaged if supply voltage is higher than 7 V.	A
NC	11	Possible device damage due to large current when NC is grounded	A
NC	12	Possible device damage due to large current when NC is grounded	A
MODE	13	The MODE pin damaged if supply voltage is higher than 7 V.	A
VOUT	14	$V_O = V_{IN}$	B
VOUT	15	$V_O = V_{IN}$	B
VOUT	16	$V_O = V_{IN}$	B
FB	17	The FB pin is damaged if supply voltage is higher than 3.6 V.	A
COMP	18	The COMP pin is damaged if supply voltage is higher than 7 V.	A
ILIM	19	The ILIM pin is damaged if supply voltage is higher than 3.6 V.	A
AGND	20	Possible device damage due to large current	A
PGND	21	Possible device damage due to large current	A

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