Functional Safety Information

BQ77207

Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for BQ77207 (DSS package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

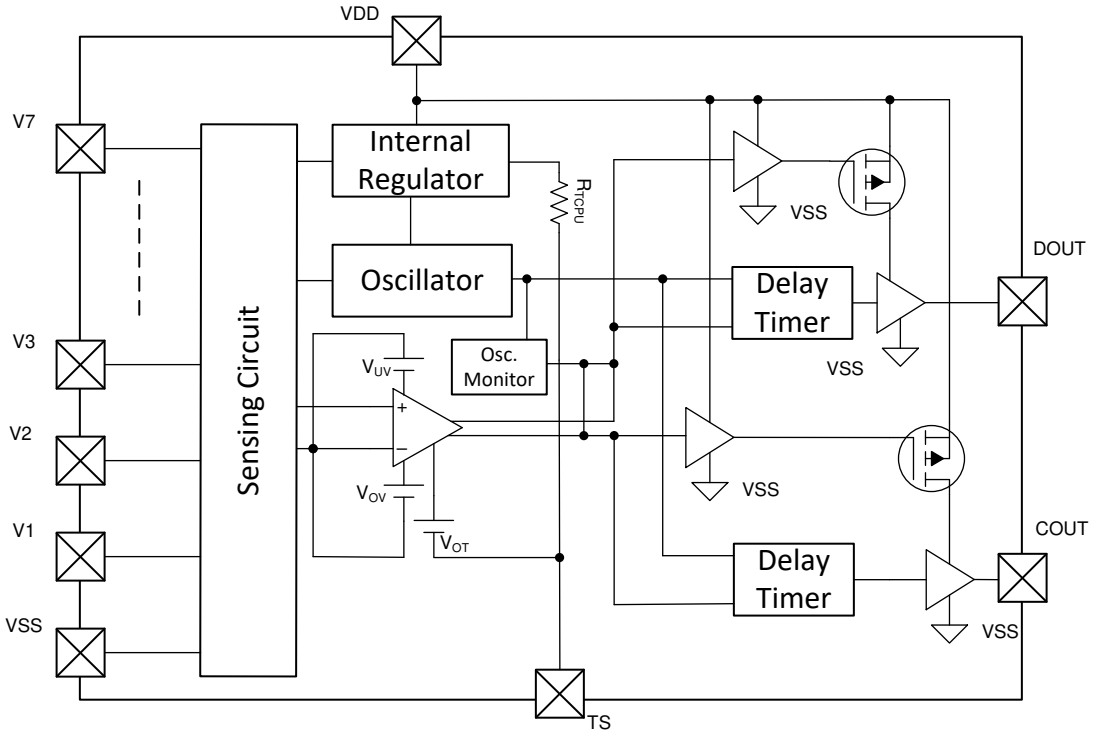

Figure 1-1. Functional Block Diagram

BQ77207 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for BQ77207 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1.2 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed =<50V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for BQ77207 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
COUT enable trigger failure	25%
DOUT enable trigger failure	25%
COUT false trigger	25%
DOUT false trigger	25%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the BQ77207. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the BQ77207 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the BQ77207 data sheet.

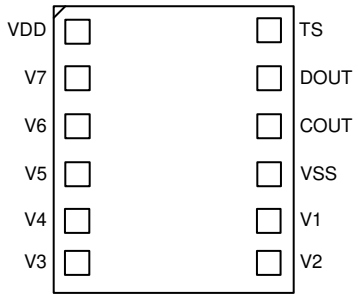

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No power to part	B
V7	2	Automatic OV detection.	D
V6	3	Automatic OV detection.	D
V5	4	Automatic OV detection.	D
V4	5	Automatic OV detection.	D
V3	6	Automatic OV detection.	D
V2	7	Automatic OV detection.	D
V1	8	Automatic OV detection.	D
VSS	9	Function as normal	D
COUT	10	No output signal to system	B
DOUT	11	No output signal to system	B
TS	12	Automatic OT detection.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No power to part	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V7	2	Automatic OW detection.	D
V6	3	Automatic OW detection.	D
V5	4	Automatic OW detection.	D
V4	5	Automatic OW detection.	D
V3	6	Automatic OW detection.	D
V2	7	Automatic OW detection.	D
V1	8	Automatic OW detection.	D
VSS	9	No power to part	B
COUT	10	No output signal to system	B
DOUT	11	No output signal to system	B
TS	12	No OT detection.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	V7	Function as normal	C
V7	2	VDD	Function as normal	C
V6	3	V7	Automatic OV detection.	D
V5	4	V6	Automatic OV detection.	D
V4	5	NC	Function as normal	D
V3	6	V4	Automatic OV detection	D
V2	7	V3	Automatic OV detection.	D
V1	8	V2	Automatic OV detection.	D
VSS	9	V1	Automatic OV detection.	D
COUT	10	VSS	No output signal to system	B
DOUT	11	COUT	No output signal to system	B
TS	12	DOUT	Automatic OT detection.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Function as normal	C
V7	2	AFunction as normal	C
V6	3	Automatic OV detection.	D
V5	4	Automatic OV detection.	D
V4	5	Automatic OV detection.	D
V3	6	Automatic OV detection.	D
V2	7	Automatic OV detection.	D
V1	8	Automatic OV detection.	D
VSS	9	Automatic OW detection.	D
COUT	10	No output signal to system	B
DOUT	11	No output signal to system	B
TS	12	No OT detection.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (April 2022)	Page
• Updated Pin Failure Mode Analysis (Pin FMA)	5

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