

Functional Safety Information
LMR51440 and LMR51450
Functional Safety FIT Rate, FMD and Pin FMA



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1 Overview

This document contains information for LMR51440 and LMR51450 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

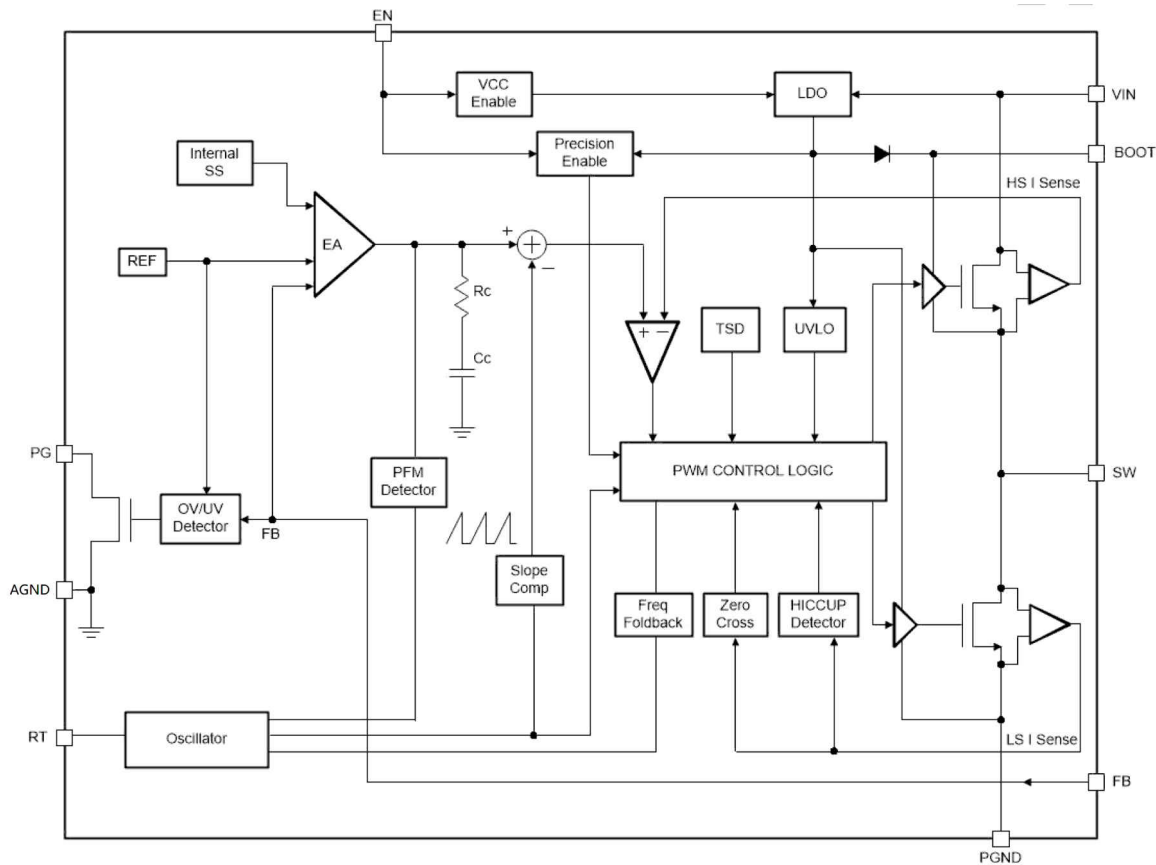


Figure 1-1. Functional Block Diagram

LMR51440 and LMR51450 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LMR51440 and LMR51450 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total Component FIT Rate	12
Die FIT Rate	7
Package FIT Rate	5

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 750 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog / mixed signal less than 50-V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LMR51440 and LMR51450 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution
SW no output	45%
SW output not in specification – voltage or timing	40%
SW power FET stuck on	5%
PGOOD false trip, fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LMR51440 and LMR51450. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 4-1](#) shows the LMR51440 and LMR51450 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMR51440 and LMR51450 data sheet.

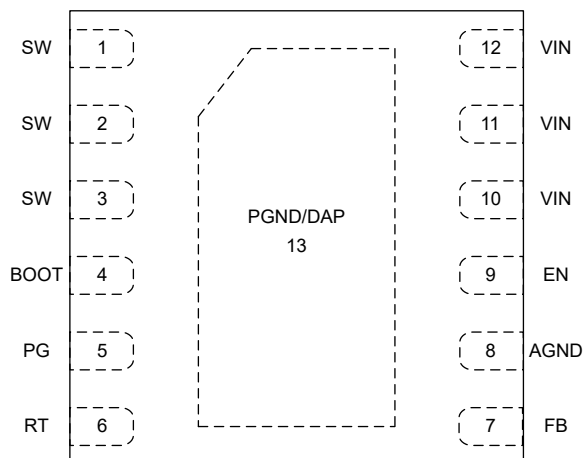


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the [LMR51440](#) and [LMR51450](#) data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	Damage to internal power FET(s) and/or other internal circuits	A
SW	2	Damage to internal power FET(s) and/or other internal circuits	A
SW	3	Damage to internal power FET(s) and/or other internal circuits	A
BOOT	4	$V_{OUT} = 0$ V, possible damage to internal circuits	A
PG	5	No power-good function	B
RT	6	Normal operation	D
FB	7	The regulator operates at maximum duty cycle. Output voltage rises to nearly the input voltage (VIN) level. Possible damage to customer load and/or output stage components can occur. No effect on device.	B
AGND	8	Normal operation	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	9	Loss of ENABLE functionality Device remains in shutdown mode.	B
VIN	10	Device does not operate. No output voltage is generated. Output capacitors discharges through input short. Large reverse current can damage device.	A
VIN	11	Device does not operate. No output voltage is generated. Output capacitors discharges through input short. Large reverse current can damage device.	A
VIN	12	Device does not operate. No output voltage is generated. Output capacitors discharges through input short. Large reverse current can damage device.	A
PGND/DAP	13	Normal operation	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	With both pins open: loss of output voltage. With one pin open: some loss of device performance.	B
SW	2	With both pins open: loss of output voltage. With one pin open: some loss of device performance.	B
SW	3	With both pins open: loss of output voltage. With one pin open: some loss of device performance.	B
BOOT	4	Loss of output voltage regulation; low or no output voltage.	B
PG	5	No power good function	B
RT	6	Normal operation	D
FB	7	Loss of output voltage regulation. Output voltage can rise or fall outside of intended regulation window.	B
AGND	8	Loss of output voltage regulation. Possible damage to internal circuits.	A
EN	9	Loss of ENABLE functionality. Erratic operation; probable loss of regulation.	B
VIN	10	With both pins open: loss of output voltage. With one pin open: possible device damage.	A
VIN	11	With both pins open: loss of output voltage. With one pin open: possible device damage.	A
VIN	12	With both pins open: loss of output voltage. With one pin open: possible device damage.	A
PGND/DAP	13	Loss of output voltage regulation. Possible damage to internal circuits.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	SW	No effect	D
SW	2	SW	No effect	D
SW	3	BOOT	$V_{OUT} = 0$ V, possible damage to internal circuits	A
BOOT	4	PG	PG pin ESD damage if BOOT pin voltage > 20 V	A
PG	5	RT	RT pin ESD damage if PG pin voltage > 5.5 V	A
FB	7	AGND	The regulator operates at maximum duty cycle. Output voltage rises to nearly the input voltage (VIN) level. Possible damage to customer load and/or output stage components can occur. No effect on device.	B
AGND	8	EN	Loss of ENABLE functionality. Device remains in shutdown mode.	B
EN	9	VIN	Normal operation, no damage to device. Loss of ENABLE functionality.	B
VIN	10	VIN	No effect	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	11	VIN	No effect	D
PGND/DAP	13	Any	Other pin is shorted to ground, see Table 4-2	Any

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	Damage to internal power FET(s) and/or other internal circuits	A
SW	2	Damage to internal power FET(s) and/or other internal circuits	A
SW	3	Damage to internal power FET(s) and/or other internal circuits	A
BOOT	4	$V_{OUT} = 0$ V. BOOT ESD clamp runs current to destruction.	A
PG	5	Pin ESD Damage if supply voltage > 20 V	A
RT	6	Pin ESD Damage if supply voltage > 5.5 V	A
FB	7	If supply voltage exceeds 5.5 V damage occurs. $V_{OUT} = 0$ V	A
AGND	8	Possible damage to internal circuits or package	A
EN	9	No damage to device. Loss of ENABLE functionality.	B
VIN	10	No effect	D
VIN	11	No effect	D
VIN	12	No effect	D
PGND/DAP	13	Possible damage to internal circuits or package	A

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