Functional Safety Information

LM2936Q-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

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1 Overview

This document contains information for the LM2936Q-Q1 (SOIC, TO-252, VSSOP, and SOT-223 packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

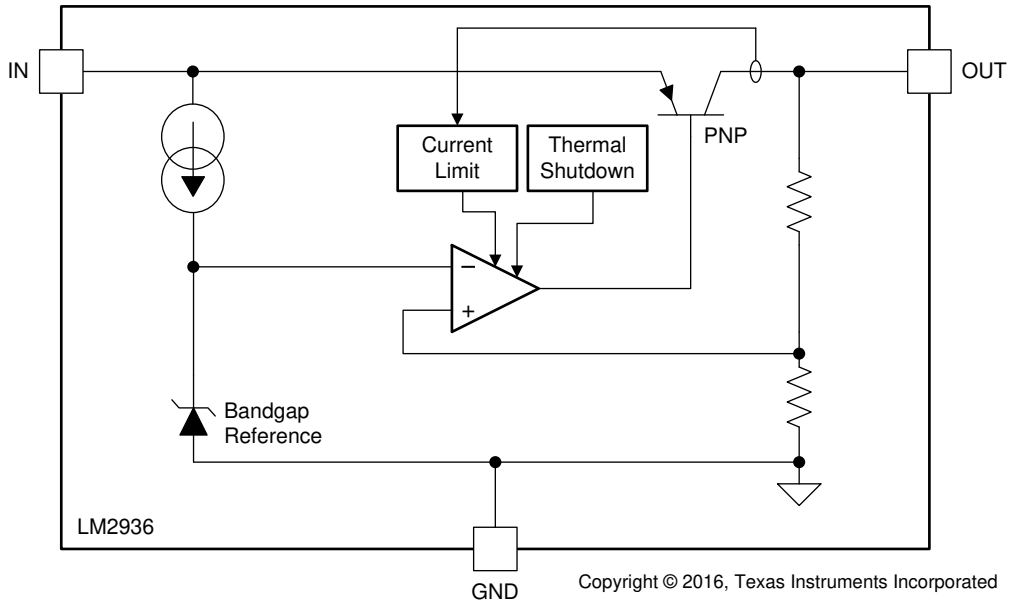

Figure 1-1. Functional Block Diagram

The LM2936Q-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC Package

This section provides functional safety failure in time (FIT) rates for the SOIC package of the LM2936Q-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	18
Die FIT rate	13
Package FIT rate	5

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 TO-252 Package

This section provides functional safety failure in time (FIT) rates for the TO-252 package of the LM2936Q-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	14
Die FIT rate	5
Package FIT rate	9

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 VSSOP Package

This section provides functional safety failure in time (FIT) rates for the VSSOP package of the LM2936Q-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	35
Die FIT rate	30
Package FIT rate	5

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.4 SOT-223 Package

This section provides functional safety failure in time (FIT) rates for the SOT-223 package of the LM2936Q-Q1 based on two different industry-wide used reliability standards:

- Table 2-7 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-8 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-7. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	7
Package FIT rate	6

The failure rate and mission profile information in Table 2-7 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-8. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-8 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM2936Q-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output (output low)	15
Output high (following input)	20
Short any two adjacent pins	5
Output not in specification	60

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM2936Q-Q1 (SOIC, TO-252, VSSOP, and SOT-223 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2, Table 4-6, Table 4-10, and Table 4-14)
- Pin open-circuited (see Table 4-3, Table 4-7, Table 4-11, and Table 4-15)
- Pin short-circuited to an adjacent pin (see Table 4-4, Table 4-8, Table 4-12, and Table 4-16)
- Pin short-circuited to IN (see Table 4-5, Table 4-9, Table 4-13, and Table 4-17)

Table 4-2 through Table 4-17 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device contains the 3-Pin TO-252, 4-Pin SOT-223, 8-Pin SOIC, or 8-Pin VSSOP pin configurations.
- Device operates at free-air temperatures between -40°C and 125°C.
- Device operates at an input voltage less than 40V.
- Device operates according to all recommended operating conditions and does not exceed the absolute maximum ratings.

4.1 SOIC Package

Figure 4-1 shows the LM2936Q-Q1 pin diagram for the SOIC package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM2936Q-Q1 data sheet.

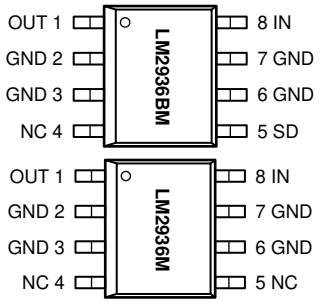

Figure 4-1. Pin Diagram (SOIC) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Device cycles in and out of thermal shutdown depending upon input voltage. Short circuit current limit triggers to clamp output current.	B
GND	2	No effect. Normal operation.	D
GND	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
SD, NC	5	Shutdown is forced off, enabling the device permanently. SD control is lost.	B
		No effect. Normal operation.	D
GND	6	No effect. Normal operation.	D
GND	7	No effect. Normal operation.	D
IN	8	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Power not driven to load. Device is unloaded.	D
GND	2	Marginal thermal performance degradation is possible. Normal operation.	C
GND	3	Marginal thermal performance degradation is possible. Normal operation.	C
NC	4	No effect. Normal operation.	D
SD, NC	5	Shutdown is forced off, enabling the device permanently. SD control is lost.	B
		No effect. Normal operation.	D
GND	6	Marginal thermal performance degradation is possible. Normal operation.	C
GND	7	Marginal thermal performance degradation is possible. Normal operation.	C
IN	8	Device not powered. Device not functional.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	GND	Device cycles in and out of thermal shutdown depending upon input voltage. Short circuit current limit triggers to clamp output current.	B
GND	2	GND	No effect. Normal operation.	D
GND	3	NC	No effect. Normal operation.	D
SD, NC	5	GND	Shutdown is forced off, enabling the device permanently. SD control is lost.	B
			No effect. Normal operation.	D
GND	6	GND	No effect. Normal operation.	D
GND	7	IN	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to IN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Device shuts off as OUT and is now higher than setpoint. Output is no longer regulated.	B
GND	2	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A
GND	3	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A
NC	4	No effect. Normal operation.	D
SD, NC	5	Device shuts down.	B
		No effect. Normal operation.	D
GND	6	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A
GND	7	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A
IN	8	No effect. Normal operation.	D

4.2 TO-252 Package

Figure 4-2 shows the LM2936Q-Q1 pin diagram for the TO-252 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM2936Q-Q1 data sheet.

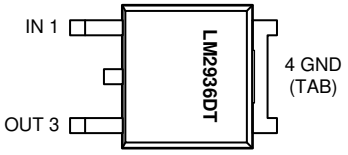

Figure 4-2. Pin Diagram (TO-252 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A
OUT	3	Device cycles in and out of thermal shutdown depending upon input voltage. Short circuit current limit triggers to clamp output current.	B
GND (TAB)	4	No effect. Normal operation.	D

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Device not powered. Device not functional.	B
OUT	3	Power not driven to load. Device is unloaded.	D
GND (TAB)	4	No loop for current to flow, device is inoperable and absolute maximum condition violations are possible.	A, B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	OUT	Device shuts off as OUT is now higher than setpoint. Output is no longer regulated.	B
OUT	3	GND (TAB)	Device cycles in and out of thermal shutdown depending upon input voltage. Short circuit current limit triggers to clamp output current.	B
GND (TAB)	4	IN	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to IN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
OUT	3	Device shuts off as OUT is now higher than setpoint. Output is no longer regulated.	B
GND (TAB)	4	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A

4.3 VSSOP Package

Figure 4-3 shows the LM2936Q-Q1 pin diagram for the VSSOP package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM2936Q-Q1 data sheet.

Figure 4-3. Pin Diagram (VSSOP Package)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Device cycles in and out of thermal shutdown depending upon input voltage. Short circuit current limit triggers to clamp output current.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
NC	5	No effect. Normal operation.	D
NC	6	No effect. Normal operation.	D
GND	7	No effect. Normal operation.	D
IN	8	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Power not driven to load. Device is unloaded.	D
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
NC	5	No effect. Normal operation.	D
NC	6	No effect. Normal operation.	D
GND	7	A floating GND pin results in incorrect voltage regulation or no output voltage. Fast transients have the potential to exceed absolute maximum voltages.	A
IN	8	Device not powered. Device not functional.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC	No effect. Normal operation.	D
NC	2	NC	No effect. Normal operation.	D
NC	3	NC	No effect. Normal operation.	D
NC	5	NC	No effect. Normal operation.	D
NC	6	GND	No effect. Normal operation.	D
GND	7	IN	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A

Table 4-13. Pin FMA for Device Pins Short-Circuited to IN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Device shuts off as OUT is now higher than setpoint. Output is no longer regulated.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
NC	5	No effect. Normal operation.	D
NC	6	No effect. Normal operation.	D
GND	7	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A
IN	8	No effect. Normal operation.	D

4.4 SOT-223 Package

Figure 4-4 shows the LM2936Q-Q1 pin diagram for the SOT-223 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM2936Q-Q1 data sheet.

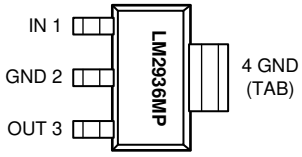

Figure 4-4. Pin Diagram (SOT-223 Package)

Table 4-14. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A
GND	2	No effect. Normal operation.	D
OUT	3	Device cycles in and out of thermal shutdown depending upon input voltage. Short circuit current limit triggers to clamp output current.	B
GND (TAB)	4	No effect. Normal operation.	D

Table 4-15. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Device not powered. Device not functional.	B
GND	2	No low impedance loop for current to flow, device is inoperable and absolute maximum condition violations are possible.	A, B
OUT	3	Power not driven to load. Device is unloaded.	D
GND (TAB)	4	Thermal performance degradation. Device functions but thermals are heavily impacted.	C

Table 4-16. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	GND	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A
GND	2	OUT	Device cycles in and out of thermal shutdown depending upon input voltage. Short circuit current limit triggers to clamp output current.	B

Table 4-17. Pin FMA for Device Pins Short-Circuited to IN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
GND	2	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A
OUT	3	Device shuts off as OUT is now higher than setpoint. Output is no longer regulated.	B
GND (TAB)	4	Device not powered. Device not functional. Absolute maximum voltages can potentially permanently damage the device.	A

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