Functional Safety Information

TPS7B85-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPS7B85-Q1 (VSON package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

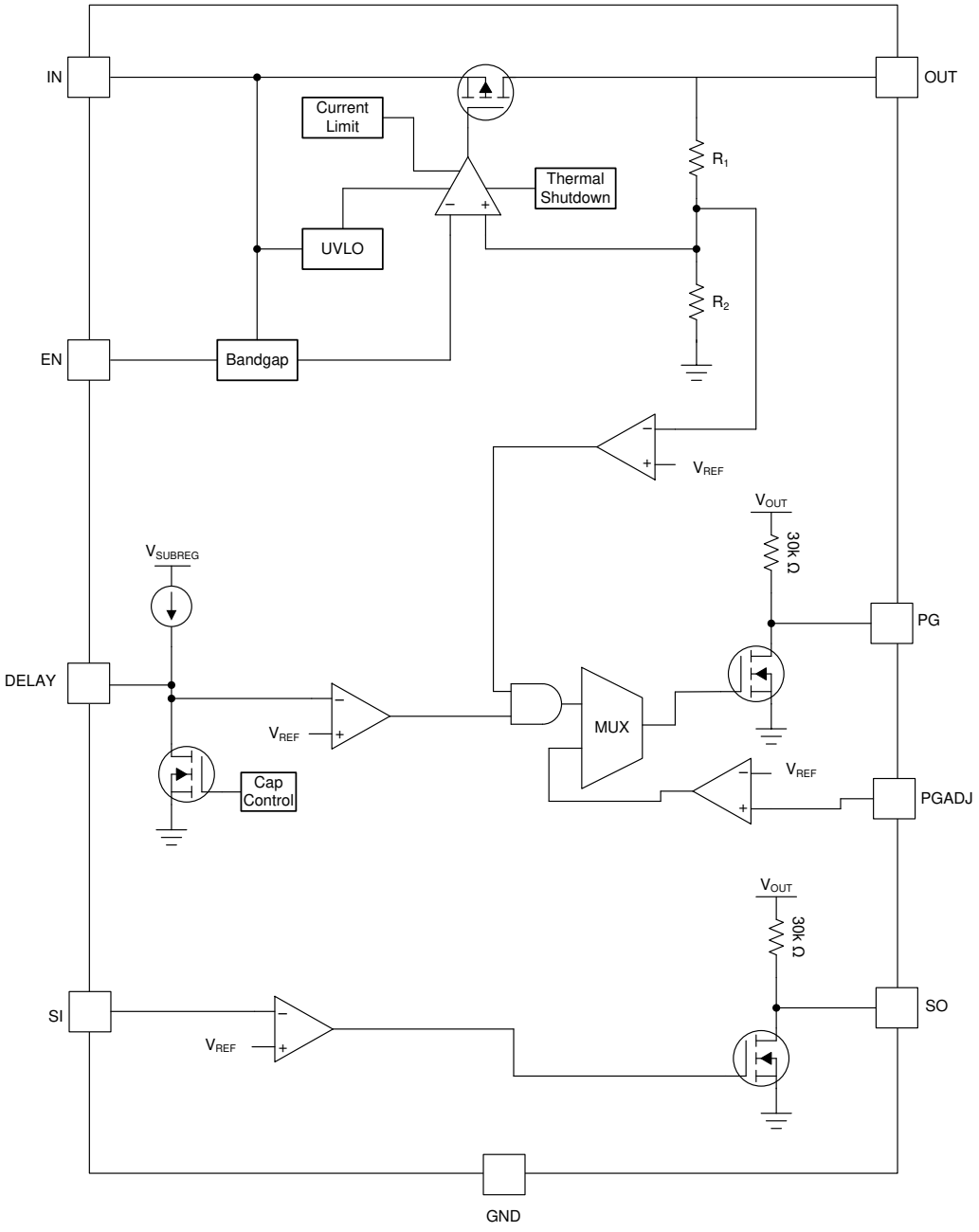

Figure 1-1. Functional Block Diagram

The TPS7B85-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS7B85-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10
Die FIT rate	6
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS and BICMOS ASICs, analog and mixed ≤ 50-V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B85-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
V_{OUT} high (following V_{IN})	40
V_{OUT} low (no output)	40
Short any two pins	10
V_{OUT} not in specification (voltage or timing)	5
PG false trigger, fails to trigger	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B85-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS7B85-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B85-Q1 data sheet.

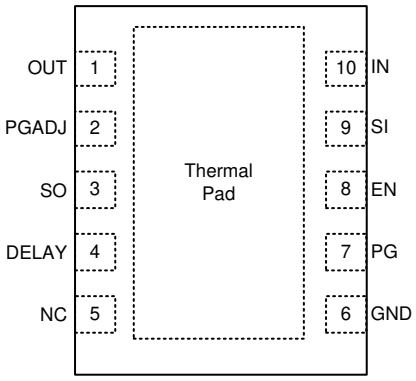

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Output voltage is at or near ground. The device is in current limit. The device can cycle in and out of thermal shutdown depending on power dissipation.	B
PGADJ	2	The PG threshold is set to $V_{PG(TH,FALLING)}$.	B
SO	3	Ground current is increased.	B
DELAY	4	Ground current is increased.	B
NC	5	No effect. Normal operation.	D
GND	6	No effect. Normal operation.	D
PG	7	Ground current is increased.	B
EN	8	The device is always off.	B
SI	9	The SO output is always low.	B
IN	10	No input to the device. The output is off.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The load is not powered.	B
PGADJ	2	PG either trips normally or trips early. The state is indeterminate.	B
SO	3	The SO output loses functionality.	B
DELAY	4	The power-good delay is $t_{(DLY\_FIX)}$.	C
NC	5	No effect. Normal operation.	D
GND	6	There is no current loop for internal biasing, so the device cannot function.	B
PG	7	The PG output is not accessible.	B
EN	8	The device state is unknown. The device can be on or off.	B
SI	9	SO output is unreliable. Ground current can be increased if SO output is pulled low due to the floating SI input.	B
IN	10	No input. The output is at ground.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	PGADJ	The PG output asserts at $V_{OUT} = V_{PGADJ(TH,FALLING)} + V_{PGADJ(HYST)}$. Damage is possible if V_{OUT} exceeds the PGADJ absolute maximum rating.	B/A
PGADJ	2	SO	If SO is logic high, the PG output asserts at $V_{OUT} = V_{PGADJ(TH,FALLING)} + V_{PGADJ(HYST)}$. If SO is logic low, PG asserts at the default output voltage ratio.	B
SO	3	DELAY	If SO never asserts, PG cannot assert. If SO asserts and V_{OUT} < DELAY (absolute maximum), the delay function is overridden and the default delay is used. Damage is possible if V_{OUT} exceeds the DELAY absolute maximum rating.	B/A
DELAY	4	NC	No effect. Normal operation.	D
GND	6	PG	PG functionality is lost and ground current increases.	B
PG	7	EN	PG functionality is lost. If EN is pulled low by PG, the device turns off. If $V_{EN} > V_{OUT}$, the device is not loaded, and $V_{OUT} > V_{PG(TH,RISING)}$, V_{OUT} charges to V_{EN}. Damage is possible if $V_{EN} > V_{PG}$ (absolute maximum).	B/A
EN	8	SI	The device state (ON/OFF) depends on the voltage at SI, or the SI/SO circuit depends on voltage at EN, depending on which supply has a stronger driving capability to the EN and SI pins.	B
SI	9	IN	SO is always high.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible. $V_{OUT} = V_{IN}$.	B
PGADJ	2	PG asserts after the power-good delay period has expired, causing a false power-good signal. PGADJ can be damaged if V_{IN} exceeds the absolute maximum rating for PGADJ.	B/A
SO	3	When there is a low-load condition, V_{OUT} can charge to V_{IN}. SO can be damaged if V_{IN} exceeds the absolute maximum rating for SO.	B/A
DELAY	4	There is no PG delay. PG trips when the output gets to the target with no delay.	B
NC	5	No effect. Normal operation.	D
GND	6	No input to the device. The output is off.	B
PG	7	When there is a low-load condition, V_{OUT} can charge to V_{IN}. SO can be damaged if V_{IN} exceeds the absolute maximum rating for SO.	B/A
EN	8	The device is always on when $V_{IN} > V_{UVLO(RISING)}$.	B
SI	9	The SO output is a function of only V_{IN}, $V_{SI(HIGH)}$, and $V_{SI(LOW)}$.	B
IN	10	No effect. Normal operation.	D

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265