Functional Safety Information

TPS4800-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS4800-Q1 (VSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

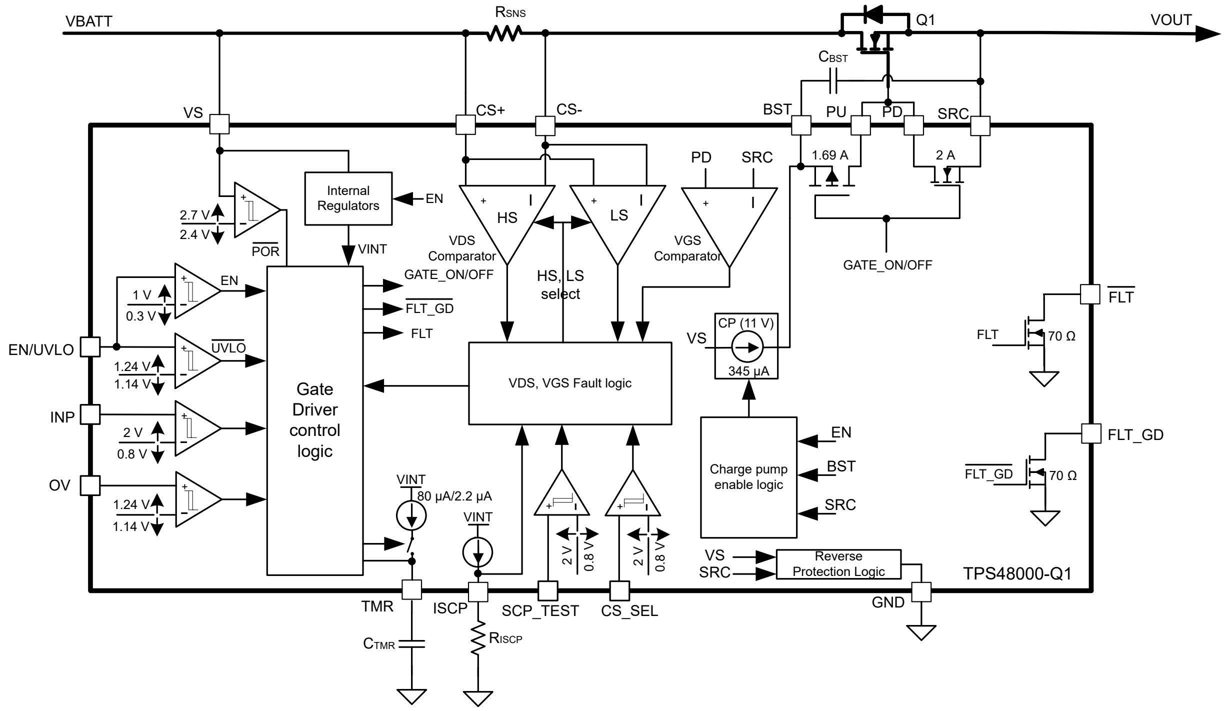

Figure 1-1. Functional Block Diagram

TPS4800-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFOMRATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS4800-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	9
Die FIT Rate	3
Package FIT Rate	6

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 0.6 mW
- Climate type: World-wide Table 8 IEC TR 62380
- Package factor (lambda 3): Table 17b IEC TR 62380
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS4800-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Gate output stuck high	10%
Gate output stuck low	45%
Gate output functional, not in specification voltage or timing	34%
Short circuit protection fails to trip or false trip	5%
UVLO fails to trip or false trip	1%
Pin to Pin short any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS4800-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS4800-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS4800-Q1 data sheet.

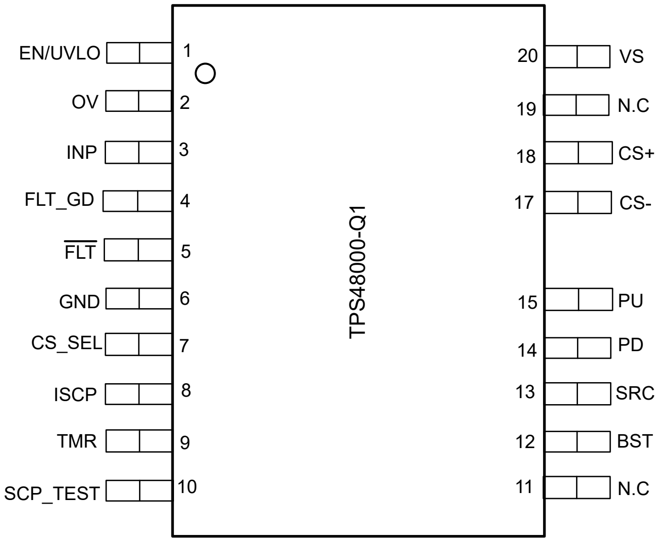

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follow data sheet recommendation for operating conditions, external component selection and PCB layout

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	Normal operation. The device is disabled.	B
OV	2	Normal operation. Overvoltage functionality is disabled.	B
INP	3	Normal operation. The PD output is low and the external FET is off.	B
FLT_GD	4	Charge pump UVLO fault diagnostic cannot be reported.	B
$\overline{\text{FLT}}$	5	Overcurrent, UVLO fault diagnostic cannot be reported.	B
GND	6	Normal operation	D
CS_SEL	7	Normal operation with current sensing configured for high side sensing.	B
ISCP	8	SCP threshold sets to minimum threshold.	B
TMR	9	Overcurrent does not get detected hence overcurrent protection is disabled.	B
SCP_TEST	10	Normal operation.	B
N.C	11	No effect. Normal operation.	D
BST	12	Gate Driver supply does not come up. FETs remain OFF.	B
SRC	13	Short to GND protection kicks in.	B
PD	14	With PD grounded, if the pin voltage between SRC and PD exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
PU	15	Gate Driver supply gets short circuited. FETs remain OFF.	B
CS-	17	Short to GND protection kicks in.	B
CS+	18	With CS+ grounded, if the pin voltage between CS+ and CS– exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
N.C	19	Normal operation.	D
VS	20	Device supply grounded. Device does not power up.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	Internal pulldown brings EN/UVLO to low disabling the device.	B
OV	2	Internal pulldown brings OV to low. Overvoltage functionality is disabled.	B
INP	3	Internal pulldown brings INP to low, pulling PD output low.	B
FLT_GD	4	Charge pump UVLO fault diagnostic cannot be reported.	B
FLT	5	Overcurrent, UVLO fault diagnostic cannot be reported.	B
GND	6	Device does not power up and is disabled.	B
CS_SEL	7	Internal pulldown brings CS_SEL to low, resulting in normal operation with current sensing configured for high side sensing.	B
ISCP	8	SCP threshold sets to maximum threshold.	B
TMR	9	Overcurrent response time and auto-retry duration gets reduced to device minimum setting.	C
SCP_TEST	10	Internal pulldown brings CS_SEL to low, resulting in normal operation.	B
N.C	11	No effect. Normal operation.	D
BST	12	External FET can get turned ON and OFF repetitively due to no capacitor connection at BST pin.	B
SRC	13	The external FET does not turned OFF as the FET source got disconnected from the internal pulldown driver.	B
PD	14	The external FET does not turn OFF as the FET GATE disconnects from the internal pulldown driver.	B
PU	15	The external FET does not turn OFF as the FET GATE disconnects from the internal pulldown driver.	B
CS-	17	CS- gets internally clamped to CS+ minus 2 diode drops. If ISCP feature is used, then the external FET may not turn ON due to false over current detection.	B
CS+	18	ISCP feature will not work.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
N.C	19	Normal operation.	D
VS	20	Device does not get powered up and is disabled.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	2 (OV)	If EN/UVLO is driven high then OV also gets detected high making the device PD pulled low to SRC and external FET gets disabled.	B
OV	2	3 (INP)	If INP is driven high then OV also gets detected high making the device PD pulled low to SRC and external FET gets disabled.	B
INP	3	4 (FLT_GD)	Charge pump UVLO fault diagnostic cannot be reported.	B
FLT_GD	4	5 (FLT)	Overcurrent, UVLO, Charge pump UVLO fault diagnostic cannot be reported.	B
FLT	5	6 (GND)	Overcurrent, UVLO fault diagnostic cannot be reported.	B
GND	6	7 (CS_SEL)	Normal operation. Device gets configured for high side sensing.	B
CS_SEL	7	8 (ISCP)	With CS_SEL grounded then SCP threshold sets to minimum threshold. With CS_SEL pulled high then SCP threshold sets to maximum threshold.	C
ISCP	8	9 (TMR)	TMR and ISCP thresholds get affected. External FET shuts off at a different threshold than set by ISCP. During an overcurrent fault the device is in Latch-off mode if ISCP has a < 100 kΩ resistor.	C
TMR	9	10 (SCP_TEST)	SCP_TEST feature gets disabled.	B
N.C	11	12 (BST)	No effect. Normal operation.	D
BST	12	13 (SRC)	Gate drive supply gets shorted and external FETs do not turn ON.	B
SRC	13	14 (PD)	Shorting of the pulldown switch (between PD and SRC) of the internal gate driver. External FET remains OFF.	B
PD	14	15 (PU)	Turn ON and OFF speeds of the external FETs can get impacted.	C
CS-	17	18 (CS+)	Bypasses the external current sense resistor or FET VDS sensing based on application circuit. SCP features get disabled.	B
CS+	18	19 (N.C)	Normal operation.	D
N.C	19	20 (VS)	Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	EN/UVLO pin is supply rated. Device remains enabled.	B
OV	2	OV pin is supply rated. PD remains pulled low to SRC due to overvoltage fault.	B
INP	3	INP pin is supply rated and will be treated driven high.	B
FLT_GD	4	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
FLT	5	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
GND	6	Supply power is bypassed and device does not turn on.	B
CS_SEL	7	CS_SEL pin is supply rated. Device gets configured for low side current sensing.	B
ISCP	8	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
TMR	9	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
SCP_TEST	10	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
N.C	11	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
BST	12	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
SRC	13	Output stuck on to supply	B
PD	14	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
PU	15	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
CS-	17	In the application, the external sense resistor or FET VDS sensing gets bypassed. short circuit protection will not work.	A
CS+	18	No effect. Normal operation.	D
N.C	19	No effect. Normal operation.	D
VS	20	No effect. Normal operation.	D

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