Functional Safety Information

TPS552872-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPS552872-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagrams for reference.

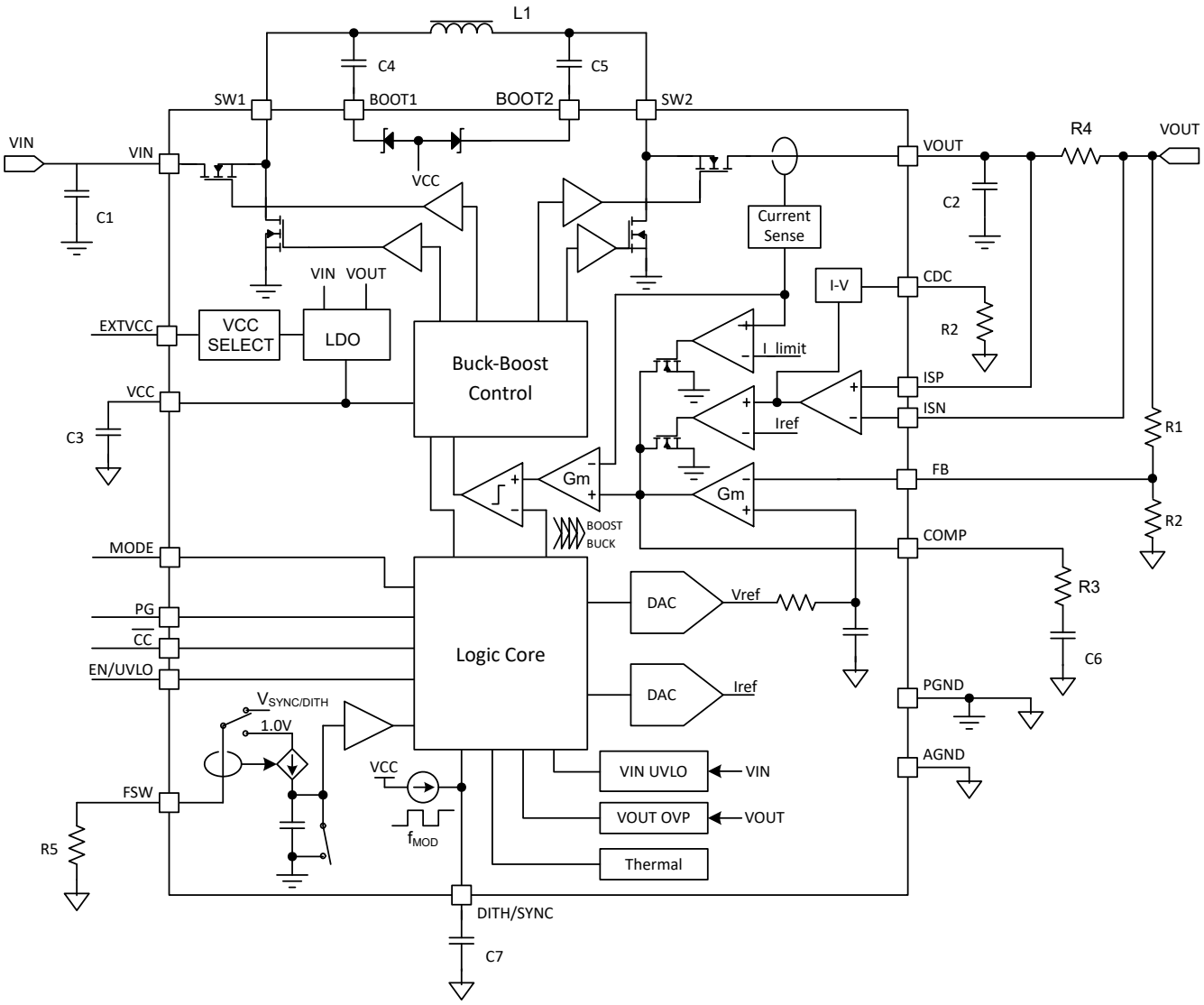

Figure 1-1. TPS552872-Q1 Functional Block Diagram

The TPS552872-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TPS552872-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	25
Die FIT Rate	9
Package FIT Rate	16

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS552872-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VO not in specification voltage or timing	50%
VO No output GND or HIZ	12.5%
SW FETs stuck on	30%
EN enable fails or false enable	2.5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS552872-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS552872-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS552872-Q1 data sheet.

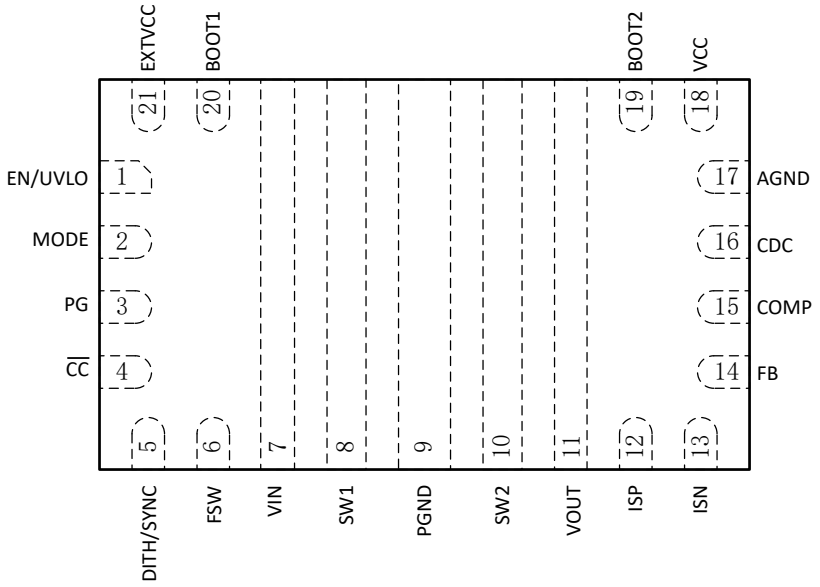

Figure 4-1. TPS552872-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* in the TPS552872-Q1 data sheet.
- The configuration is as shown in the *Application and Implementation* section found in the TPS552872-Q1 data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	Loss of ENABLE functionality. The device remains in shutdown mode.	B
MODE	2	The device works in auto PFM mode, loss of forced PWM functionality.	C
PG	3	Correct output voltage. Loss of power-good indication functionality.	C
$\overline{CC}$	4	Correct output voltage. Loss of constant current output indication functionality.	C
DITH/SYNC	5	Correct output voltage. Loss of DITH/SYNC functionality.	C
FSW	6	Possible device damage.	A
VIN	7	The device does not operate. Power supply is short.	B
SW1	8	Possible device damage.	A
PGND	9	No effect.	D
SW2	10	Possible device damage.	A
VOUT	11	The device remains in hiccup output short circuit protection mode.	B
ISP	12	The device remains in hiccup output short circuit protection mode.	B
ISN	13	No output voltage.	B
FB	14	Out rises to 23.5 V until output overvoltage protection is triggered.	B
COMP	15	The output voltage is out of regulation.	B
CDC	16	Loss of the cable voltage droop compensation functionality and the output voltage is overcompensated.	B
AGND	17	The internal circuited can be disturbed.	C
VCC	18	The device does not operate. VCC is short.	B
BOOT2	19	No output voltage.	B
BOOT1	20	No output voltage.	B
EXTVCC	21	The device selects the external power supply to supply the device through the VCC pin. If there is no external 5-V rail supplying VCC, the device does not operate and output is 0 V. If there is external 5-V rail supplying VCC, no effect on device operating.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	No output voltage. Loss of ENABLE functionality.	B
MODE	2	Correct output voltage. But working mode is not fixed.	C
PG	3	Correct output voltage. Loss of power-good indication functionality.	C
$\overline{CC}$	4	Correct output voltage. Loss of constant current output indication functionality.	C
DITH/SYNC	5	Correct output voltage. Loss of DITH/SYNC functionality.	C
FSW	6	No output voltage.	B
VIN	7	The device does not work and there is no output voltage.	B
SW1	8	Possible device damage.	A
PGND	9	Possible device damage.	A
SW2	10	Possible device damage.	A
VOUT	11	Possible device damage.	A
ISP	12	No output voltage.	B
ISN	13	The output voltage is out of regulation.	B
FB	14	OVP is triggered.	B
COMP	15	Output voltage is out of regulation.	B
CDC	16	Loss of CDC functionality and no cable voltage drop compensation.	C
AGND	17	Possible device damage.	A
VCC	18	Possible device damage.	A
BOOT2	19	Efficiency is lower.	B
BOOT1	20	Possible device damage.	A
EXTVCC	21	The device always selects internal LDO as VCC source. Loss of external VCC supply functionality.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	MODE	The MODE pin is damaged if EN/UVLO pin is higher than 6 V.	A
MODE	2	PG	Correct output voltage. Loss of MODE and PG functionality.	B
PG	3	$\overline{CC}$	Correct output voltage. Loss of PG and $\overline{CC}$ functionality.	C
$\overline{CC}$	4	DITH/SYNC	Correct output voltage. Loss of $\overline{CC}$ and DITH/SYNC functionality.	C
DITH/SYNC	5	FSW	Possible device damage.	A
FSW	6	VIN	The FSW pin is damaged if VIN pin is higher than 6 V.	A
VIN	7	SW1	Possible device damage.	A
SW1	8	PGND	Possible device damage.	A
PGND	9	SW2	Possible device damage.	A
SW2	10	VOUT	Possible device damage.	A
VOUT	11	ISP	Output current limit accuracy is affected.	C
ISP	12	ISN	Correct output voltage. Loss of output current limit functionality.	C
ISN	13	FB	Output voltage equals 1.2 V.	B
FB	14	COMP	Output voltage is out of regulation.	B
COMP	15	CDC	Output voltage is out of regulation.	B
CDC	16	AGND	Loss of the cable voltage droop compensation functionality and the output voltage is overcompensated.	B
AGND	17	VCC	The device does not operate. VCC is short.	B
VCC	18	BOOT2	The VCC pin is damaged if BOOT2 is higher than 6 V.	A
BOOT2	19	VOUT	Possible device damage.	A
BOOT1	20	VIN	Possible device damage.	A
BOOT1	20	EXTVCC	Possible device damage.	A
EXTVCC	21	EN/UVLO	EXTVCC pin is damaged if EN/UVLO pin is higher than 6 V.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	The EN/UVLO pin is damaged if supply voltage is higher than 20 V.	A
MODE	2	The MODE pin is damaged if supply voltage is higher than 6 V.	A
PG	3	The PG pin is damaged if supply voltage is higher than 6 V.	A
$\overline{CC}$	4	The $\overline{CC}$ pin is damaged if supply voltage is higher than 6 V.	A
DITH/SYNC	5	The DITH/SYNC pin is damaged if supply voltage is higher than 6 V.	A
FSW	6	The FSW pin is damaged if supply voltage is higher than 6 V.	A
VIN	7	No effect.	D
SW1	8	Possible device damage.	A
PGND	9	The device does not operate. Power supply is short.	B
SW2	10	The device is damaged if supply voltage is higher than 25 V.	A
VOUT	11	The VOUT pin is damaged if supply voltage is higher than 25 V. The output voltage is equal to the supply voltage.	A
ISP	12	The ISP pin is damaged if supply voltage is higher than 25 V. The output voltage is equal to the supply voltage.	A
ISN	13	The ISN pin damaged if supply voltage is higher than 25 V. The output voltage is equal to the supply voltage.	A
FB	14	The FB pin is damaged if supply voltage is higher than 6 V.	A
COMP	15	The COMP pin is damaged if supply voltage is higher than 6 V.	A
CDC	16	The CDC pin is damaged if supply voltage is higher than 6 V.	A
AGND	17	The device does not operate. Power supply is short.	B
VCC	18	The VCC pin is damaged if supply voltage is higher than 6 V.	A
BOOT2	19	The BOOT2 pin is damaged if supply voltage is higher than 31 V.	A
BOOT1	20	Possible device damage.	A
EXTVCC	21	The EXTVCC pin is damaged if supply voltage is higher than 6 V.	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265