Functional Safety Information

OPA2377-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the OPA2377-Q1 (VSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

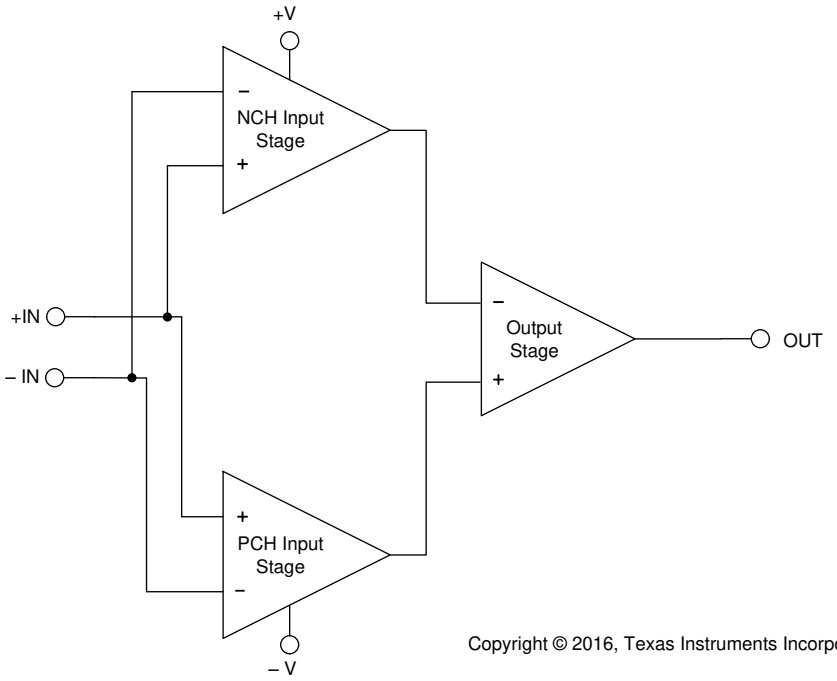

Figure 1-1. Functional Block Diagram

The OPA2377-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the OPA2377-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	2
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 10.45 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	CMOS, BICMOS Digital, analog, or mixed	12 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the OPA2377-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	30%
Output saturate low	25%
Output saturate high	25%
Output functional, not in specification voltage or timing	20%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the OPA2377-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the OPA2377-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the OPA2377-Q1 data sheet.

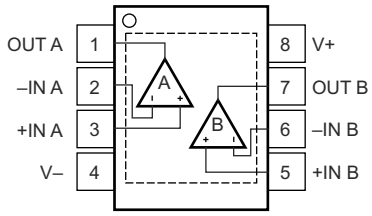

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- 'Short circuit to Power' means to V+ supply.
- 'Short circuit to GND or Ground' means to V– supply.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	Depending on circuit configuration, device will likely be forced into short circuit condition with OUT A voltage ultimately forced to V– voltage. Prolonged exposure to short circuit conditions could result in long term reliability issues.	A
–IN A	2	Negative feedback not present to device. Depending on circuit configuration, output will most likely move to negative supply.	B
+IN A	3	Device common–mode tied to negative rail. Depending on circuit configuration, output will likely not respond due to the device being put in an invalid common–mode condition.	C
+IN B	5	Device common–mode tied to negative rail. Depending on circuit configuration, output will likely not respond due to the device being put in an invalid common–mode condition.	C
–IN B	6	Negative feedback not present to device. Depending on circuit configuration, output will most likely move to negative supply.	B
OUT B	7	Depending on circuit configuration, device will likely be forced into short circuit condition with OUT B voltage ultimately forced to V– voltage. Prolonged exposure to short circuit conditions could result in long term reliability issues.	A
V+	8	Op–Amp supplies will be shorted together leaving V+ pin at some voltage between V+ and V– sources (depending on source impedance).	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	No negative feedback or ability for OUT A to drive application.	B
–IN A	2	Inverting pin of Op–Amp left floating. Negative feedback will not be provided to device, likely resulting in device output moving between positive and negative rail. –IN A pin voltage will likely end up at positive or negative rail due to leakage on ESD diodes.	B
+IN A	3	Input common–mode left floating. Op–Amp will not be provided with common–mode bias, device output will likely end up at positive or negative rail. +IN A pin voltage will likely end up at positive or negative rail due to leakage on ESD diodes.	B
V–	4	Negative supply left floating. Op–Amp will cease to function as no current can source/sink to the device.	A
+IN B	5	Input common–mode left floating. Op–Amp will not be provided with common–mode bias, device output will likely end up at positive or negative rail. +IN B pin voltage will likely end up at positive or negative rail due to leakage on ESD diodes.	B
–IN B	6	Inverting pin of Op–Amp left floating. Negative feedback will not be provided to device, likely resulting in device output moving between positive and negative rail. –IN B pin voltage will likely end up at positive or negative rail due to leakage on ESD diodes.	B
OUT B	7	No negative feedback or ability for OUT B to drive application.	B
+V	8	Positive supply left floating. Op–Amp will cease to function as no current can source/sink to the device.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	–IN A	Depending on circuit configuration, gain of circuit will be reduced to unity gain and application may not function as intended	B
–IN A	2	+IN A	Both inputs will be tied together. Depending on the offset of the device, this will likely move the output voltage near mid supply.	D
+IN A	3	V–	Device common–mode tied to negative rail. Depending on circuit configuration, output will likely not respond due to the device being put in an invalid common–mode condition.	C
V–	4	+IN B	Device common–mode tied to negative rail. Depending on circuit configuration, output will likely not respond due to the device being put in an invalid common–mode condition.	C
+IN B	5	–IN B	Both inputs will be tied together. Depending on the offset of the device, this will likely move the output voltage near mid supply.	D
–IN B	6	OUT B	Depending on circuit configuration, gain of circuit will be reduced to unity gain and application may not function as intended	B
OUT B	7	V+	Depending on circuit configuration, device will likely be forced into short circuit condition with OUT B voltage ultimately forced to V+ voltage. Prolonged exposure to short circuit conditions could result in long term reliability issues.	A
V+	8	OUT A	Depending on circuit configuration, device will likely be forced into short circuit condition with V+ voltage ultimately forced to OUT A voltage. Prolonged exposure to short circuit conditions could result in long term reliability issues.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	Depending on circuit configuration, device will likely be forced into short circuit condition with OUT A voltage ultimately forced to V+ voltage. Prolonged exposure to short circuit conditions could result in long term reliability issues.	AB
–IN A	2	Negative feedback not present to device. Depending on non–inverting input voltage and circuit configuration, output will most likely move to negative supply.	B
+IN A	3	Depending on circuit configuration, application will likely not function due to the device common–mode being connected to +IN A.	B
V–	4	Op–Amp supplies will be shorted together leaving V– pin at some voltage between V– and V+ sources (depending on source impedance).	A
+IN B	5	Depending on circuit configuration, application will likely not function due to the device common–mode being connected to +IN B.	B
–IN	6	Negative feedback not present to device. Depending on non–inverting input voltage and circuit configuration, output will most likely move to negative supply.	B
OUT B	7	Depending on circuit configuration, device will likely be forced into short circuit condition with OUT B voltage ultimately forced to V+ voltage. Prolonged exposure to short circuit conditions could result in long term reliability issues.	A

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