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# **Resetting Non-FIFO Variations of the 12-Bit THS1206**

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## **ABSTRACT**

The THS1207 and THS1209 are non-FIFO variations of the THS1206. They require some special procedures for properly resetting and configuring the device. This application brief helps explain the necessary steps required to get reliable data from these 12-bit, two and four channel simultaneous sampling data converters.

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## **1 Introduction**

The THS1207 and THS1209 are counterparts to the THS1206, 4 channels, 12-bit, simultaneous sampling, 6 MSPS analog to digital converter. Aside from sampling rate and channel count, the major difference in these parts is that the FIFO has been removed.

This application brief explains the necessary steps required to configure the device, as well as read reliable, consistent data.

## 2 Resetting the SYNC Generator

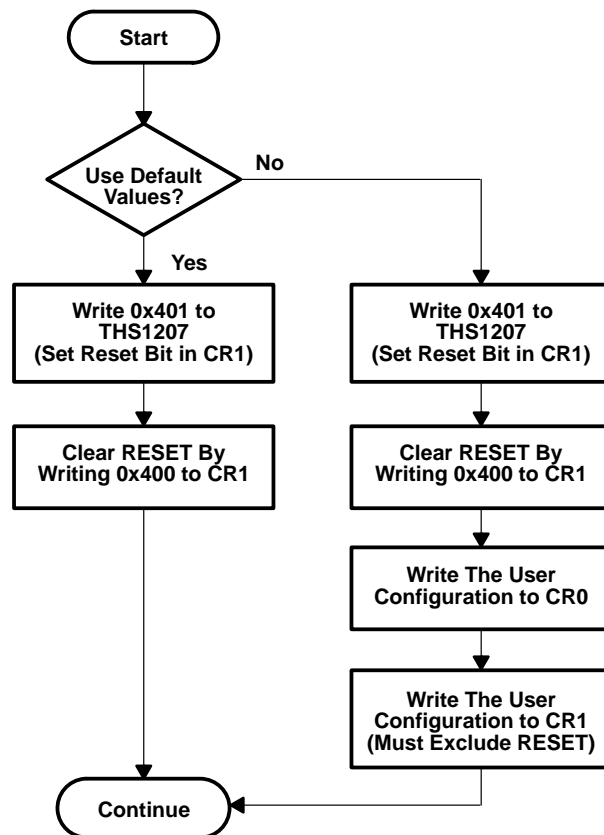
Bit 1 of configuration register 1 (CR1), must be considered the SYNC generator reset bit (SRST). This is similar to the THS1206 in that the THS1206 uses this bit to reset the FIFO to a known starting position. Similar results are possible by writing a 1 to CR1, bit 1, during the reset/configuration sequence of the THS1207 and THS1209.

This flow chart shows the initialization sequence of the THS1207. After power up, it is necessary to perform a device reset by writing hex values 0x401 and 0x400 to the device.

If the default configuration values are desired, there is no need to perform any additional writes to the device. The default value for configuration register 0 (CR0) is 0x020. The default value for CR1 is 0x010.

Because the default configuration values select single channel operation, the SYNC pulse is disabled, and there is no need to reset the SYNC generator.

If multiple channel operation is desired, it is necessary to set the SRST bit as part of the user configuration write to CR1 (CR1 bit 1 = 1). It is not necessary to clear the SRST bit once it has been set.



**Figure 1. THS1207 Configuration Flow**

### 3 Reading Data

Proper data readings depend on the proper application of the read signal. As with the THS1206, the THS1207 and THS1209 can be configured with independent, active low, read and write strobes. Active low CS0 and active high CS1 provide chip selection to the device and can be tied to static levels if desired.

With the non-FIFO devices, it is necessary to issue a read strobe after each CONV\_CLK. It is not appropriate to consider the SYNC pulse as an interrupt source to the host processor. The SYNC pulse is merely an indication that data currently available is the data acquired from channel one.

The read SYNC pulse is not available when the device is configured for single channel operation. The SYNC pulse is only active when two or more channels are selected for conversion during the initialization sequence.

Data setup times are listed in the data sheets as  $t_{su}(CONV\_CLK\_READL)$ . The read strobe must be applied after this setup time but before the subsequent falling CONV\_CLK edge. Failure to read the data bus within each conversion cycle, or multiple reads during the same conversion cycle, can cause the non-FIFO THS1207 and THS1209 SYNC pulse to behave erratically. Resetting BIT 1 of CR1 clears erratic SYNC pulse behavior.

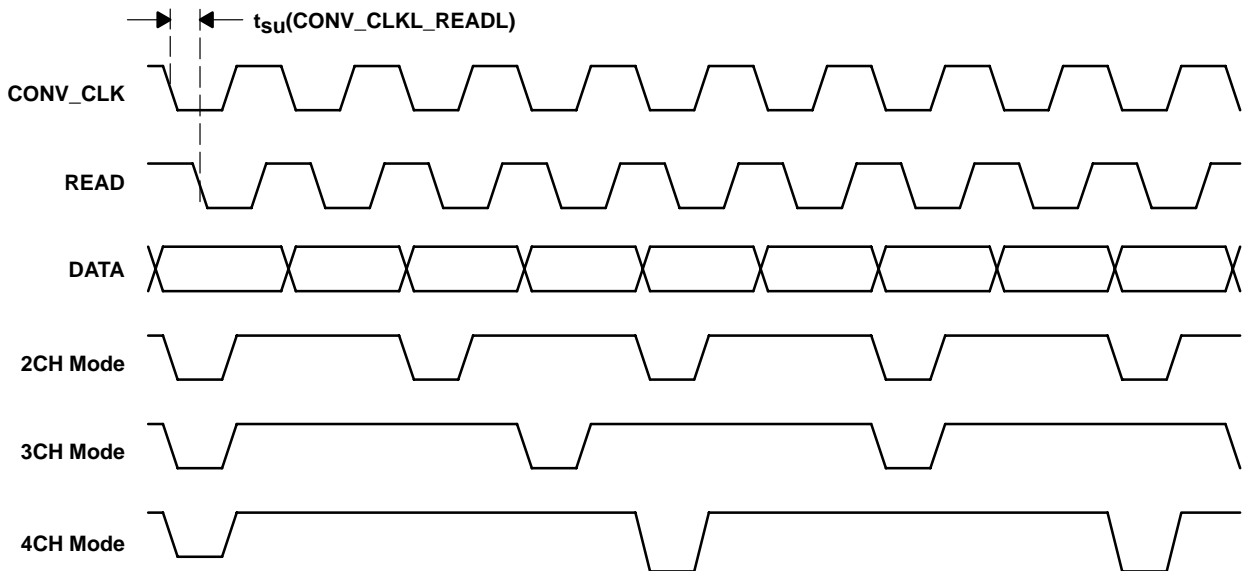


Figure 2. SYNC Pulse in 2, 3, and 4 Channel Modes

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