Application Report
SLAA565A–December 2012–Revised May 2015

Effects of Clock Spur on High-Speed DAC Performance

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ABSTRACT

High-speed digital-to-analog converters (DACs), synthesizer and clock distribution products are widely used in many applications, such as waveform generators, software defined radio, and modern wireless infrastructure equipment. While standards bodies or system specifications set boundaries for the DAC output performance requirement, very few researches discussed the effects of clock spur on DAC output performance. This application note introduces a model to illustrate the clock spur transfer characteristic, and reveals that the corresponding DAC spur is mixing components of DAC output signal and clock spur. For further validation of the model, some WCDMA signal tests are also made to show how clock spur deteriorates DAC ACPR performance and how to avoid this problem.

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1 Introduction

In this section, test circuits and test methods are introduced. Figure 1 shows test circuits used in this application note. The circuit consists of an RF signal generator, a spurious signal generator, a DAC3482 EVM and a TSW1400 EVM. The related part information is shown in Table 1.

In this system, the RF signal generator provides a 983.04-MHz, 5-dBm clock to CDCE62005 in DAC3482 EVM. The CDCE62005 is configured as a clock distributor. It divides the input clock and generates two outputs. One output is the OSTR clock used for DAC3482 synchronization. The other is the FPGA clock for TSW1400 EVM. The TSW1400 EVM generates DATA clock, pattern data and other control signals for digital blocks in the DAC3482. Another signal generator can generate a 983.04-MHz clock with spurs. This spurious clock injects to the DAC core in the DAC3482. Clock spur transfer characteristics can be derived by tracking the spur response in DAC output.

For determining the clock spur transfer characteristics, Section 2 gives single-tone test results under spurious clocks, and then analyzes clock signal flow within the DAC internal blocks. Based on test results and analysis, a clock spur transfer model is derived.

Through frequency plan analysis, Section 3Section 3 introduces a method to use the derived model in an application to avoid clock spur problems. Some WCDMA signal test results are shown in Section 3 illustrating how improper frequency plan causes ACPR degradation.

Section 4Section 4 summarizes the results and gives conclusions for this application note.

Table 1. Part and EVM Information

Part	Description
CDCE62005	5/10 Outputs Clock Generator/Jitter Cleaner with Integrated Dual VCO
DAC3482	2-channel, 16-bit, 1.25 GSPS Digital-to-Analog Converter
DAC3482 EVM	DAC3482 Evaluation Module
TSW1400 EVM	High Speed Data Capture and Pattern Generation Platform

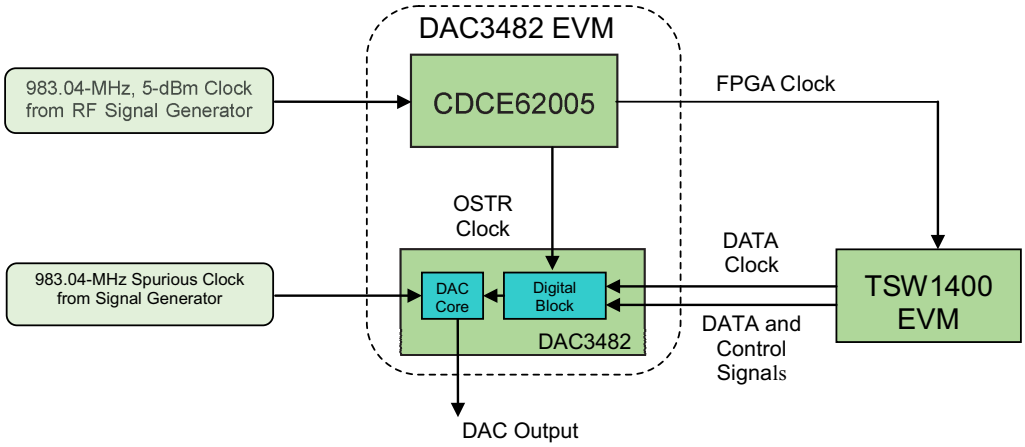

Figure 1. EVM Setup for Test

2 Clock Spur Transfer Model

Starting with an example, Figure 2 shows a 983.04-MHz clock with four spurs, and Figure 3 shows the corresponding single-tone DAC test result under this spurious clock. Table 2 shows the detailed spur information for both clock and DAC output.

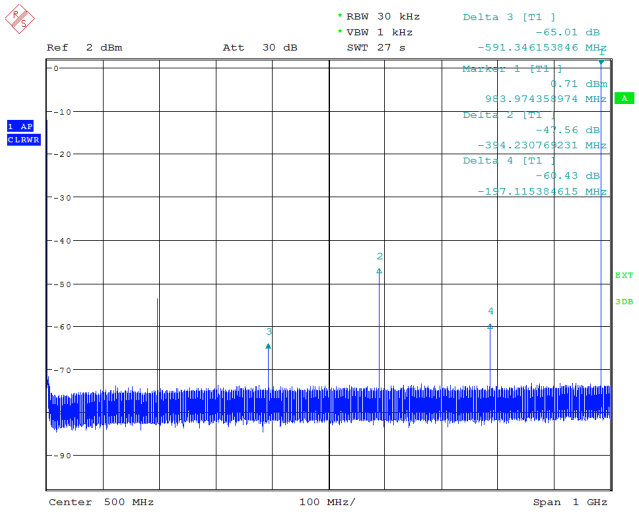

Figure 2. 983.04-MHz Clock with Four Spurs

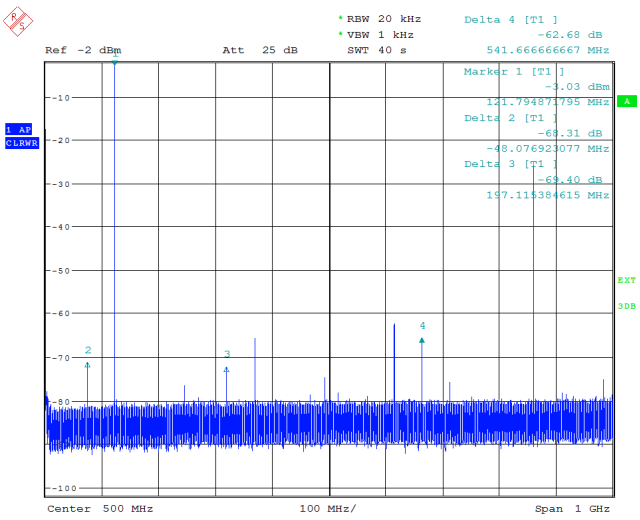

Figure 3. 122.88-MHz DAC Output Under the Spurious 983.04-MHz Clock

Table 2. Detailed Clock and DAC Output Spur Information

	Frequency MHz	Power dBc
Clock	983.04	0
DAC output	122.88	0
Clock spur	196.608	–54.27
	393.224	–64.32
	589.824	–47.63
	786.43	–60.52
DAC output spur	73.728	–68.09
	270.344	–79.4
	319.488	–70.59
	466.944	–78.14
	516.104	–77.65
	663.55	–63.3
	712.704	–73.6
	909.31	–78.02

The first issue needing discussion is whether clock spur is divided when 983.04-MHz clock is divided to form 122.88-MHz DAC output. Figure 4 shows the signal flow diagram for DAC3482. From this diagram, it is obvious that the dividing action happens in NCO. Since this NCO is a digital block which has immunity to clock spurs, the main influence of clock spur happens in the DAC core. The clock spur is not divided in transfer process because there is no clock divider in the DAC core.

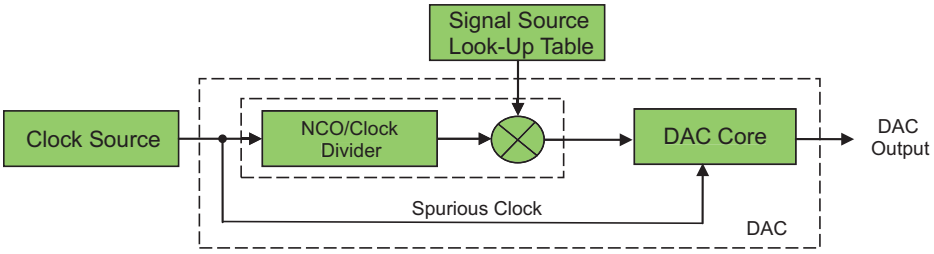

Figure 4. Signal Flow Diagram of DAC3482

The second issue is how to model the DAC core. The simplest way is assuming it as a sampling system, and then all the clock spurs can be treated as additive sampling clocks. The left side of Figure 5 shows this assumption. When f_{spur} is larger than f_{DAC_output}, then the resulted DAC output spur locates at (f_{spur} – f_{DAC_output}). For 196.608-MHz, 393.224-MHz, 589.824-MHz, and 786.43-MHz spurs in the test, the corresponding spurs should locate at 73.728 MHz, 270.344 MHz, 466.944 MHz and 663.55 MHz. However, according to Table 2 , there are still spurs located at 319.488 MHz, 516.104 MHz, 712.704 MHz, and 909.31 MHz. So, this assumption cannot illustrate all cases. Another way is assuming it as a mixer. This is because In Figure 4, the DAC core mixes the input signal and clock together to form output. The right side of Figure 5 shows this assumption. It can illustrate all the frequencies of DAC output spur in test. Table 3 shows the corresponding relationship between clock spur and the DAC output spur when DAC is modeled as a mixer.

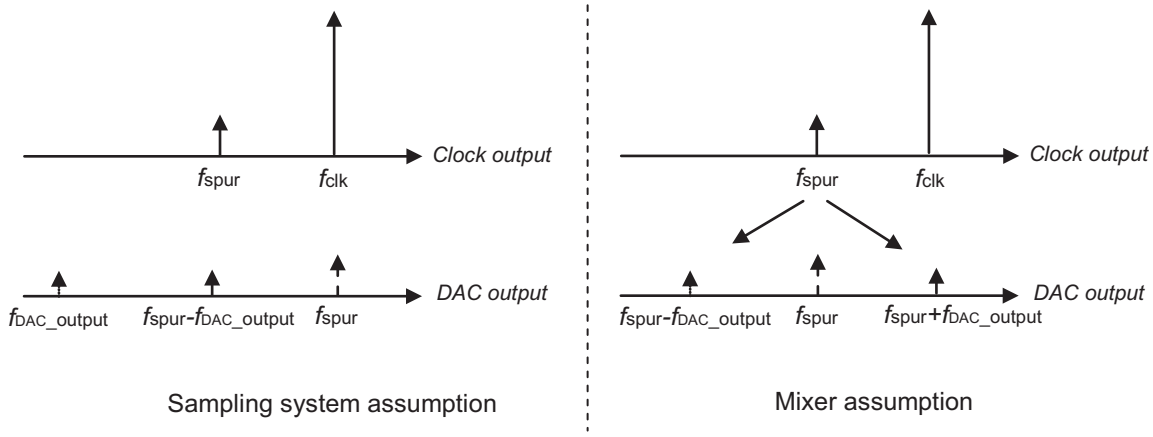

Figure 5. Using Two Assumptions to Illustrate the Test Results

Table 3. Clock Spurs and Corresponding DAC Output Spurs, DAC IF = 122.88 MHz

Clock Spur Frequency MHz	Clock Spur Power dBc	DAC Output Spur MHz	DAC Spur Power dBc
196.608	–54.27	73.728	–68.09
196.608	–54.27	319.488	–70.59
393.224	–64.32	270.344	–79.4
393.224	–64.32	516.104	–77.65
589.824	–47.63	466.944	–78.14
589.824	–47.63	712.704	–73.6
786.43	–60.52	663.55	–63.3
786.43	–60.52	909.31	–78.02

The assumption that considers the DAC core as a mixer illustrates output spur frequency, however, it cannot predict DAC spur power. For example, the strongest spur in Figure 6 is 589.824 MHz, and the power of this spur is –47.63 dBc. But the power of the corresponding 466.933-MHz DAC spur is only –78.14 dBc, which is much smaller than the DAC spur in 663.55 MHz (–63.3 dBc) caused by –60.52 dBc, 786.43-MHz clock spur. If the DAC is simply modeled as a mixer, then larger clock spur should result larger DAC output spur. Obviously, the test results are just opposite to this. The illustration for this phenomenon is that DAC is not a simple mixer, it has its own influence to clock spur. So the DAC output spur is determined by both clock spur and DAC internal mechanics.

Although the mixer assumption cannot precisely predict power of DAC output spur, it can still help designers locate DAC output spur frequency. Figure 6 shows the derived model based on mixer assumption. A mixer is modeled inside DAC core to illustrate that the DAC output is mixing component of spurious clock and DAC IF data. And a spur attenuator is introduced to model DAC internal mechanics which lower clock spur influence. Table 4 shows another example to further support this model. In this example, the clock is 983.04 MHz with six spurs, and the DAC output frequency is 122.88 MHz. All of the DAC output spurs can be predicted before test by the model shown in Figure 6.

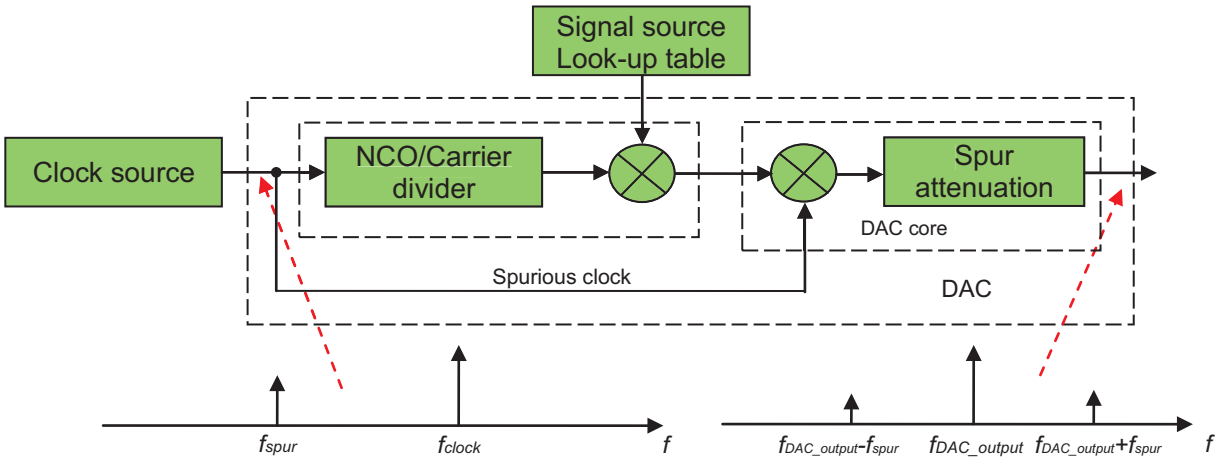

Figure 6. Clock Spur Transfer Model

Table 4. Example Supporting the Derived Model

Clock Spur Frequency MHz	Clock Spur Power dBc	DAC Output Spur MHz	DAC Spur Power dBc
140.434	–63.57	17.553	–75.28
140.434	–63.57	263.313	–78.71
280.873	–62.59	157.988	–94.14
280.873	–62.59	403.748	–95.83
421.304	–44.4	298.424	–78.33
421.304	–44.4	544.184	–76.59
561.736	–63.12	438.857	–77.69
561.736	–63.12	684.617	–71.06
702.168	–61.79	579.293	–92.09
702.168	–61.79	825.052	–96.1
842.607	–57.02	719.726	–81.04
842.607	–57.02	965.484	–94.67

Until now, the clock spur transfer characteristic is derived. Using the mixer assumption, and taking the DAC internal mechanics into account, the derived model can precisely predict frequency of DAC output spur caused by clock spur. But it cannot predict DAC output spur power. In application, it can help designers make spurious free frequency plan.

3 How to Avoid Clock Spurs at DAC Output

In this section, a method is introduced to show how to design a spurious free frequency plan. Also, some WCDMA test results are shown to illustrate how an improper frequency plan degrades DAC ACPR performance.

Assume that the DAC IF and bandwidth are set, designers can use the following method to optimize clock performance to avoid spur problem. According to the model shown in Figure 6, if DAC IF meets the following equation, DAC output may suffer from in-band spur problem or ACPR degradation.

$$IF - \frac{1}{2}BW \le \left| f_{clk\_spur} \pm f_{DAC\_output} \right| \le IF - \frac{1}{2}BW$$

$$IF - \frac{1}{2}BW_{channel} \le f_{DAC\_output} \le IF - \frac{1}{2}BW_{channel} \quad (1)$$

The BW (bandwidth) used in Equation 1 is shown in Figure 7. Notice that this BW is not only channel bandwidth, but a wider $BW_{alternate}$ which takes the adjacent channel and alternate channel ACPR into consideration. If using $BW_{channel}$ in Equation 1, designers can only avoid in-band spur problems while the DAC output spur may still lie in adjacent channels or alternate channels which may degrade ACPR. Using $BW_{alternate}$, designers can avoid both DAC in-band spur problems and ACPR degradation caused by clock spur.

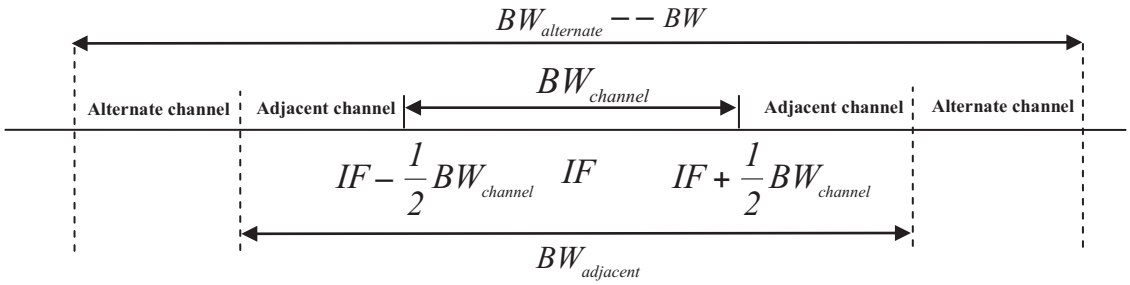

Figure 7. BW Used in Equation (1)

Solving Equation 1, the result is:

$$0 \le f_{clk\_spur} \le BW$$
$$2IF - BW \le f_{clk\_spur} \le 2IF + BW \quad (2)$$

Equation 2 means for fixed DAC IF and BW, clock spur performance must be optimized at the frequency range of (0, BW) and (2 × IF – BW, 2 × IF + BW) to avoid the in-band spur problem and ACPR degradation. It also means that clock spurs at other frequency ranges impose little influence on DAC output.

Assume another case that the clock is selected, according to Equation 2; the DAC IF should avoid the following range:

$$\frac{f_{clk\_spur} - BW}{2} \le IF \le \frac{f_{clk\_spur} + BW}{2} \quad (3)$$

Equation 3 means clock spurs can influence DAC IF selection. Figure 8 shows, when selecting an IF, designers should avoid the frequency ranges that may cause spur problem.

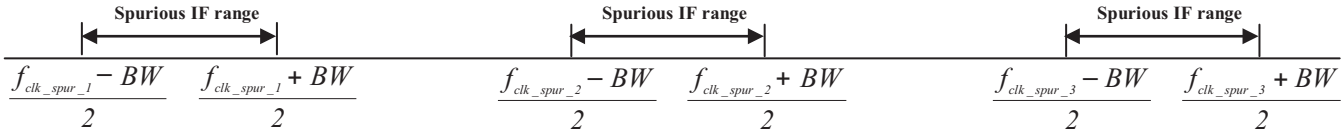

Figure 8. Avoid These IF Ranges That May Cause Spur Problem

To confirm Equation 2 and Equation 3, some tests are made with WCDMA signals. In these tests, the signal has single carrier, with 3.84 MCPS and 5-MHz bandwidth. When considering alternate channel ACPR, the BW = 5 × pattern bandwidth which equals 25 MHz. Figure 9 to Figure 12 show the different clocks used in the test. Figure 13 to Figure 28 show, with improper frequency planning, ACPR performance is degraded. For example, as Figure 14 shows, if the clock spur is 98.304 MHz, according to Equation 3, DAC IF should not locate at (36,652 MHz, 61.652 MHz). If the DAC IF is set to 51.652 MHz, ACPR performance is degraded by clock spur.

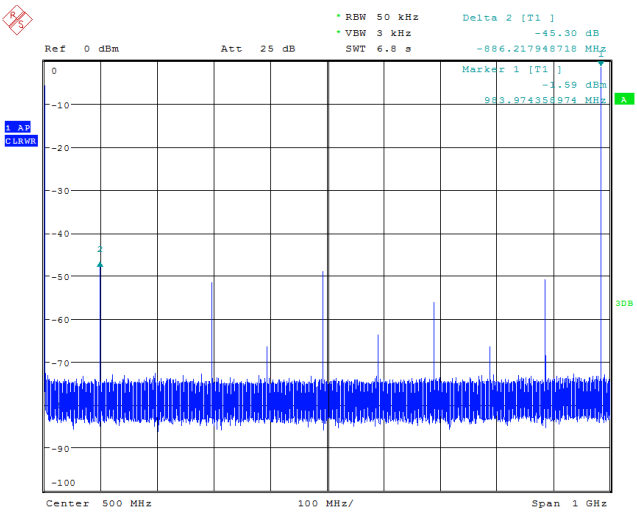

Figure 9. 983.04-MHz Clock With 98.304-MHz Spur

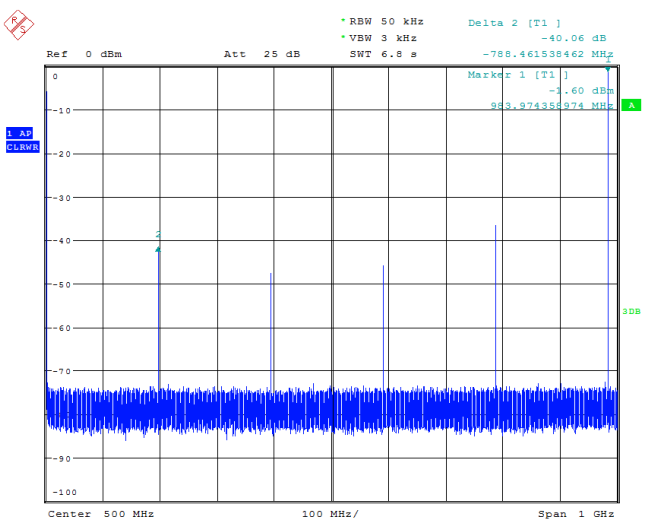

Figure 10. 983.04-MHz Clock With 196.608-MHz Spur

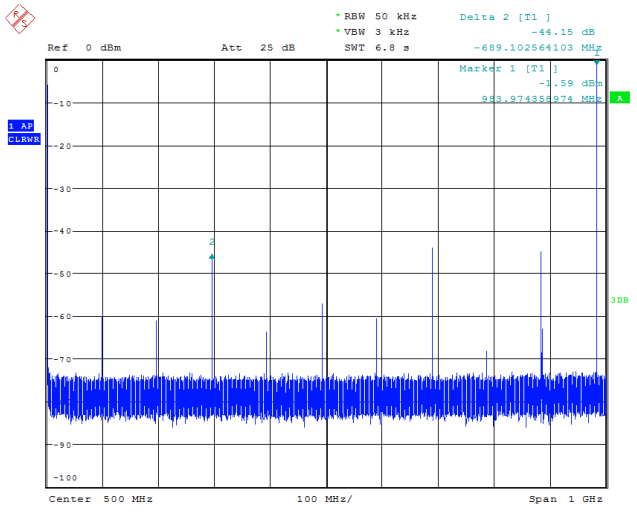

Figure 11. 983.04-MHz Clock With 294.912-MHz Spur

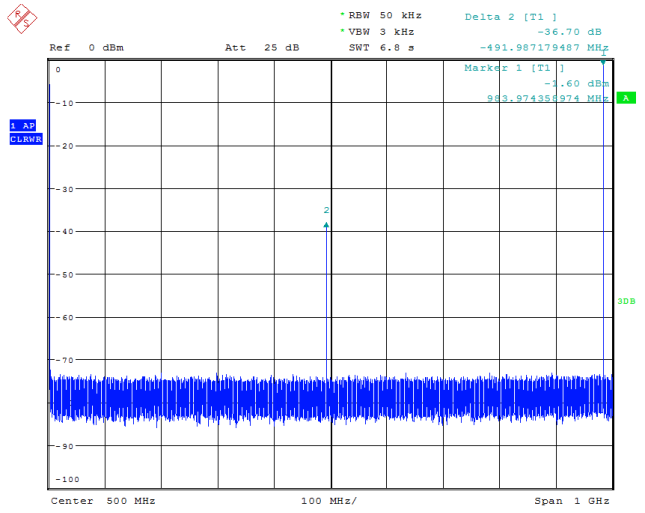

Figure 12. 983.04-MHz Clock With 491.52-MHz Spur

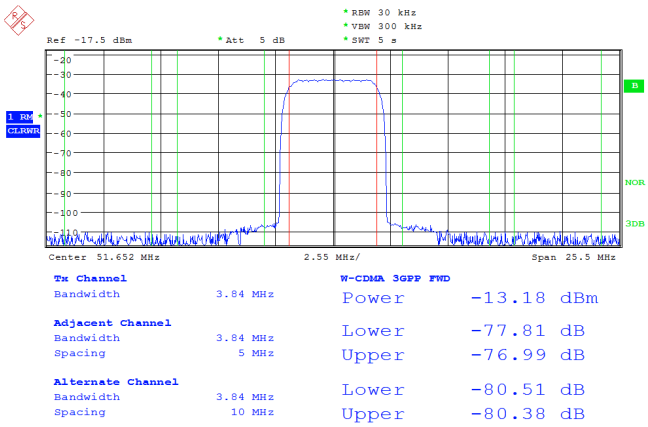

Figure 13. 51.652-MHz DAC Output Under Spurious Free Clock

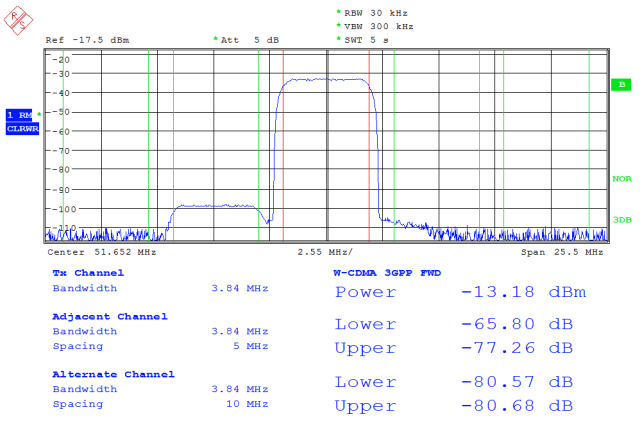

Figure 14. 51.652-MHz DAC Output, 98.304-MHz Clock Spur, Adjacent Channel

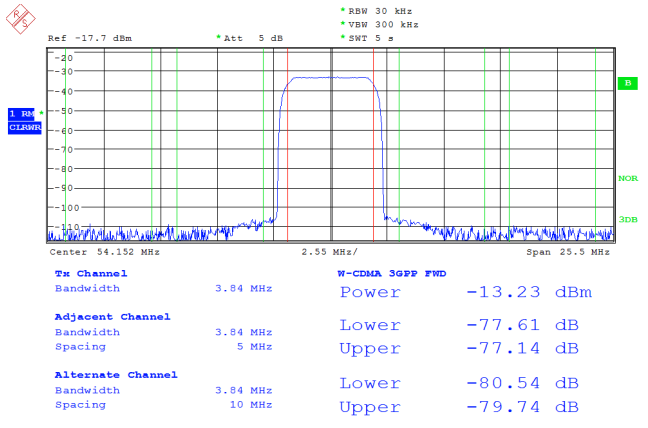

Figure 15. 54.152-MHz DAC Output Under Spurious Free Clock

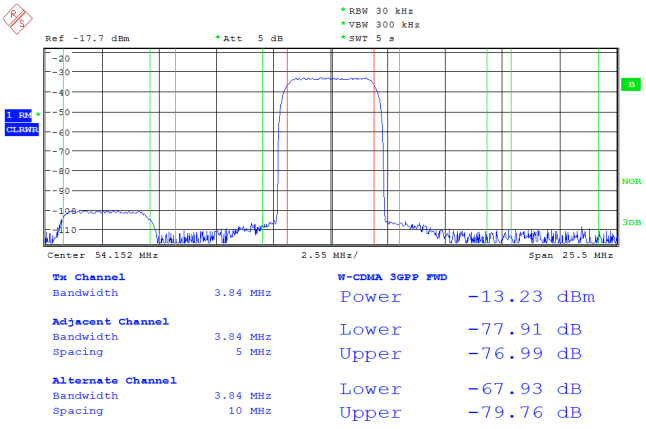

Figure 16. 54.152-MHz DAC Output, 98.304-MHz Clock Spur, Alternate Channel

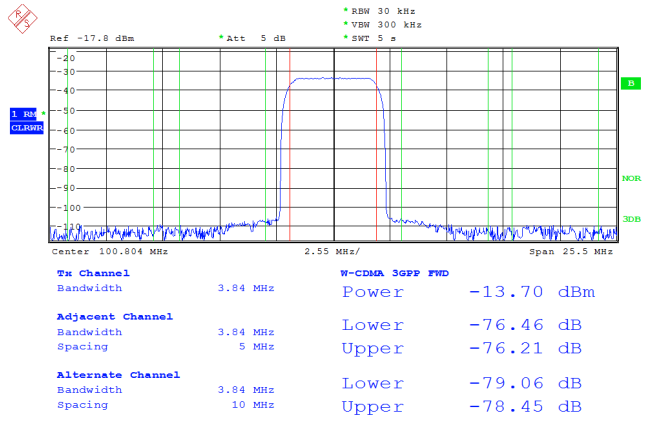

Figure 17. 100.804-MHz DAC Output Under Spurious Free Clock

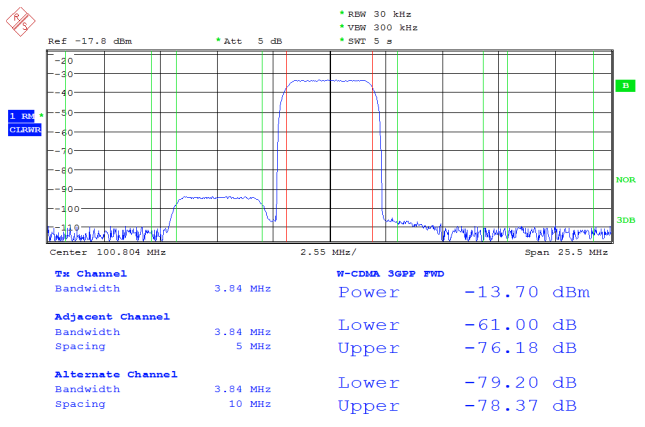

Figure 18. 100.804-MHz DAC Output, 196.608-MHz Clock Spur, Adjacent Channel

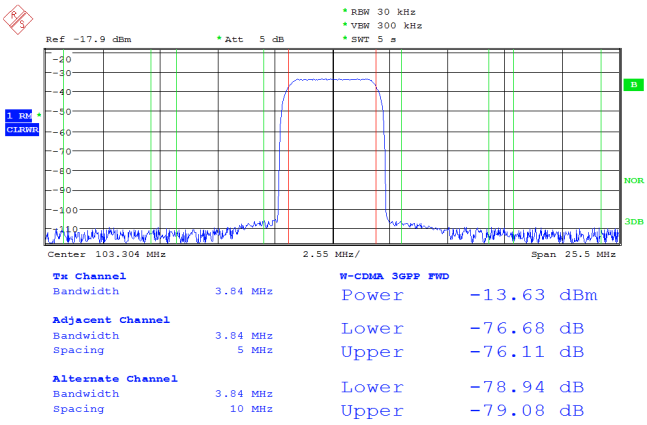

Figure 19. 103.304-MHz DAC Output Under Spurious Free Clock

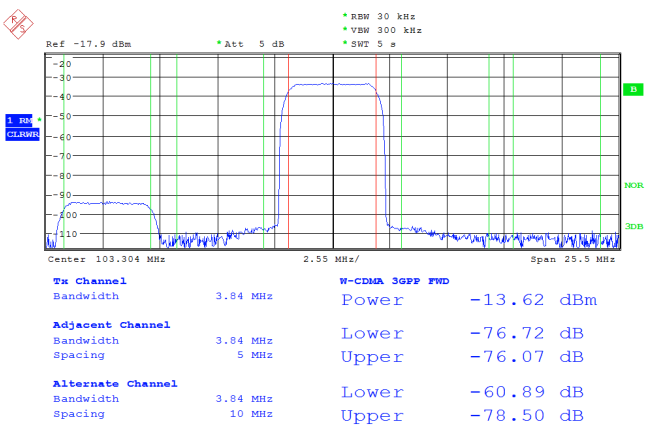

Figure 20. 103.304-MHz DAC Output, 196.608-MHz Clock Spur, Alternate Channel

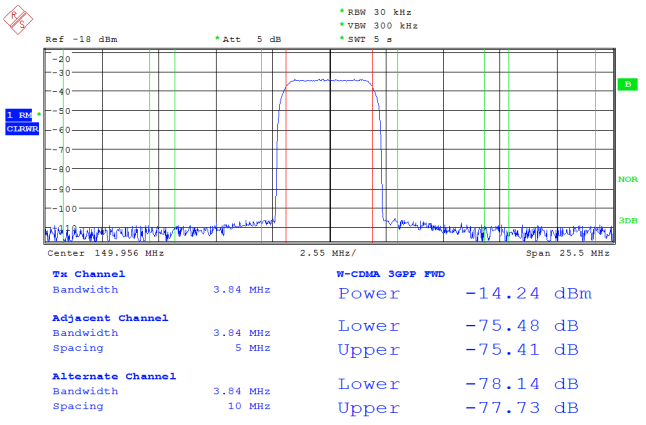

Figure 21. 149.956-MHz DAC Output Under Spurious Free Clock

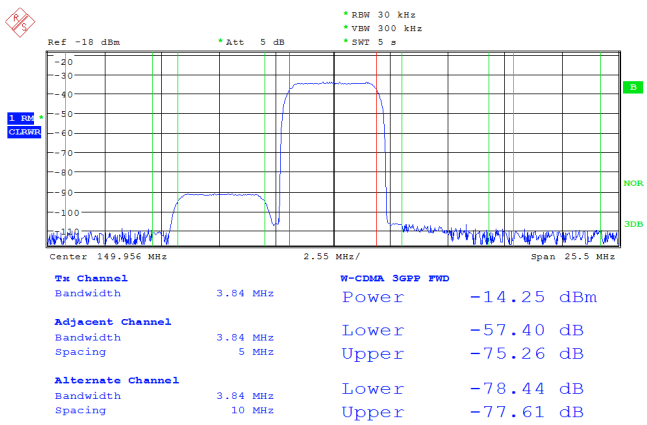

Figure 22. 149.956-MHz DAC Output, 294.912-MHz Clock Spur, Adjacent Channel

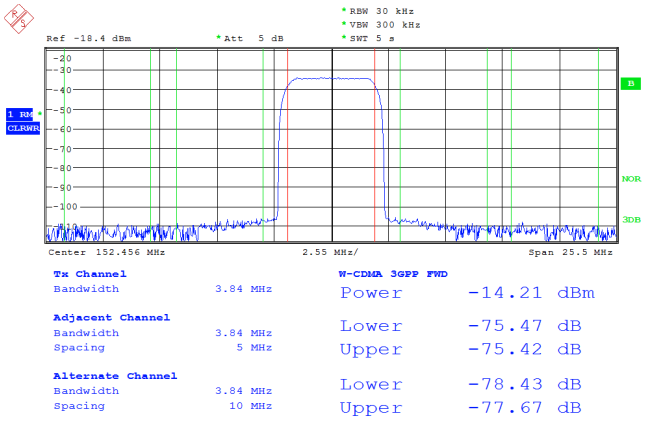

Figure 23. 152.456-MHz DAC Output Under Spurious Free Clock

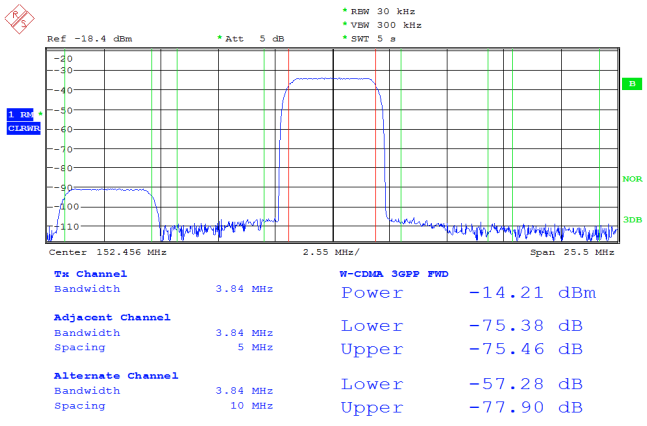

Figure 24. 152.456-MHz DAC Output, 294.912-MHz Clock Spur, Alternate Channel

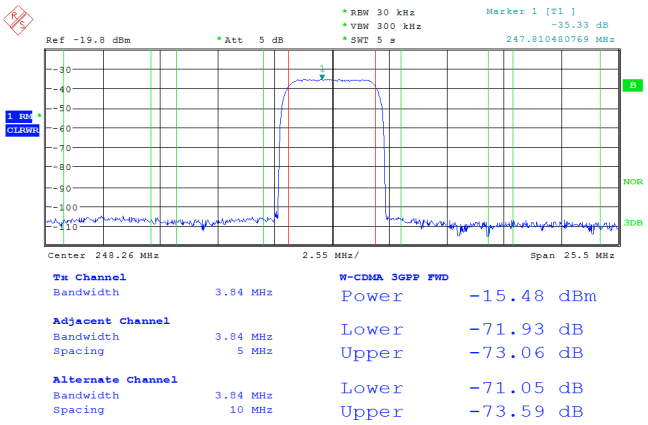

Figure 25. 248.26-MHz DAC Output Under Spurious Free Clock

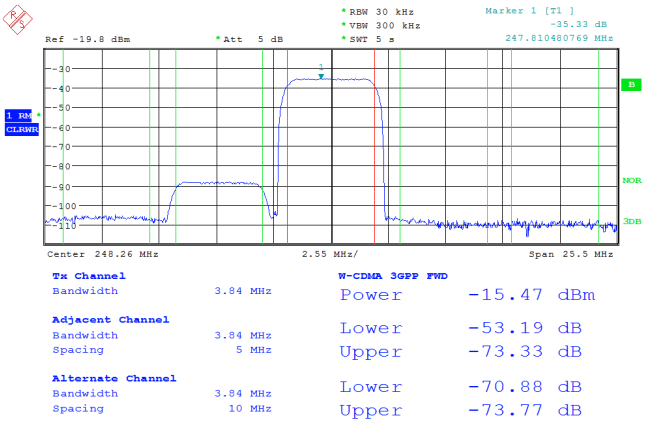

Figure 26. 248.26-MHz DAC Output, 491.52-MHz Clock Spur, Adjacent Channel

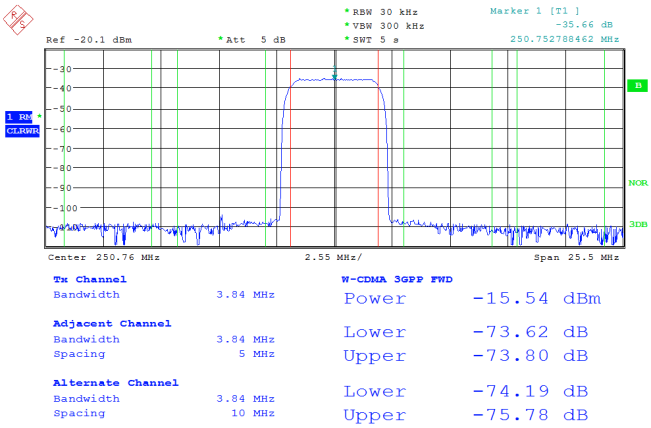

Figure 27. 250.76-MHz DAC Output Under Spurious Free Clock

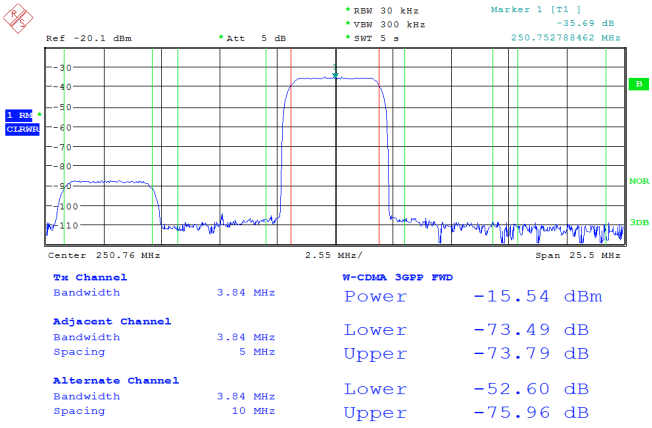

Figure 28. 250.76-MHz DAC Output, 491.52-MHz Clock Spur, Adjacent Channel

Until now, this section discusses two kinds of application examples which can help designers make spurious free frequency plan. When selecting the DAC IF, use Equation 2 to optimize clock spur performance. When selecting clock, use Equation 3 to avoid clock spur problems.

4 Conclusion

This application note discusses effects of clock spur on DAC performance. By analyzing DAC internal signal flow and some test results, a model for evaluating clock spur transfer characteristics is introduced. This model reveals that DAC output spur is mixing components of DAC output signal and clock spur. This model precisely predicts DAC output spur frequency caused by clock, but it cannot predict spur power. Designers can use this model and the derived equations to make spurious free frequency plan to avoid clock spur problems.

References

- DAC3482 datasheet, Texas Instruments Inc., 2011 (SLAS748D)
- DAC3482 EVM User's Guide, Texas Instruments Inc., 2012 (SLAU432)
- TSW140x High Speed Data Capture/Pattern Generator Card, Texas Instruments Inc., 2012 (SLWU079A)

Revision History

Changes from Original (December 2012) to A Revision	Page
• Changed format to current TI application report template.	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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