Application Report
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Eye Scan Testing With the DAC38RFxx

Kyle Addington *Wireless Infrastructure*

ABSTRACT

The DAC38RFxx family of devices comes equipped with the capability to generate eye diagrams by using JTAG communication with the DAC38RF8x eye scan GUI software. By running this software, users can generate eye diagrams to compare with the JESD204B standard eye mask requirements, and verify signal integrity performance of the SerDes link between DAC and FPGA/ASIC. This application report describes the required steps to create eye diagrams using the DAC38RFxx EVM and eye scan GUI.

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1 Testing Requirements

This test procedure requires the following pieces of hardware and software:

- DAC38RF8x EVM (or other DAC38RFxx custom board with access to the JTAG pins through a CMOS header)
- 5-V DC power supply
- Signal generator for clock supply
- USB to JTAG converter. (This example uses FTDI's USB 2.0 Hi-Speed to MPSSE 3.3V cable, http://www.ftdichip.com/Products/Cables/USBMPSSE.htm)
- Spectrum analyzer
- DAC38RF8x_EYE_SCAN GUI (request software through the Texas Instruments E2E™ online community)
- DAC38RF8x GUI

2 Hardware Setup

Follow this procedure to setup the hardware:

1. Connect TSW14J56 FMC Interface Connector (J4 of TSW14J56) to DAC38RF8x FMC Interface Connector (J20 of DAC38RF8x EVM).
2. Connect USB 2.0 Type A to Mini-B cable from the PC to DAC38RF8x EVM USB Mini-B port (J16) for programming
3. Connect USB 3.0 Type A to Type B cable from the PC to TSW14J56 Rev D USB 3.0 B port (J9)
4. Connect 5V power supply to the DAC38RF8x EVM board using J21.
5. Connect 5V power supply to the TSW14J56 board using J11.
6. Turn the TSW14J56 board on by moving switch SW6 to the ON position.
7. Configure signal generator for DAC clocking frequency. For external clocking mode, supply clocking frequency to DACCLKP SMA connector (J1) and install jumper J10 on the DAC38RF8x EVM. For onboard clocking, supply a clock signal to the LMK CLKIN SMA connector (J4) and remove jumper J10. The following procedures will be using the onboard clocking mode with a 364.68-MHz, 10-dBm clock signal applied to the LMK CLKIN SMA connector.
8. Connect DAC38RFxx JTAG pins to PC using FTDI's USB 2.0 Hi-Speed to MPSSE cable. If using the DAC38RFxx EVM (revision E and below), some soldering modifications must be made to access the JTAG connections. One way to access the DAC38RFxx JTAG pins is to remove resistors R173-R177 and connect a 5-pin CMOS header by running wires to the resistor pads. An example of this setup is shown in Figure 1.
9. To enable JTAG Communication the TRST pin must be toggled low and back high once after startup. The EVM board has an internal pullup on the TRST pin, so the pin can be toggled by momentarily attaching a jumper cable from ground to the header which corresponds to the TRST pin.

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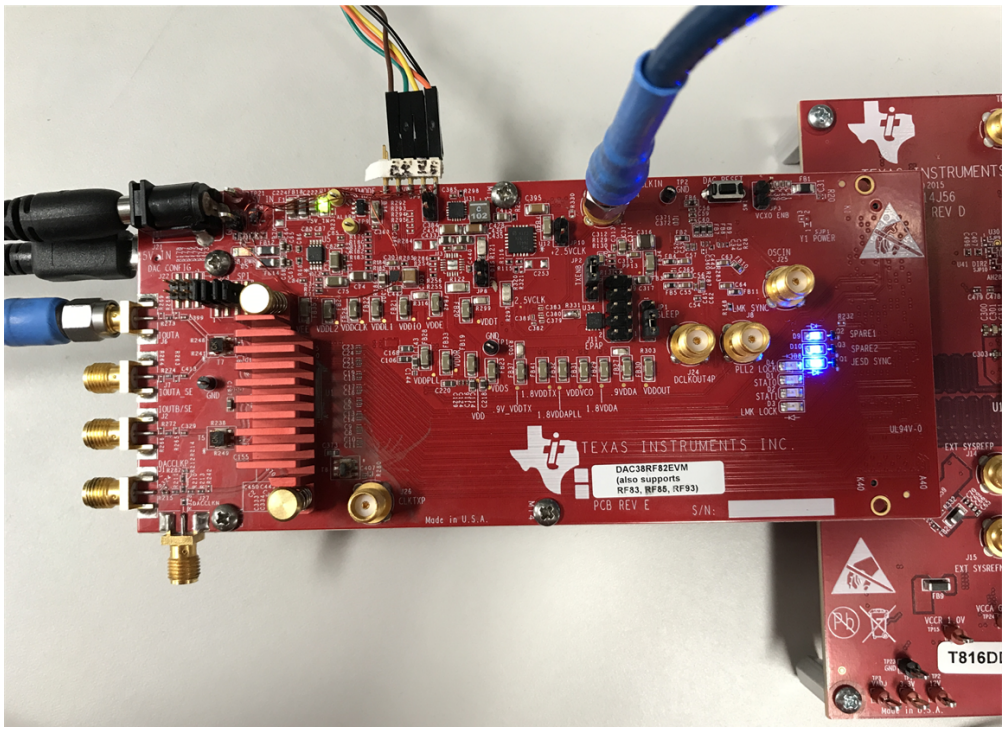

Figure 1. Hardware Setup With Soldering Modifications

3 Test Procedure

3.1 Configuring the DAC

The following Procedure describes how to set up the DAC using the DAC38RFxx EVM GUI:

1. Launch the DAC38RFxx EVM GUI.
2. Click the *Not in RESET* button to reset the DAC, and then click the *DAC in RESET* button to bring the DAC out of reset for configuration.
3. Click the *LOAD DEFAULT* button to load in the DAC initial configuration registers.
4. Next fill in the values in the *DAC Mode* box according to the desired configuration. Figure 2 shows the correct values for the LMF = 841 configuration. For this mode set the following parameters:
   - The number of DACs to dual DAC
   - The number of IQ pairs per DAC to 1 IQ pair
   - The number of SerDes lanes per DAC to 4 lanes
   - The desired Interpolation to 12x
   - Check the *PLL enable* box
   - The *Ref Freq* box to 368.64
   - The multiplier M/N to 6/1
5. Click the *CONFIGURE DAC* button.
6. Click the *PLL AUTO TUNE* button.
7. Click the *Reset DAC JESD Core & SYSREF TRIGGER* button.

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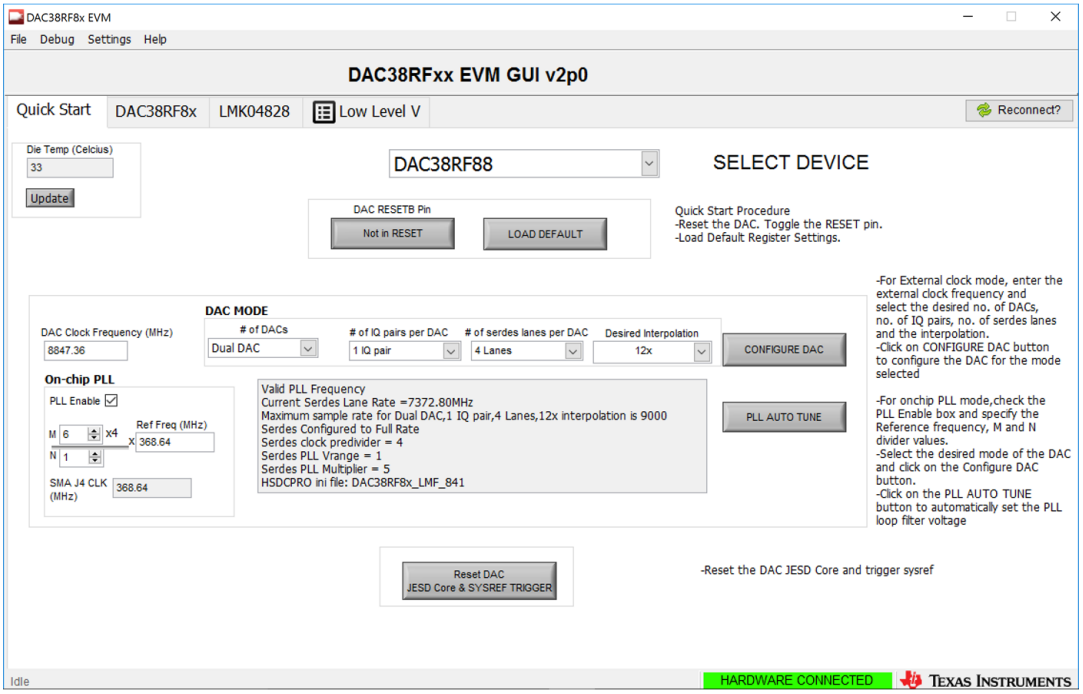

Figure 2. DAC38RF8x EVM GUI Quick Start Tab

8. The configuration should now be complete. To verify the clocking setup is correct navigate to the DAC38RF8x tab and then click the *Clocking* sub-tab. The value in the *PLL LF Voltage* box should read a value between 2 and 6. See Figure 3.

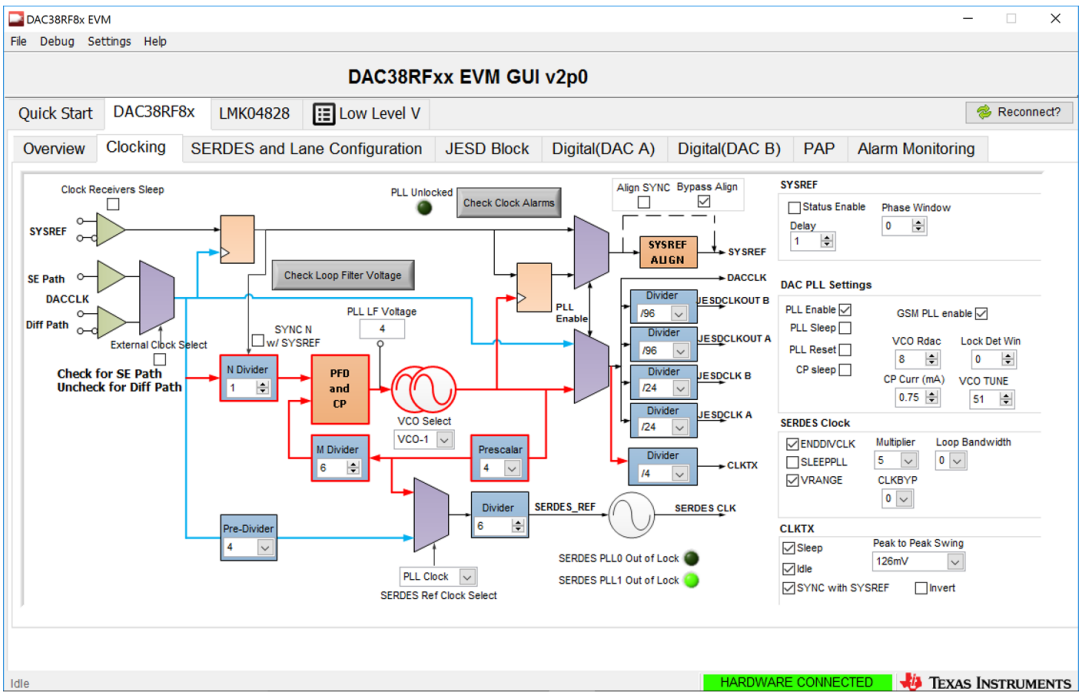

Figure 3. DAC38RFxx EVM GUI Clocking tab

9. To verify the DAC output is working properly navigate to the *Digital(DAC A)* sub-tab:
   (a) Enable the mixer and NCO for path AB.
   (b) Enter the sampling rate and enter the value *1000* for the NCO frequency.

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(c) Click the *UPDATE NCO* button.

(d) Check the *Constant Input* box and enter a value into the *Constant Value* box to send data to the DAC. See Figure 4 for reference. If the DAC is running properly there should now be a 1-GHz tone at the DAC output IOUTA.

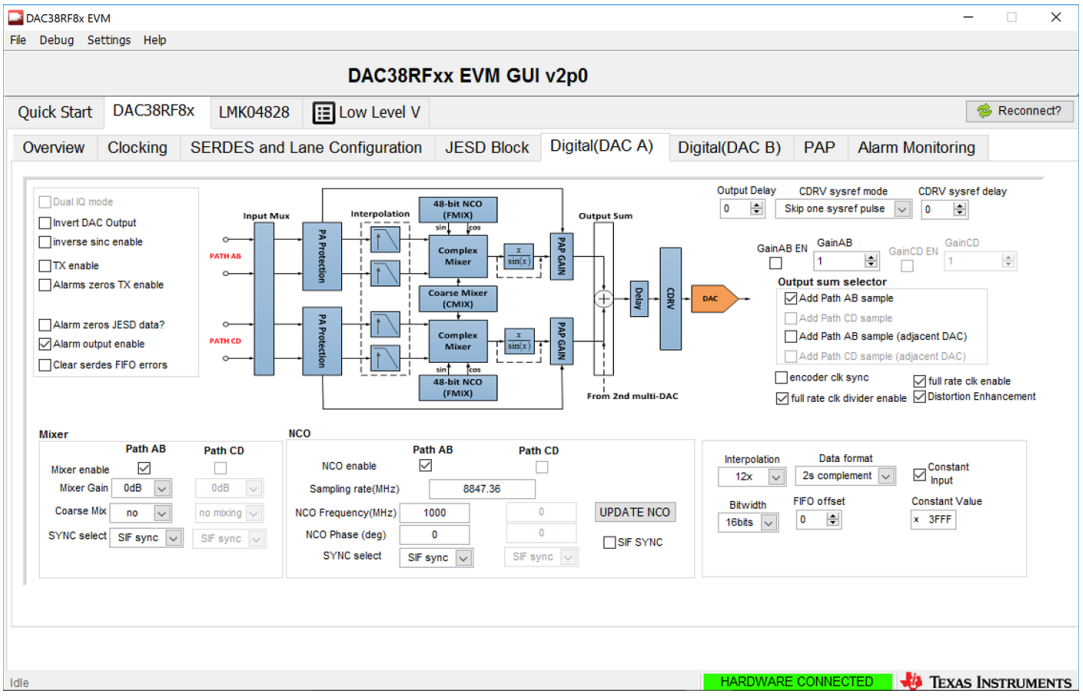

Figure 4. DAC38RFxx EVM GUI Digital(DAC A) Tab

3.2 Using the Eye Scan GUI

After the DAC has been configured, the next step is to generate the eye diagram using the DAC38RFxx eye scan GUI. This section gives a brief description of how the eye scan utility functions, and then outlines the procedure for creating the eye diagrams. The basic principles used are described as follows:

1. Enable dedicated eye scan input samplers, and generate an error when the value sampled differs from the normal data sample.
2. Apply a voltage offset to the dedicated eye scan input samplers, to effectively reduce their sensitivity. The amount of voltage offset is variable between 0 and ±300 mV in steps of approximately 10 mV.
3. Apply a phase offset to adjust the point in the eye that the dedicated eye scan data samples are taken. The samplers phase position has a resolution of 1/32 UI, where 1 UI is one-half the bit period.
4. Reset the error counter to remove any false errors accumulated as a result of the voltage or phase offset adjustments.
5. Run in this state for a period of time, periodically checking to see if any errors have occurred.
6. Change the voltage, phase offset, or both and repeat.

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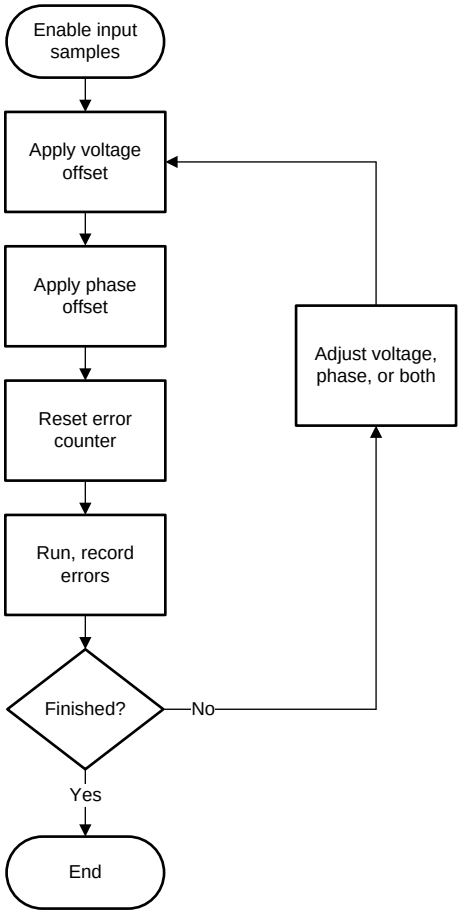

Figure 5. Flowchart

The following procedure describes how to set up the GUI and run the test procedure.

1. Launch the eye scan GUI application. Figure 6 shows the GUI main window.

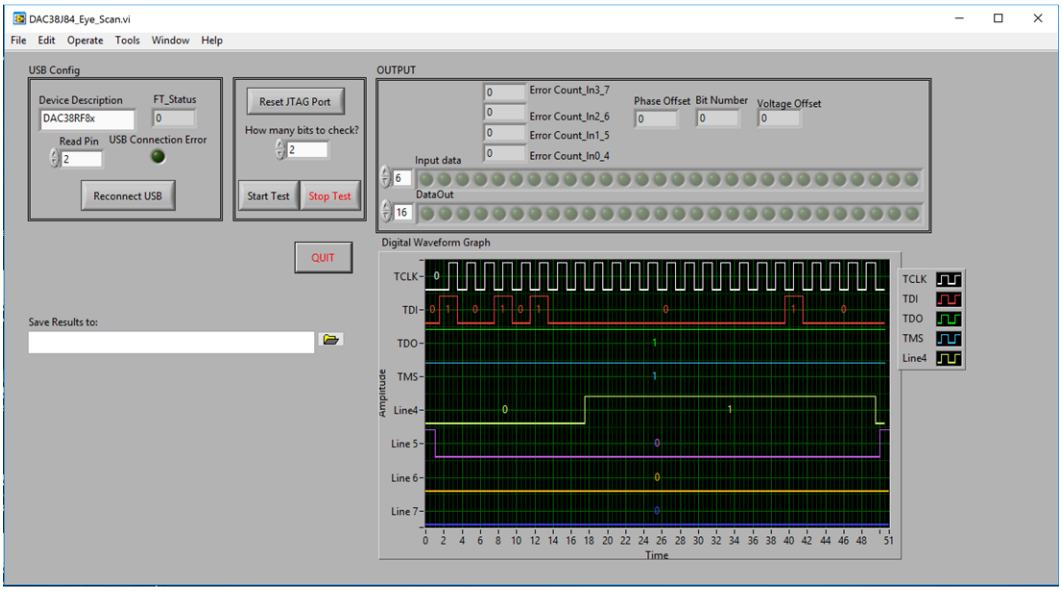

Figure 6. DAC38RF8x_EYE_SCAN GUI

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2. Set the *Device Description* box to DAC38RF8x and click *Reconnect USB*. The value in this box should match the product description in the FTDI chip programming. The *USB Connection Error* light should turn off when the connection is made.
3. Set the *Read Pin* box to 2. This value corresponds to which lane of the FTDI part is mapped to the JTAG TDO pin.
4. In the *How many bits to check* box select a value from 1 to 20. Increasing the number of bits to check increases the accuracy of the eye diagram; however, it also increases the run time of the test. TI recommends checking all 20 bits, but a quick check can be done by using just a few bits.
5. Enter a file destination in the *Save Results to:* box. This box is where the eye scan data will be saved to when the test is complete.
6. Click *Start Test*. While the test is running, users should see the input data lights cycling through the different values. For each bit in the *How many bits to* check box the eye scan will cycle through 32 different phase offset values from –16 to +16 and 64 different voltage offset values from –32 to +32. Figure 6 shows what the GUI should look like for a functioning eye scan. When the test is running properly the *DataOut* lights should be changing to reflect the received data. If the test must be stopped for some reason, click the *Stop Test* button. The *Stop Test* button will end the test but may not properly close the FTDI connection, so TI recommends restarting the GUI and reestablish a good connection if this step is necessary.

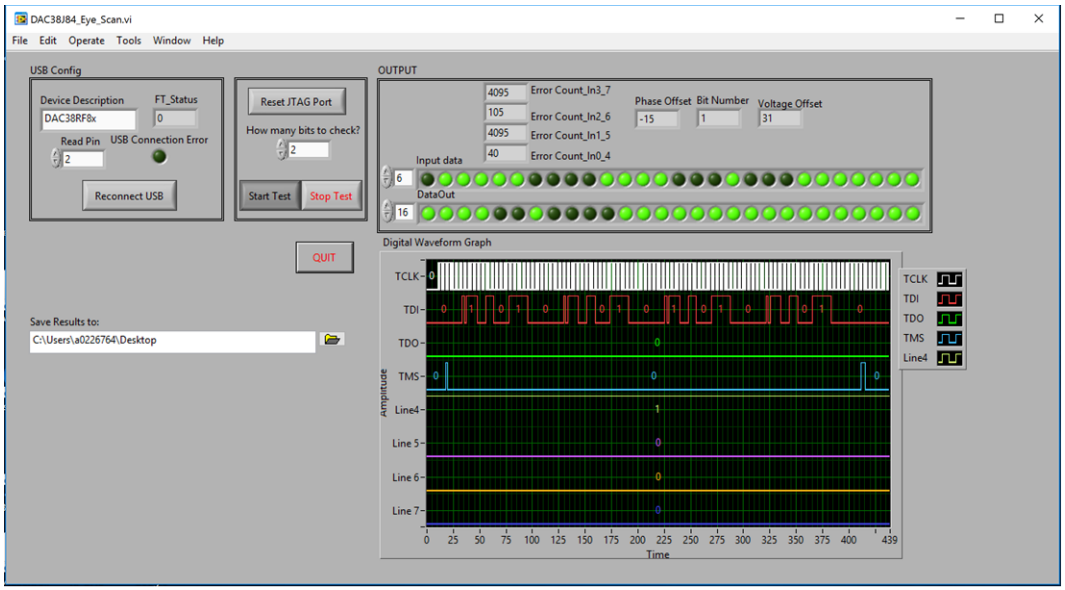

Figure 7. Eye Scan Test in Progress

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3.3 Analyzing the Results

After the test is complete a display similar to Figure 8 appears to show the eye diagram. Verify the data file path is correct and click the *Read File* button to load in the eye scan results. The window should now resemble Figure 9.

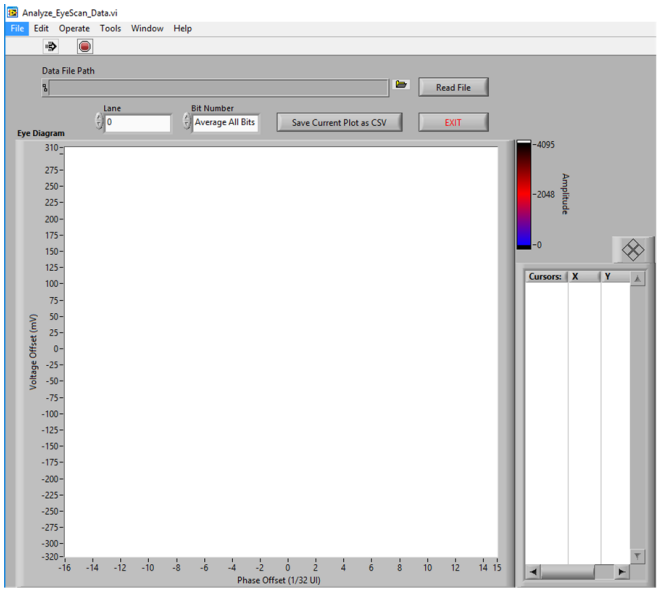

Figure 8. Eye Scan Viewer

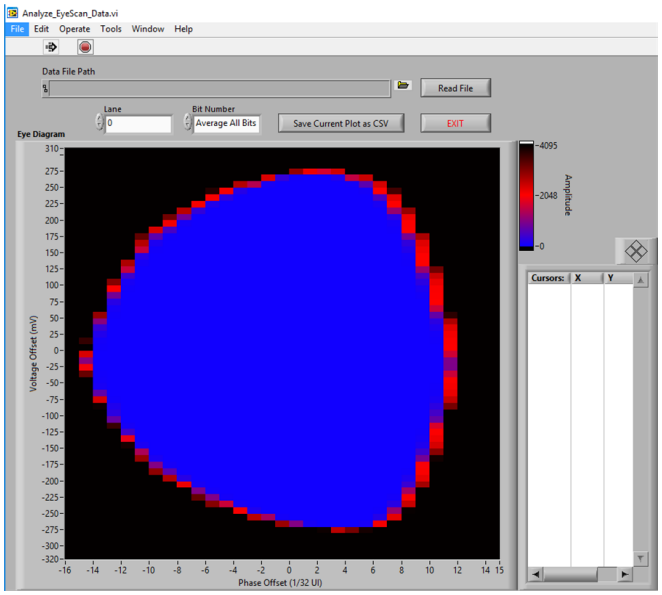

Figure 9. Generated Eye Diagram

4 Interpretation of Results

The JESD204B standard specifies eye mask requirements for receivers and transmitters based on the data signal speed. For the eye scan test the DAC is acting as a receiver, accepting signals from the FPGA, so the test results should be compared to the receiver standard for the required speed. The standard eye masks designate a *keep-out* area for the signal, and therefore the eye opening must be large enough to completely envelop the eye mask to ensure a good bit error ratio. Figure 10 and Figure 11 show the JESD204B standard eye masks are shown in the two figures below.

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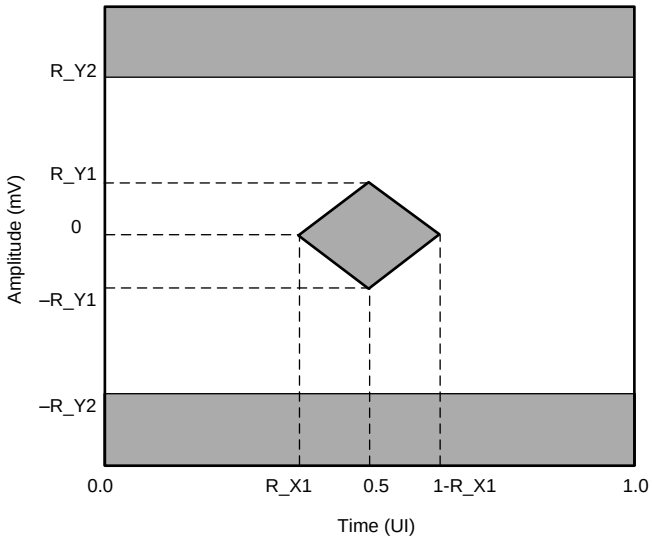
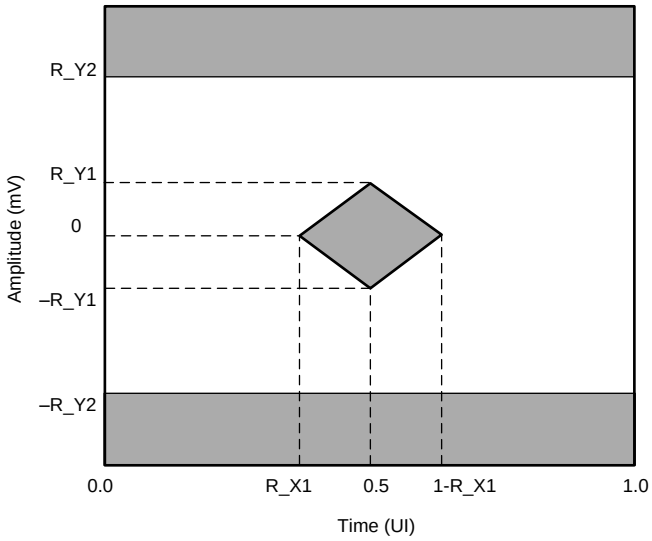


R_X1 (UI)	1-R_X1 (UI)	R_Y1 (V)	R_Y2 (V)	R-SJ-hf (p-p UI)	R-SJ-max (p-p UI)	R_BHPJ (p-p UI)	TJ (p-p UI)
0.35	0.62	0.055	0.525	0.05	5	0.45	0.70

Figure 10. Standard JESD204B Eye Mask for 11-G Receiver



R_X1 (UI)	1-R_X1 (UI)	R_Y1 (V)	R_Y2 (V)	R-SJ-hf (p-p UI)	R-SJ-max (p-p UI)	R_BHPJ (p-p UI)	TJ (p-p UI)
0.30	0.70	0.0625	0.375	0.05	5	0.45	0.60

Figure 11. Standard JESD204B Eye Mask for 6-G Receiver

If the eye diagram generated by the GUI fits these eye mask specifications, the DAC SerDes link is demonstrating a good signal quality and should exhibit low bit error rate performance as according to the standard.

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5 References

For additional reference, refer to:

- Texas Instruments, *DAC38RF8x Dual-Channel, Differential-Output, 14-bit, 9-GSPS, RF-Sampling DAC with JESD204B Interface, On-Chip PLL and Wide-Band Interpolation* data sheet
- Texas Instruments, *DAC38RF8xEVM* user's guide

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