Application Note

Clocking Configuration of Device and Flexible Clocking For TAx5x1x Family

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ABSTRACT

This document applies to the following part numbers:

TAC5212, TAC5112, TAC5211, TAC5111, TAA5212, TAD5212, TAD5112, TAC5412-Q1, TAC5411-Q1, TAC5312-Q1, TAC5311-Q1, TAC5212-Q1, TAC5211-Q1, TAC5112-Q1, TAC5111-Q1, TAA5412-Q1, TAD5212-Q1, TAD5112-Q1,TAA5242,TAD5142,TAD5242

These devices have a smart auto-configuration block to generate all necessary internal clocks required for the ADC and DAC Circuitry as well as the digital filter engine used for signal processing. This configuration is done by monitoring the frequency of the FSYNC and BCLK signal on the audio buses. The device supports the various data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming.

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1 Introduction

The Device Supports a Primary as well as Secondary ASI. There are several automatic modes of operation described where either the primary BCLK /FYSNC or Secondary BCLK/FSYNC can be used for determination of the incoming timing modes.

In addition, the MCLK / FSYNC can also be used to do the timing determination.

The device has the following interfaces that setup the clocking.

Interface	Setup
MCLK	Master Clock
FSYNC	Primary FSYNC/ Secondary SYNC
PASI BCLK	Primary BCLK
PASI FSYNC	Primary FSYNC
SASI BCLK	Secondary BCLK
SASI FSYNC	Secondary SYNC

The BCLK and FSYNC Pins as well as the GPIO/GPI/GPO pins can be configured to setup the Primary and Secondary ASI.

The timings must lie within the limits described in Table 1-1 and Table 1-2.

Table 1-1. Multiples of 48Khz

Pins	Timings
Fs	3KHz-768KHz
BCLK	256KHz - 24.576MHz
MCLK	256KHz - 49.152MHz

Table 1-2. Multiples of 44.1Khz

Pins	Timings
Fs	2.75KHz-705.6KHz
BCLK	235.2KHz – 22.57MHz
MCLK	235.1KHz - 45.15MHz

Note

The nomenclature of *Target* is used to indicate Slave Mode of Operation. The nomenclature of *Controller* is used to indicate Master Mode of operation.

2 Operating Modes for the Clocking

Internally, the modes of operation are categorized as the following:

Auto Mode of Operation: Based on the CLK_SRC_SEL configuration **B0_P0_R52[3:1]**, the mode can be further divided as follows:

1. **Auto Primary BCLK Ratio Mode (3'd0) –** Primary ASI BCLK is selected to be the audio source clock by the user.
2. **Auto Secondary BCLK Ratio Mode (3'd2) –** Secondary ASI BCLK is selected to be the audio source clock by the user.
3. **Auto MCLK Ratio Mode (3'd1 or 3'd3) –** MCLK supplied at the input Pad to be user as audio source, Frequency of MCLK is Integer multiple of Fsync frequency.
4. **Auto MCLK Fixed Mode (3'd4) –** MCLK supplied at the input Pad to be user as audio source, MCLK frequency has no integral relation with the Fsync frequency (PLL use is mandatory).
5. **Custom Mode of Operation** CUSTOM_CLK_CFG register to 1'b1 (B0_P0_R50[0]). User Configures all the Dividers manually in this mode.
6. **Semi-Automatic mode**: This is used to detect Non-audio timings automatically.

2.1 Automatic Modes of Operation

The Fsync and BCLK-to-Fsync-Ratio of the Primary ASI Interface are auto detected by the device. Based on the device configuration (number of channels, signal processing configuration, and so on), all clock dividers/mux selects are auto inferred.

PLL enablement is auto Inferred based upon the MIPS Required and highest Clock Frequency available in the system.

Table 2-1 shows the different sample rates that are recognized by the automatic configuration module. Incoming timings are split into several buckets of frequency. Note that for automatic modes the incoming FSYNC must be within one of the frequency buckets

Table 2-1. Sample Rates Accepted in the Automatic Mode

Fs Min (KHz)	Fs Typ (KHz)	Fs Max (KHz)
698.54	768	775.68
349.27	384	387.84
174.64	192	193.92
87.32	96	96.96
43.66	48	48.48
29.11	32	32.32
21.83	24	24.24
14.55	16	16.16
10.91	12	12.12
7.28	8	8.08
4.37	4.8	4.85
2.73	3	3.03

Table 2-2 shows the BCLK to FSYNC Ratios that are recognized by the automatic clocking mechanism.

Table 2-2. BCLK to FSYNC Ratio

Expanded List of BCLK to Fs Ratio Supported										
16	20	24	32	40	48	60	64	72	80	96
100	112	120	128	140	144	160	168	176	180	192
200	208	216	220	224	240	256	260	264	272	280
288	300	304	312	320	336	340	352	360	368	380
384	400	408	416	420	432	440	448	456	460	464
480	496	500	504	512	520	528	540	544	552	560
576	580	592	600	608	620	624	640	648	656	660
672	680	688	696	700	704	720	736	740	744	752
760	768	780	784	792	800	816	820	832	840	848
860	864	880	888	896	900	912	920	928	936	940
944	960	976	980	984	992	1000	1008	1020	1024	1032
1040	1056	1060	1080	1088	1100	1104	1120	1128	1140	1152
1160	1176	1180	1184	1200	1216	1220	1224	1240	1248	1260
1272	1280	1296	1312	1320	1344	1368	1376	1392	1408	1416
1440	1464	1472	1488	1504	1512	1536	1568	1600	1632	1664
1696	1728	1760	1792	1824	1856	1888	1920	1952	1984	2016
2048										

Note

In Automatic clocking the device recognizes integer ratios of BCLK/FSYNC. However, Table 2-2 shows some ratios of BCLK/FSYNC where optimum SNR and lowest power consumption is obtained. Therefore, these timings are preferred.

Refer to the Table 2-1 and Table 2-2 above. If the incoming frequency is 43.66Mhz and the Incoming BCLK is 873.2Khz then the automatic configuration shall recognize the BCLK/Fs ratio as 20 and shall setup the internal clocking accordingly.

3 Clocking Modes

3.1 Auto Primary BCLK Ratio

Primary ASI should be Target, Secondary ASI can be either Controller, Target or disabled Primary ASI BCLK provided by user is used as *Reference clock for the PLL* or *Audio Root Source clock*.

Table 3-1. Register Settings to Setup Mode

I2C Bits	
CLK_SRC_SEL	(B0_P0_R52[3:1]) – must be 3'd0
CUSTOM_CLK_CFG register	(B0_P0_R50[0]) – must be 1'b0
PASI_SAMP_RATE	(B0_P0_R50[7:2])
PASI_FS_BCLK_RATIO	{B0_P0_R56[5:0], B0_P0_R57
Must be configured as 0 for the device to auto detect	
PASI_MST_CFG	B0_P0_R55[4]
0 to operate Primary ASI as Target(Default)	

To operate Secondary ASI as Controller Mode, we need to specify the Fs Rate as well as the BCLK to Fs ration

Table 3-2. Register Setting to Setup as Controller

Mode	Controller
SASI_MST_CFG	B0_P0_R55[3]
1 to operate Secondary ASI as Controller, 0 to operate Secondary ASI as Target(Default)	
SASI_FS_BCLK_RATIO	B0_P0_R58[5:0], B0_P0_R59
SASI_SAMP_RATE	B0_P0_R51[7:2]
FS_MODE	B0_P0_R55[0]
1 to generate Fsync frequency as a multiple of 44.1KHz , 0 to generate Fsync frequency as a multiple of 48KHz (Default)	

3.2 Auto Secondary BCLK Ratio

Secondary ASI needs to be Target, Primary ASI can be either Controller, Target, or disabled Secondary ASI BCLK provided by user is used as *Reference clock for the PLL* or *Audio Root Source clock*.

Configurations to enter this mode include:

Table 3-3. Register Settings to Setup Mode

Mode	Configuration
CLK_SRC_SEL	(B0_P0_R52[3:1]) – must be 3'd0
CUSTOM_CLK_CFG register	(B0_P0_R50[0]) – must be 1'b0
SASI_SAMP_RATE	(B0_P0_R51[7:2])
SASI_FS_BCLK_RATIO	{B0_P0_R58[5:0], B0_P0_R59
Must be configured as 0 for the device to auto detect	

Controller Mode: To operate primary ASI as Controller Mode, specify the Fs Rate as well as the BCLK to Fs ratio.

Table 3-4. Register Setting to Setup as Controller

Mode	Configuration
PASI_MST_CFG	B0_P0_R55[4]
1 to operate Primary ASI as Controller 0 to operate Primary ASI as Target (Default)	
PASI_FS_BCLK_RATIO	B0_P0_R56[5:0], B0_P0_R57
PASI_SAMP_RATE	B0_P0_R50[7:2]
FS_MODE	B0_P0_R55[0]
Must be configured as 0 for the device to auto detect	

3.3 Auto MCLK Ratio

MCLK supplied at the input Pad is to be user as audio source, Frequency of MCLK is Integer multiple of Fsync frequency. Both the Primary FSYNC can be used as timing reference. Auto detection is enabled in this mode.

Both Primary and Secondary ASI's can be configured either Controller or Target. At least one can be enabled. MCLK provided by the user is used as *Reference clock for the PLL* or *Audio Root Source clock*

Table 3-5. Register Settings to Setup Mode

Mode	Configuration
CLK_SRC_SEL	(B0_P0_R52[3:1]) – must be 3'd1 or 3d3
Frequency that is integer multiple of PASI Fsync, when CLK_SRC_SEL is configured as 3'd1. Frequency that is integer multiple of SASI Fsync, when CLK_SRC_SEL is configured as 3'd3.	
CUSTOM_CLK_CFG register	(B0_P0_R50[0]) – must be 1'b0
PASI/SASI_SAMP_RATE	(B0_P0_R50[7:2] B0_P0_R51[7:2])
FS_MCLK_RATIO	{B0_P0_R53[5:0], B0_P0_R54}
Must be configured as 0 for the device to auto detect	

Controller Mode: To operate primary ASI as Controller Mode, the Fs Rate needs to be specified as well as the BCLK to Fs ration

Table 3-6. Register Setting to Setup as Controller

Mode	Configuration
PASI_MST_CFG	B0_P0_R55[4]
1 to operate Primary ASI as Controller, 0 to operate Primary ASI as Target (Default)	
SASI_MST_CFG	B0_P0_R55[3]
1 to operate Secondary ASI as Controller , 0 to operate Secondary ASI as Target(Default)	
FS_MCLK_RATIO	B0_P0_R53[5:0], B0_P0_R54
PASI_SAMP_RATE	B0_P0_R50[7:2]
SASI_SAMP_RATE	B0_P0_R51[7:2]
FS_MODE	B0_P0_R55[0]
1 to generate Fsync frequency as a multiple of 44.1 KHz , 0 to generate Fsync frequency as a multiple of 48 KHz (Default)	

3.4 Auto MCLK Fixed

MCLK supplied at the input Pad to be user as audio source, MCLK frequency has no integral relation with the Fsync frequency (PLL use is mandatory) Both Primary and Secondary ASI's can be only configured as Controller.

Only certain combinations of MCLK Frequencies as given in MCLK_FREQ_SEL register are allowed. The following frequencies for MCLK are allowed.

Table 3-7. Allowed MCLK Frequencies

MCLK_FREQ_SEL	Frequency to be Provided (MHz)
3'd0	12
3'd1	12.288
3'd2	13
3'd3	16
3'd4	19.2
3'd5	19.68
3'd6	24
3'd7	24.576

Table 3-8. Register Settings to Setup Mode

Mode	Configuration
CLK_SRC_SEL	(B0_P0_R52[3:1]) – needs to be 3'd4
CUSTOM_CLK_CFG register	(B0_P0_R50[0]) – needs to be 1'b0
MCLK_FREQ_SEL register	(B0_P0_R55[7:5])
FS_MODE register	(B0_P0_R55[0])

Table 3-9. Primary as Controller

Mode	Configuration
PASI_MST_CFG	B0_P0_R50[7:2]
PASI_FS_BCLK_RATIO	B0_P0_R56[5:0], B0_P0_R57

Table 3-10. Secondary as Controller

Mode	Configuration
SASI_SAMP_RATE	B0_P0_R51[7:2]
PASI_FS_BCLK_RATIO	{B0_P0_R58[5:0], B0_P0_R59}

The following menus from Pure Path Console 3 Show this mode.

The MCLK input is setup for a input frequency of 13Mhz on GPIO1 pin.

The Primary ASI is a Controller. This creates a FSYNC of 48Khz and BCLK of 6.144Mhz.

3.5 Custom Mode and Semi Automatic Mode of Operation

CUSTOM_CLK_CFG register to 1'b1 (B0_P0_R50[0]). User Configures all the Dividers manually in this mode

3.5.1 Semi-Automatic Mode

At times there is a need to work with Non-Standard Clock Rates. To enable detection of a nonstandard clock rate, the frequency range has to be specified, see Table 3-11 and Table 3-12. This specification can be done by setting the following registers.

- PASI_SAMP_RATE(5..O) in Register 0x32
- SASI_SAMP_RATE(5..O) in Register 0x33

After defining the settings, the automatic configuration functions if the incoming FSYNC frequency is matching with the sample rate setup in 0x32 and 0x33.

Table 3-11. Frequency Ranges

S.No	Fs Bin (Hz)			Oscillator Count Range	
	Min	Typical	Max	Min	Max
1	670320	768000	806400	12	21
2	536256	614400	645120	15	26
3	446880	512000	537600	18	30
4	383040	438857.14	460800	22	35
5	335160	384000	403200	25	40
6	297920	341333.33	358400	28	45
7	268128	307200	322560	32	50
8	223440	256000	268800	38	59
9	191520	219428.57	230400	45	69
10	167580	192000	201600	52	78
11	148960	170666.67	179200	58	88
12	134064	153600	161280	65	98
13	111720	128000	134400	78	117
14	95760	109714.29	115200	92	136
15	83790	96000	100800	105	155
16	74480	85333.33	89600	118	175
17	67032	76800	80640	132	194
18	55860	64000	67200	158	232
19	47880	54857.14	57600	185	271
20	41895	48000	50400	211	309

Table 3-12. Frequency Ranges

S.No	Fs Bin (Hz)			Oscillator Count Range	
	Min	Typical	Max	Min	Max
21	37240	42666.67	44800	238	348
22	33516	38400	40320	265	386
23	27930	32000	33600	318	463
24	23940	27428.57	28800	371	540
25	20947.50	24000	25200	424	617
26	18620	21333.33	22400	478	694
27	16758	19200	20160	531	771
28	13965	16000	16800	637	925
29	11970	13714.29	14400	744	1079
30	10473.75	12000	12600	850	1233
31	9310	10666.67	11200	957	1387
32	8379	9600	10080	1063	1541
33	6982.50	8000	8400	1276	1849
34	5985	6857.14	7200	1489	2157
35	5236.88	6000	6300	1702	2465
36	4655	5333.33	5600	1915	2773
37	4189.50	4800	5040	2127	3081
38	3491.25	4000	4200	2553	3696
39	2992.50	3428.57	3600	2979	4312
40	2618.44	3000	3150	3405	4928

3.6 Additional Clocks

3.6.1 PDM Clocks

The PDM Clock frequency for the Digital Mic is programmable The Frequency can be selected using PDM_CLK_CFG Register(B0_P0_R53[7:6])

Frequencies programmable are 768 KHz, 1.536MHz, 3.072MHz, 6.144MHz.

3.6.2 Boost Clock

By default, Boost clock is generated to be 6.144MHz.

BST_CLK_FREQ_SEL(B0_P3_R72[6]) - 6Mhz or 3MHz (further division of 2).

3.6.3 SAR Clock

By default, SAR clock is generated to be 6.144MHz

SAR_CLK_FREQ_SEL(B0_P3_R73[7:6])

Frequencies Programmable : 6Mhz, 3MHz (further division of 2), 1.5MHz (further division of 4)

3.6.4 CLKOUT

Internal clocks can be routed externally to a GPIO/GPO. The following registers are used to select the clock source as well as the divider ratio.

The possible input sources that can be routed to CLKOUT include:

- DSP_CLK,SASI_BCLK,PASI_BCLK,OSC_CLK,MCLK ,CLK_SYS.

Note that OSC_CLK is 12.288Mhz.

Table 3-13. Register Settings for CLKOUT

Mode	Configuration
CLKOUT_CLK_SEL	(B0_P3_R70[2:0]),
CLKOUT_DIV_EN	(B0_P3_R71[7])
CLKOUT_DIV	(B0_P3_R71[6:0])

4 Clocking in Hardware Controlled Devices

The Tax5x1x family also has some Hardware pin controlled Variants.

TAA5242 is the ADC Variant. TAD5142 and TAD5242 are the DAC variants.

The hardware variants support an Audio Bus Controller ot target mode of operation using Mode pin MD0. In target mode ,FSYNC and BCLK work as input pins. In controller mode FSYNC and BCLK work as output pins. This is indicated in the table below.

The Hardware device supports automatic clocking as shown in Section 2.1.

Table 4-1. Controller and Target Mode Selection

MD0	Controller and Target Selection
Short to ground	Target I2S mode
Short to ground with 4.7KΩ	Target TDM mode
Short to AVDD	Controller I2S module
Short to AVDD with 4.7KΩ	Controller TDM mode
Short to AVDD with 22K Ω	Target LJ mode

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2023) to Revision A (September 2024) **Page**

- Updated Section Abstract....1
- Added Section 4....11

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