Texas Instruments

TLV320AIC20K/24KEVM

User's Guide

April 2005 *Data Acquisition Products*

SLAU088A

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It is important to operate this EVM with a maximum input supply voltage not exceeding 4 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This users guide describes the operation and use of the TLV320AIC20K codec family. A complete circuit descriptiion, schematic diagram, and bill of materials are also included.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—EVM Overview
- Chapter 2—Digital Interface
- Chapter 3—Analog Interface
- Chapter 4—EVM Operation
- Chapter 5—TLV320AIC20K/24K Bill of Materials
- Appendix A—TLV320AIC20K/24K Schematic

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Data Sheet:	Literature Number:
TLV320AIC20K/24K	SLAS363

Contents

Figures

Tables

Chapter 1

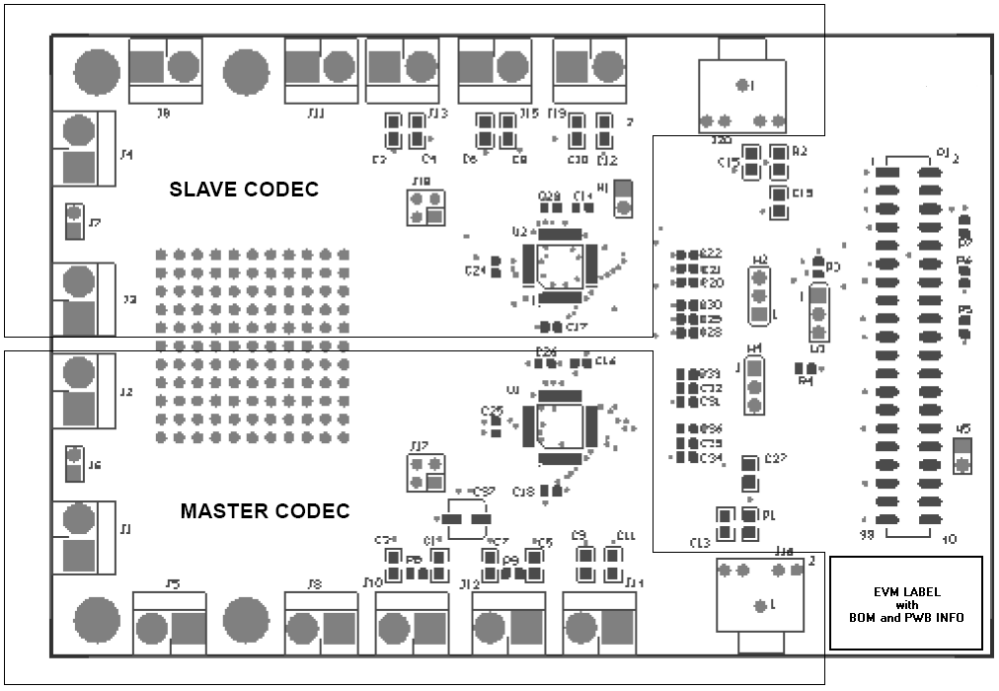
EVM Overview

This user's guide provides support for the following EVMs:

- ❑ TLV320AIC20KEVM
- ❑ TLV320AIC24KEVM

Figure 1−1. EVM

The EVM is split into two complementary halves as shown in Figure 1−1.



Chapter 2

Digital Interface

The digital signals required to operate this codec originate from the 40-pin connector—J21. There are two methods to drive the digital interface:

- Create a custom interface between the codec EVM and the host system.
- Alternatively, if a TI DSK (DSP starter kit) is the host system, a development platform (AICDEVPLAT EVM) is available from TI. This platform provides the additional functions that the codec requires in a convenient form factor.

Topic **Page**

2.1 Codec-to-Platform

The TLV320AIC20K and 24K mate with the development platform via a 40-pin Samtec connector. The mating connector (Samtec part number, TSM-120-01-T-DV-P) is used on the development platform to provide the electrical connections necessary. Consult Samtec at www.samtec.com or 1−800−SAMTEC−9 for more information.

The pinout for the 40-pin connector is listed in Table 2−1.

Table 2−1. Pinout for 40-Pin Connector

Pin Number	Signal	Description
J21.1	MCLK	Master clock
J21.2	DGND	Digital ground
J21.3	SCLK	Serial data clock
J21.4	DGND	Digital ground
J21.5	DIN	Data in
J21.6	DGND	Digital ground
J21.7	DOUT	Data out
J21.8	Reserved	Reserved for future use
J21.9	FS	Frame sync
J21.10	Reserved	Reserved for future use
J21.11	CLKX	Transmit clock
J21.12	Reserved	Reserved for future use
J21.13	FSX	Frame sync transmit
J21.14	Reserved	Reserved for future use
J21.15	DX	Data transmit
J21.16	DR	Data receive
J21.17	RESET	Global reset for all devices
J21.18	FSR	Frame sync receive
J21.19	PWDN	Global powerdown for all devices
J21.20	CLKR	Receive clock
J21.21	CNTLb	GPIO pin
J21.22	CNTLa	GPIO pin
J21.23	STATb	Status pin
J21.24	STATa	Status pin
J21.25	3.3V_D	Digital 3.3 V
J21.26	Reserved	Reserved for future use
J21.27	3.3V_D	Digital 3.3 V
J21.28	DGND	Digital ground
J21.29	1.8V_D	Digital 1.8 V
J21.30	DGND	Digital ground
J21.31	1.8V_D	Digital 1.8 V
J21.32	DGND	Digital ground

Table 2−1. Pinout for 40-Pin Connector (Continued)

Pin Number	Signal	Description
J21.33	3.3V_A_DRV	Output driver supply 3.3 V
J21.34	AGND	Analog ground
J21.35	3.3V_A_DRV	Output driver supply 3.3 V
J21.36	AGND	Analog ground
J21.37	3.3V_A	Analog 3.3 V
J21.38	AGND	Analog ground
J21.39	3.3V_A	Analog 3.3 V
J21.40	AGND	Analog ground

The development platform supports a number of functions that the codecs require. These are:

- ❑ MCLK generation
- ❑ Manual reset generation
- ❑ Power options

Refer to the *DSP − Codec Development Platform User's Guide* (TI Literature Number SLAU090) for details regarding the development platform.

Further descriptions regarding the operation of this EVM assumes that the development platform is being used for all additional signals and power.

2.2 Jumper Options

There are eight jumpers on the board that can be configured in various ways, depending upon the user's requirements. Their functions are briefly presented in Table 2–2:

Table 2–2. Jumper Options

Jumper	Function
W1	Gives users the option of disconnecting the 3.3-V driver ground from the regular analog ground
W2	Manages FSD from the master. Either connecting FSD to the next codec or providing relevant polarity
W3	Used along with W2 for correct polarity for FSD
W4	Selects whether U1 is either a master or a slave codec.
W5	Connects analog and digital ground together
P1.9–P1.10	Last FSD in the chain must be high
P1.11–P1.12	SCL must be high
P1.13–P1.14	SDA must be high

Since the EVM contains two codecs, there a variety of options available to the user:

- ❑ Stand-alone slave codec
- ❑ Single master codec
- ❑ Master/slave cascade

Note that the terms master and slave refer to the codec device itself. Keep in mind that each of these codecs contains two independent channels connected together internally. Thus any codec configuration described in this guide actually comprises two individual codecs chained together and performing as one unit.

Each of these options are discussed in the following sections.

2.2.1 Stand-Alone Slave

This configuration applies to EVM1 only. When a single codec is to be used in slave mode, U1 is always the slave codec. Follow the jumper settings detailed in Table 2–3 for this condition.

Table 2–3. Stand-Alone Slave Jumper Settings

Jumper	1–2	2–3
W2	Inserted	Not inserted
W3	Not inserted	Inserted
W4	Not inserted	Inserted
P1.9–P1.10	N/A	N/A

2.2.2 Single Master Only

This configuration applies to EVM1 only. When a single codec is to be used in master mode, U1 is always the master codec. Follow the jumper settings detailed in Table 2–4 for this condition.

Table 2–4. Single Master Only Jumper Settings

Jumper	1–2	2–3
W2	Inserted	Not inserted
W3	Inserted	Not inserted
W4	Inserted	Not inserted
P1.9–P1.10	N/A	N/A

2.2.3 Master/Slave Cascade

This configuration applies to EVM1 only and is the factory-set shipping condition. When both codecs are used, both U1 and U2 are active. In this condition U1 is always the master codec, and U2 is always the slave codec. Follow the jumper settings detailed in Table 2–5.

Table 2–5. Master/Slave Cascade Jumper Settings

Jumper	1–2	2–3
W2	Not inserted	Inserted
W3	N/A	N/A
W4	Inserted	Not inserted
P1.9–P1.10	Inserted	Inserted

Chapter 3

Analog Interface

Table 3–1 indicates the applicable connectors for each codec. In order to enable a wide range of sources and loads to be connected to the codecs, screw terminals have been used wherever possible.

Table 3–1. Analog Interface Connectors

	TLV320AIC20K		TLV320AIC24K	
	Master	**Slave**	**Master**	**Slave**
Input Sources				
8-Ω Speaker output	J2	J11	Not available	
600-Ω Line output	J5	J4	J5	J4
150-Ω Handset output	J1	J9	J1	J9
150-Ω Headset output	J8	J3	J8	J3
Output Loads				
Handset input/INP2	J12	J19	J12	J19
Headset input/INP3	J10	J13	J10	J13
Microphone input	J16	J20	J16	J20
Line input/INP1	J14	J15	J14	J15
Caller ID input/INP4	J17	J8	J17	J8

Chapter 4

EVM Operation

The EVM is shipped from the factory in master/slave cascade mode. To check if the EVM is working properly, simply install the EVM onto the development platform and apply power to the DSK. The EVM should begin working immediately.

In the default mode, the codecs recognize that there are four discrete channels, consequently the resultant SCLK and FS signals transmitted by the master codec adjust automatically based on the available MCLK.

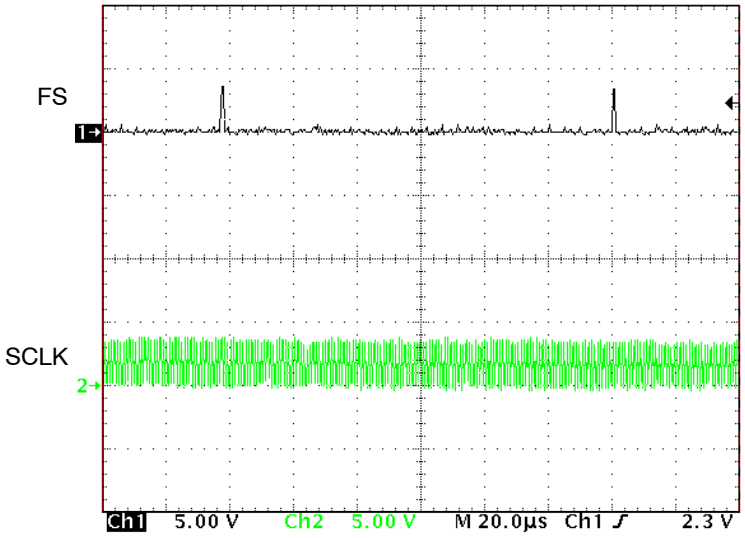
It is now possible to calculate what should be observed after power up by calculating what FS and SCLK should be observed:

- FS
  - In this example, MCLK is generated by the development platform and is equal to 100 MHz.
  - FS = MCLK/16 × m × n × p
  - Default values for m, n, and p are 16, 6, and 8 respectively
  - FS = $100 \times 10^6 / 16 \times 16 \times 6 \times 8$
  - FS = 8138 kHz
- SCLK
  - SCLK = 16 × FS × (number of devices) × 2
  - SCLK = 16 × 8138 × 4 × 2
  - SCLK = 1.04 MHz

FS can be observed either directly at the FS pin of U1 or U2 (pin 19) or on the development platform at TP9. SCLK can be observed easily at P1 pin 3 of the EVM or on the development platform at TP8.

The captured signals are shown in Figure 4−1.

Figure 4−1. EVM Captured Signals



Chapter 5

TLV320AIC20K/24K Bill of Materials

The following table contains a complete bill of materials for the TLV320AIC20K/24K codec EVM. The schematic diagram is also provided for reference. Contact the Product Information Center or e-mail dataconvapps@list.ti.com for questions regarding this EVM.

Used	Value	Ref Des	Description	Vendor	Part number
4	0.01 µF	C20 C29 C32 C34	Capacitor 10000-pF 50-V ceramic Y5V 0603	Panasonic	ECJ-1VF1H103Z
12	0.1 µF	C14 C16 C17 C18 C21 C23 C24 C25 C26 C28 C33 C35	Capacitor 0.1-µF 25-V ceramic Y5V 0603	Panasonic	ECJ-1VF1E104Z
16	0.1 µF	C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C15 C19 C27	Capacitor 0.1-µF 50-V ceramic X7R 0805	Panasonic	ECJ-2YB1H104K
4	1 µF	C22 C30 C31 C36	Capacitor 1-µF 10-V ceramic Y5V 0603	Panasonic	ECJ-1VF1A105Z
1	10 µF	C37	Capacitor 10-µF 16-V VS elect SMD	Panasonic	ECE-V1CA100SR
7	10 kΩ	R3 R4 R5 R6 R7 R8 R9	Resistor 10-kΩ 1/16-W 5% 0603 SMD	Panasonic	ERJ-3GEYJ103V
2	10 kΩ	R1 R2	Resistor 10.0-kΩ 1/10-W 1% 0805 SMD	Panasonic	ERJ-6ENF1002V
2		U1 U2 *	IC CODEC dual-channel PROG LP 48-TQFP	Texas Instruments	TLV320AIC20KIPFB
	* Alternate		IC CODEC dual-channel PROG LP 48-TQFP	Texas Instruments	TLV320AIC24KIPFB
1			TLV320AIC20 PWB	Advanced Circuit Design	6442569
0			TLV320AIC20 DDB	Texas Instruments	6442568
1		J21	40-Pin SMT socket	Samtec	SSW-120-22-F-D-VS-K
1		P1	40-Pin SMT plug	Samtec	TSM-120-01-T-DV-P

Used	Value	Ref Des	Description	Vendor	Part number
14		J1 J2 J3 J4 J5 J8 J9 J10 J11 J12 J13 J14 J15 J19	2 Terminal screw connector	Lumberg	KRMZ2
2		J16 J20	161−3504	Mouser	161-3504
2		J17 J18	4-Pin plug	Samtec	TSW-102-07-L-D
4		J6 J7 W1 W5	2 Position jumper	Samtec	TSW-102-07-L-S
3		W2 W3 W4	3 Position jumper	Samtec	TSW-103-07-L-S
2		See Assy Dwg	1.000/4−40 Nylon hex thread SP	Keystone Electronics	1902E
2		See Assy Dwg	0.500/4−40 Nylon hex thread SP	Keystone Electronics	1902C
2		See Assy Dwg	4−40 X 1/4 Machine screw PH SS	Building Fasteners	PMSSS 440 0025 PH

Appendix A

TLV320AIC20K/24K EVM Schematic

The TLV320AIC20K/24KEVM schematics are provided on the following pages.

Revision History		
REV	ECN Number	Approved

Analog_IO
Analog_IO

2xAIC20
2xAIC20

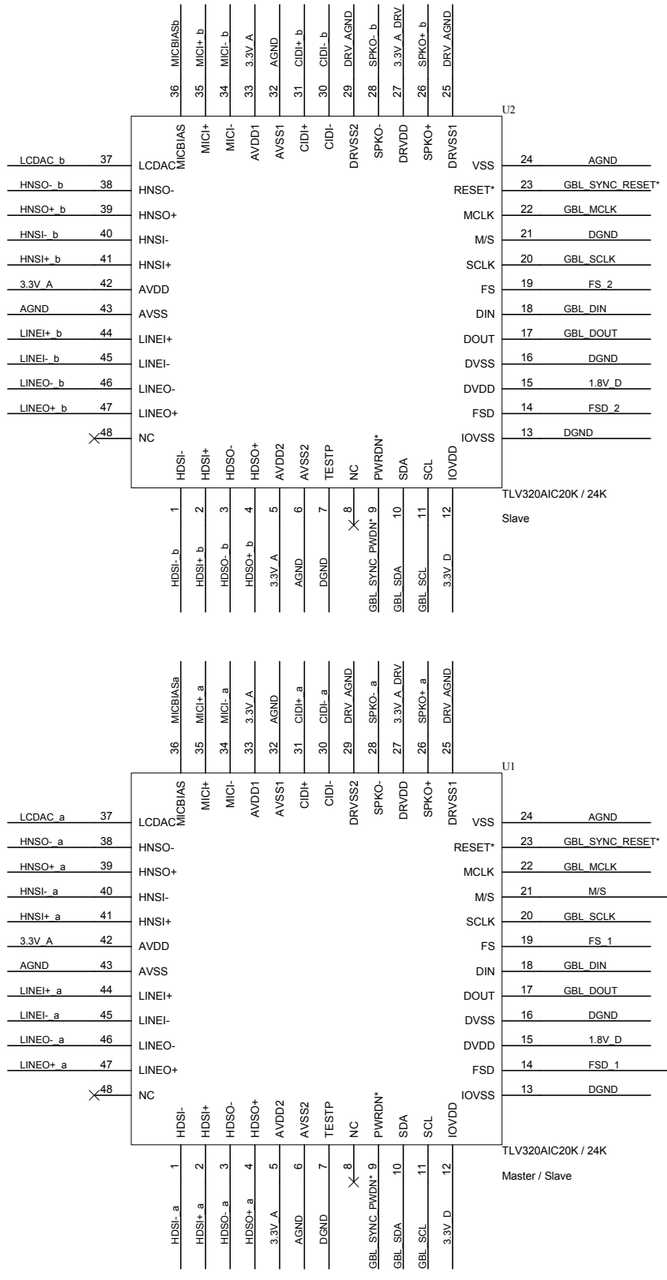
Engineer:	Joe Purvis
Drawn By:	Joe Purvis
FILE:	AIC20 CODEC

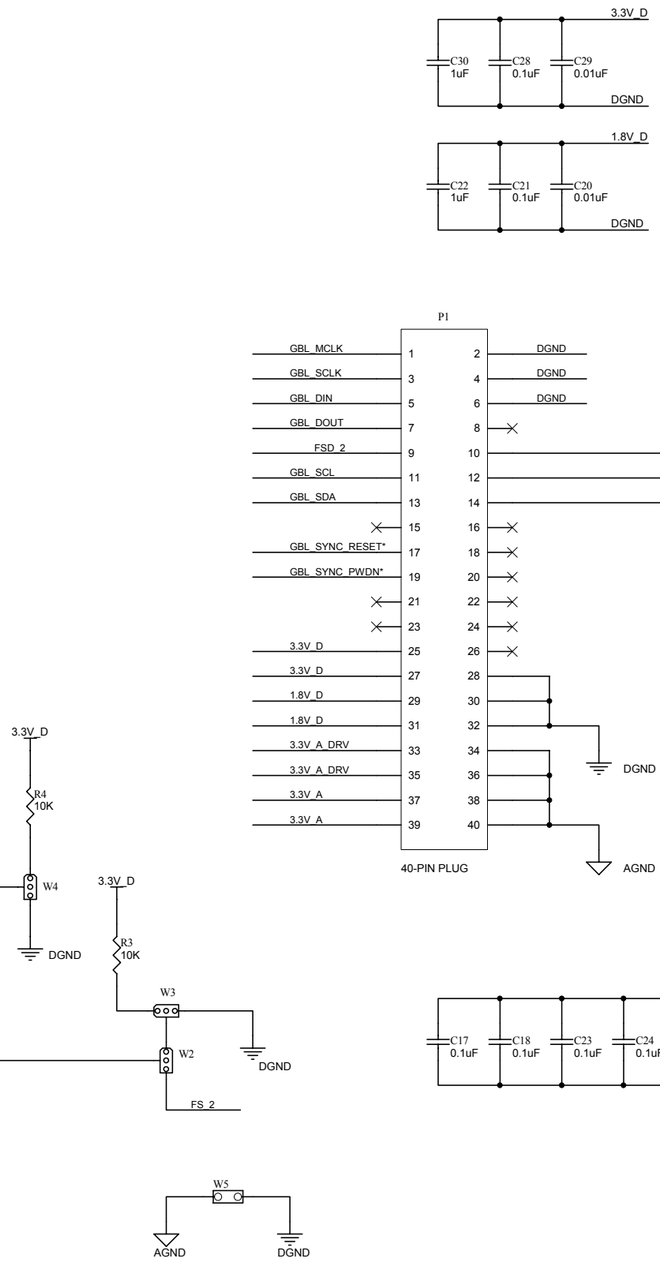
TEXAS INSTRUMENTS

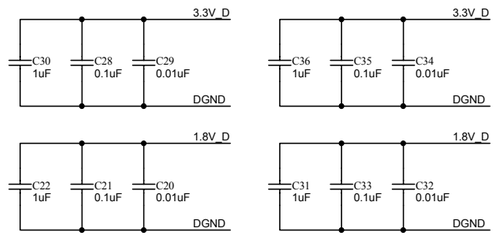
12500 TI Boulevard. Dallas, Texas 75243

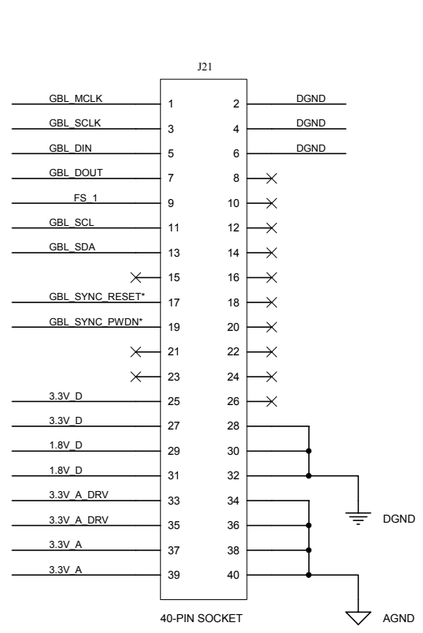
Title: System Block			
DOCUMENTCONTROL # 6442568			REV: A
DATE: 10-Feb-2005	SIZE:	SHEET: 1	OF: 3

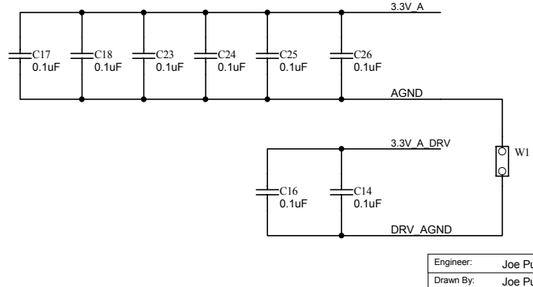
Revision History		
REV	ECN Number	Approved











TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

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Engineer:	Joe Purvis
Drawn By:	Joe Purvis
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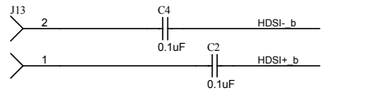

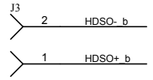

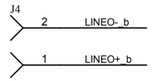

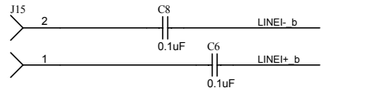

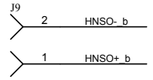

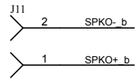

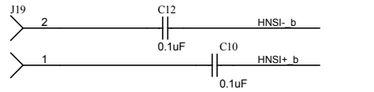

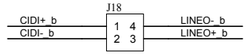

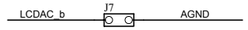

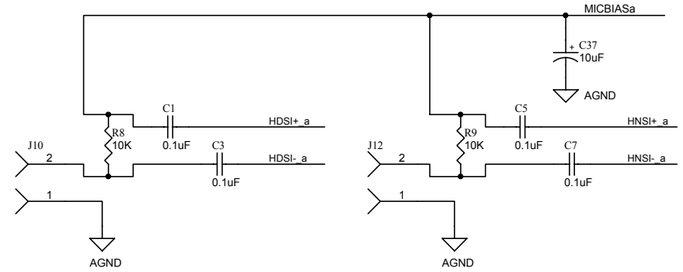

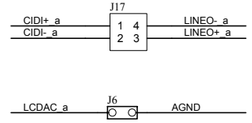

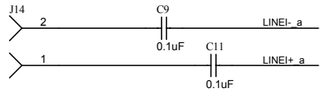

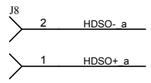

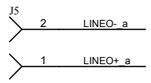

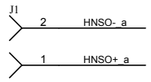

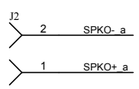

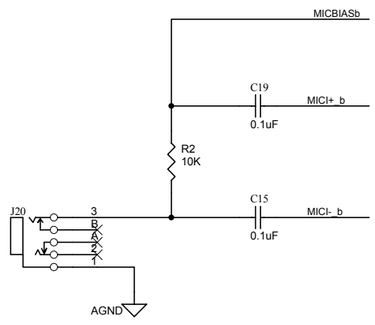

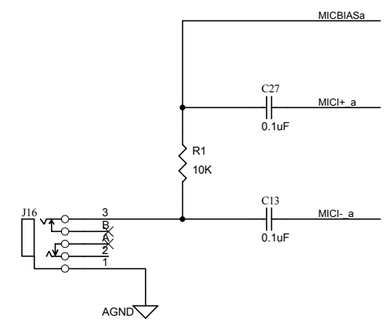

Revision History

REV	ECN Number	Approved

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: Analog I/O			
DOCUMENTCONTROL # 6442568			REV: A
DATE: 10-Feb-2005	SIZE:	SHEET: 3	OF: 3

Engineer:	Joe Purvis
Drawn By:	Joe Purvis
FILE:	Analog_IO