DAC7554 Evaluation Module

User's Guide

Literature Number: SLAU154
March 2005

Texas Instruments

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DAC7554EVM

This user's guide describes the characteristics, operation, and the use of the DAC7554 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram and circuit descriptions are included.

1 EVM Overview

This section gives a general overview of the DAC7554 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

1.1 Features

This EVM features the DAC7554 digital-to-analog converter (DAC). The DAC7554 EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality and performance of the 12-bit resolution, quad-channel and serial input DAC. This EVM features an ultralow glitch voltage output with great linearity and monotonicity. The serial interface of this DAC can communicate with any host microprocessor or TI DSP base system.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The dc power supply requirement for this DAC7554 EVM (VDD) is selectable between 3.3 V and 5 V via W1 jumper header. The 3.3 V comes from J6-8 or J5-1 (if installed), and the 5 V comes from J6-3 or J5-3 terminals (if installed), when plugged in via 5-6k interface card or the HPA449. These power supply voltages are referenced to ground through the J6-6 terminal. The V_{CC} and V_{SS} are only used by U2 operational-amplifier, which ranges from 15 V to -15 V maximum and connects through J1-3 and J1-1 respectively (if installed), or through J6-1 and J6-2 terminals. All the analog power supplies are referenced to analog ground through J1-2 and J6-6 terminals.

The negative rail of the output operational-amplifier, U2, can be selected between V_{SS} and AGND via W5 jumper. The external operational-amplifier is installed as an option to provide output signal conditioning or for other output mode requirement desired.

CAUTION

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The 4.096-V precision voltage reference is provided to supply the external voltage reference and sets the voltage output range of the DAC under test through REF3140, U3, via jumper W4 by shorting pins 1 and 2. The test point TP4 as well as J4-20 are also provided to allow the user to connect to other external reference source if the onboard reference circuit is not desired. The external voltage reference should not exceed the applied power supply, V_{DD}, of the DAC under test.

The REF3140 precision reference is powered by +5VA through J6-4 or J5-3 (if installed) terminal.

CAUTION

When applying an external voltage reference through TP4 or J4-20, make sure that it does not exceed the DAC7554 power supply (V_{DD}) maximum. Otherwise, this can permanently damage the DAC7574, U1, device under test.

1.3 EVM Basic Functions

The DAC7554 EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC7554 DAC. Functional evaluation of the DAC device can be accomplished with the use of any microprocessor, TI DSP or some sort of a waveform generator.

The headers J2 and P2 are the connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC7554 EVM using a custom built cable.

An adapter interface card (5-6k adapter interface) is also available to fit and mate with TI's TMS320C5000™ and TMS320C6000™ DSP Starter Kit (DSK). This alleviates the hassle involved in building a custom cable. In addition, there is also an MSP430 based platform (HPA449) that uses the MSP430F449 microprocessor, with which this EVM can connect and interface. For more details or information regarding the 5-6k adapter interface card or the HPA449 platform, call Texas Instruments or send email to dataconvapps@list.ti.com.

The DAC outputs can be monitored through the selected pins of J4 header connector. All the outputs can be switched through their respective jumpers W2, W11, W12 and W13, for the reason of stacking. Stacking allows a total of eight DAC channels to be used provided that the SYNC signal is unique for each EVM board stacked. The SYNC signal must be decoded for the specific EVM, therefore, the decoder should be implemented but can only be done externally from the EVM board.

In addition, the option of selecting one DAC output that can be fed to the noninverting side of the output operational-amplifier, U2, is also possible by using a jumper across the selected pins of J4. If two EVMs are stacked together, the output operational-amplifier's noninverting input, are shorted together at the J4 header. Alterations to the traces are necessary to use the U2 features. The traces for J4-1, J4-3, J4-5, and J4-7 are visible from the topside of the EVM. However, one issue still remains, the trace to the noninverting pin of U2 cannot be seperated from J4-1. Therefore, only one of the stacked EVMs can be used with the U2 feature. Finally, the output operational-amplifier, U2, must first be configured correctly for the desired waveform characteristic to be seen. See section 4 of this user's guide.

A block diagram of the EVM is shown below in the Figure 1.

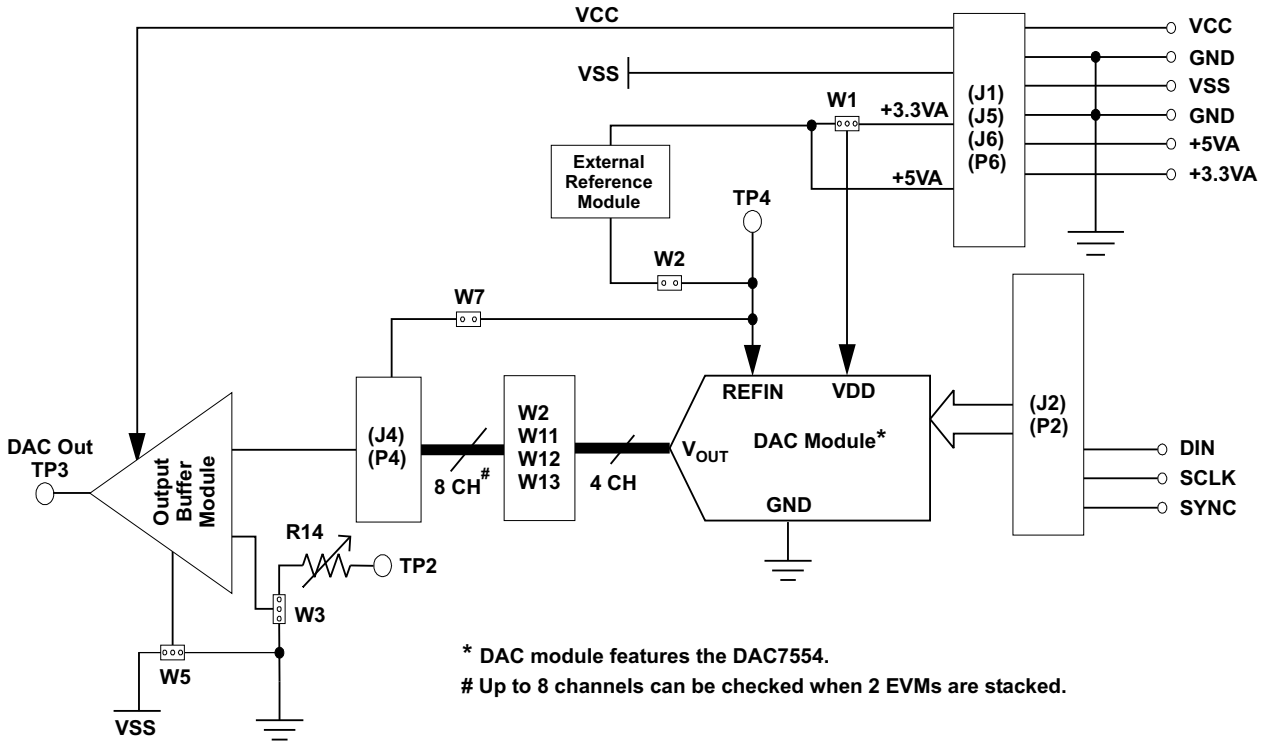


Figure 1. EVM Block Diagram

2 PCB Design and Performance

This section covers the layout design of the PCB; thereby, describing the physical and mechanical characteristics of the EVM. The list of components used on the module is also included in this section.

2.1 PCB Layout

The DAC7554 EVM is designed to preserve the performance quality of the DAC, device under test, as specified in the data sheet. Carefully analyzing the EVM's physical restrictions and the given or known elements that contributes to the EVM's performance degradation is the key to a successful design implementation. These attributes that diminish the performance of the EVM can be addressed during the schematic design phase, by properly selecting the right components and building the circuit correctly. The circuit should include adequate bypassing, identifying and managing the analog and digital signals and knowing or understanding the components mechanical attributes.

The obscure part of the design is the layout process where lack of knowledge and inexperience can easily present a problem. The main concern here is primarily with the placement of components and the proper routing of signals. The bypass capacitors should be placed as close as possible to the pins and the analog and digital signals should be properly separated from each other. The power and ground plane is very important and should be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical, so when solid planes are not possible, a split plane does the job as well. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the biggest possible trace width allowable in the design. These design practice discussed can be seen in the following figures presented below.

The DAC7554 EVM board is constructed on a two-layer printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 43,1800 mm (1.7000 inch) × 81,2800 mm (3.200 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figures 2 through 6 show the individual artwork layers.

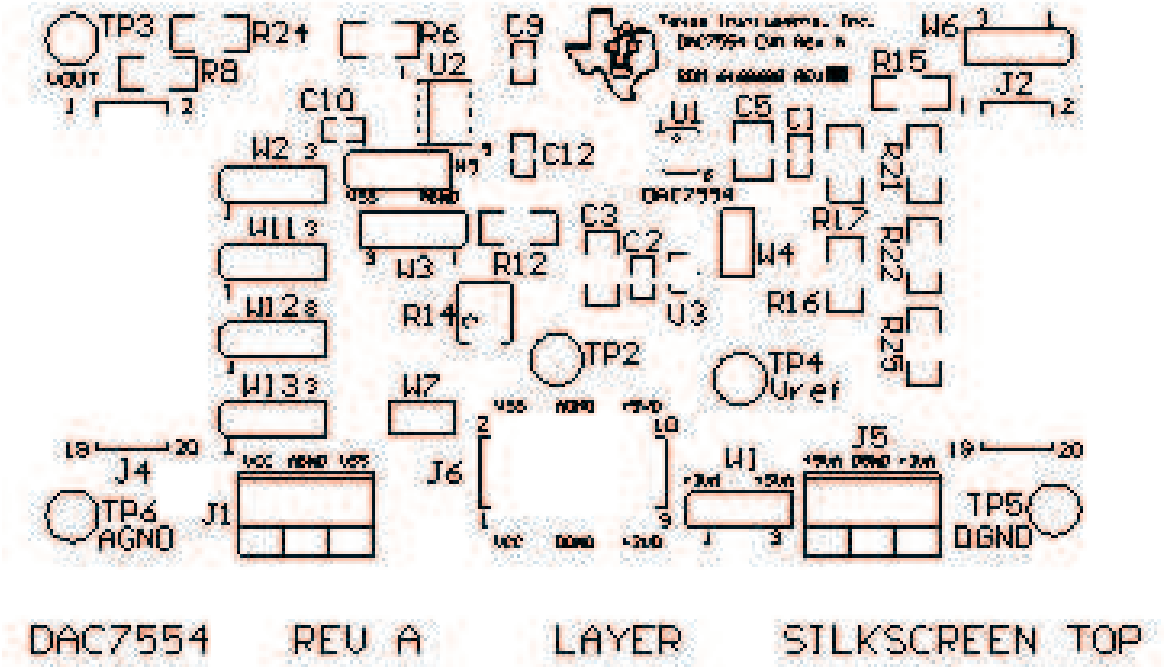


Figure 2. Top Silkscreen

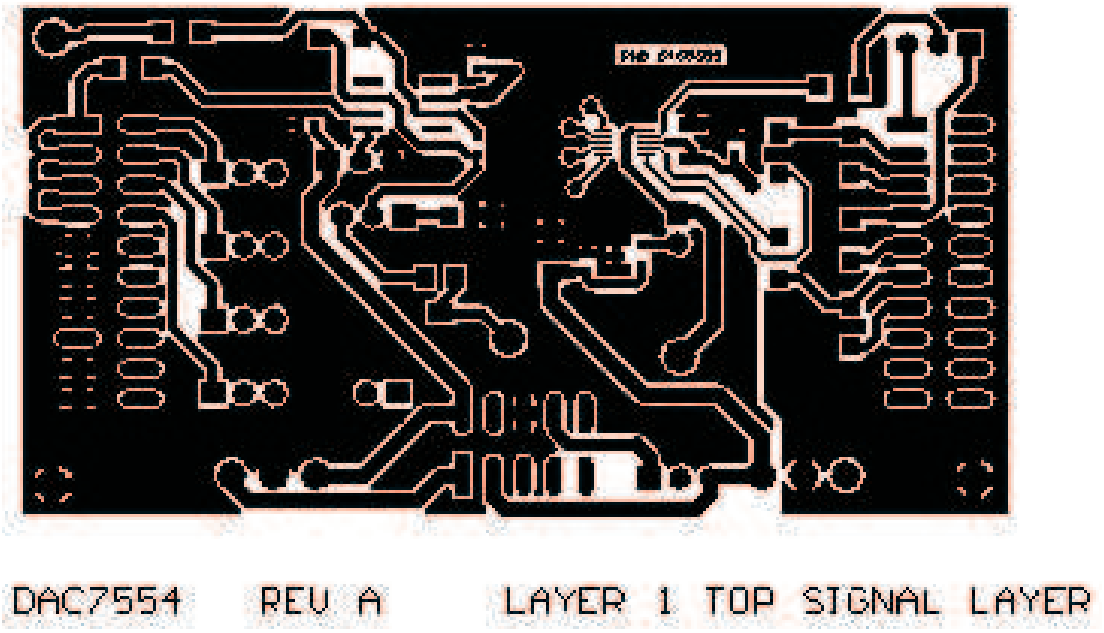


Figure 3. Top Layer (Signal and Split Ground Plane)

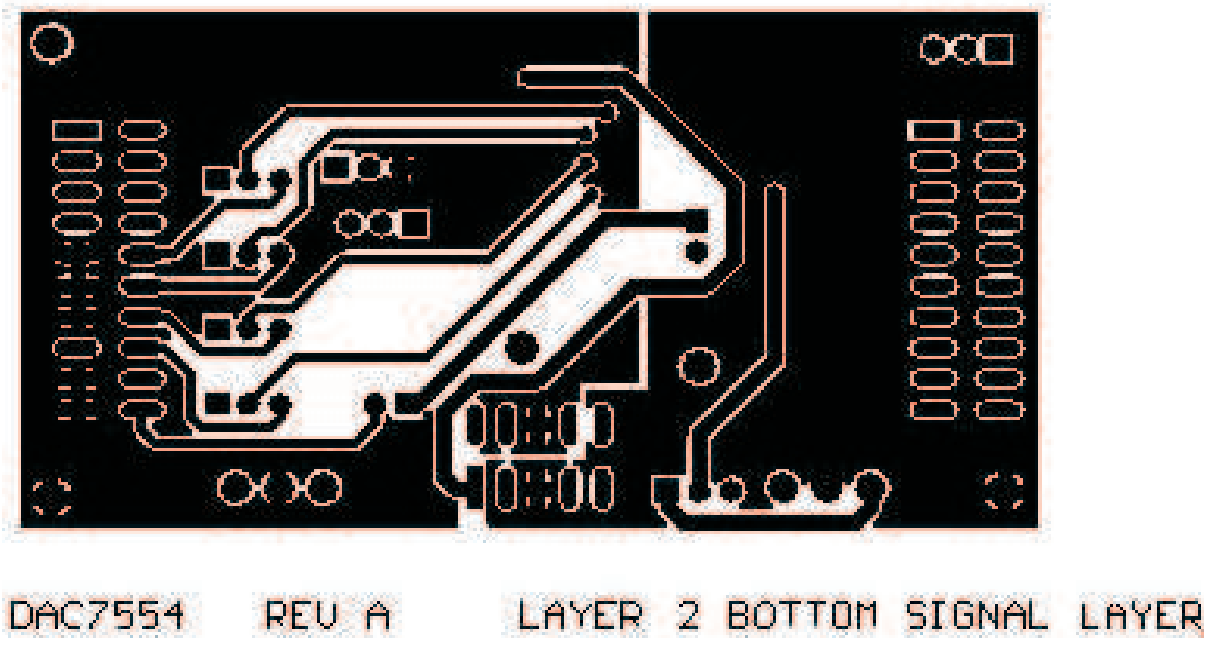


Figure 4. Bottom Layer (Signal and Split Ground Plane)

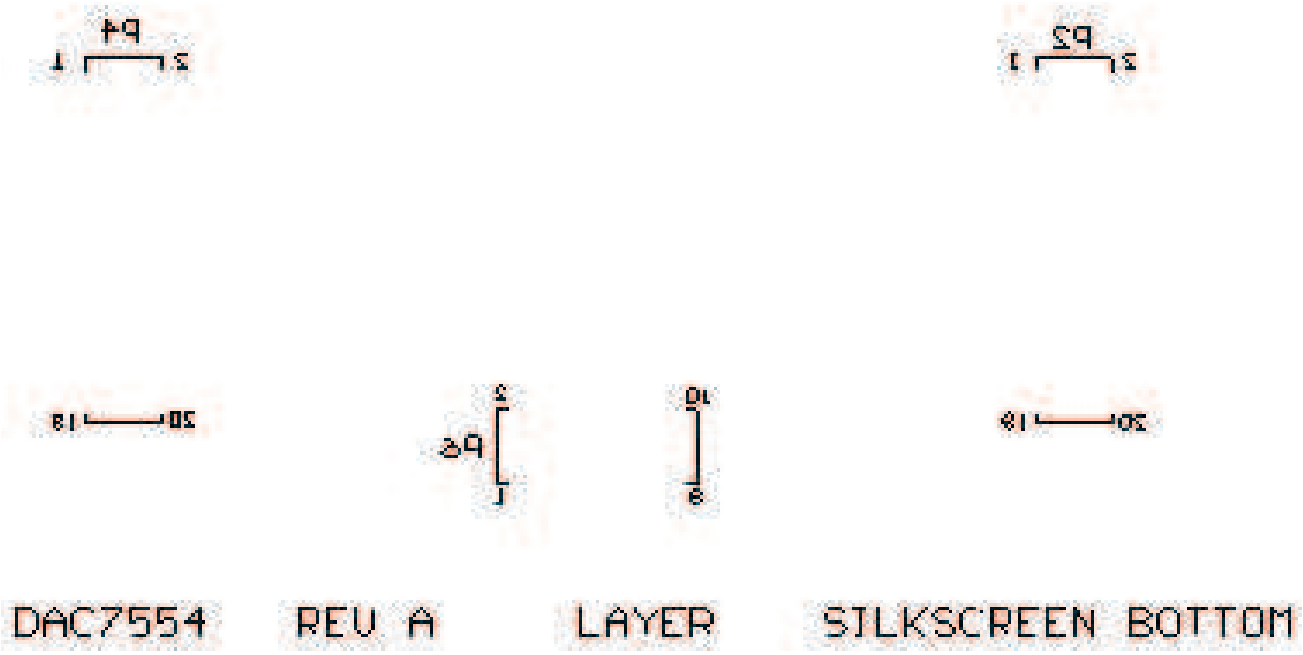


Figure 5. Bottom Silkscreen

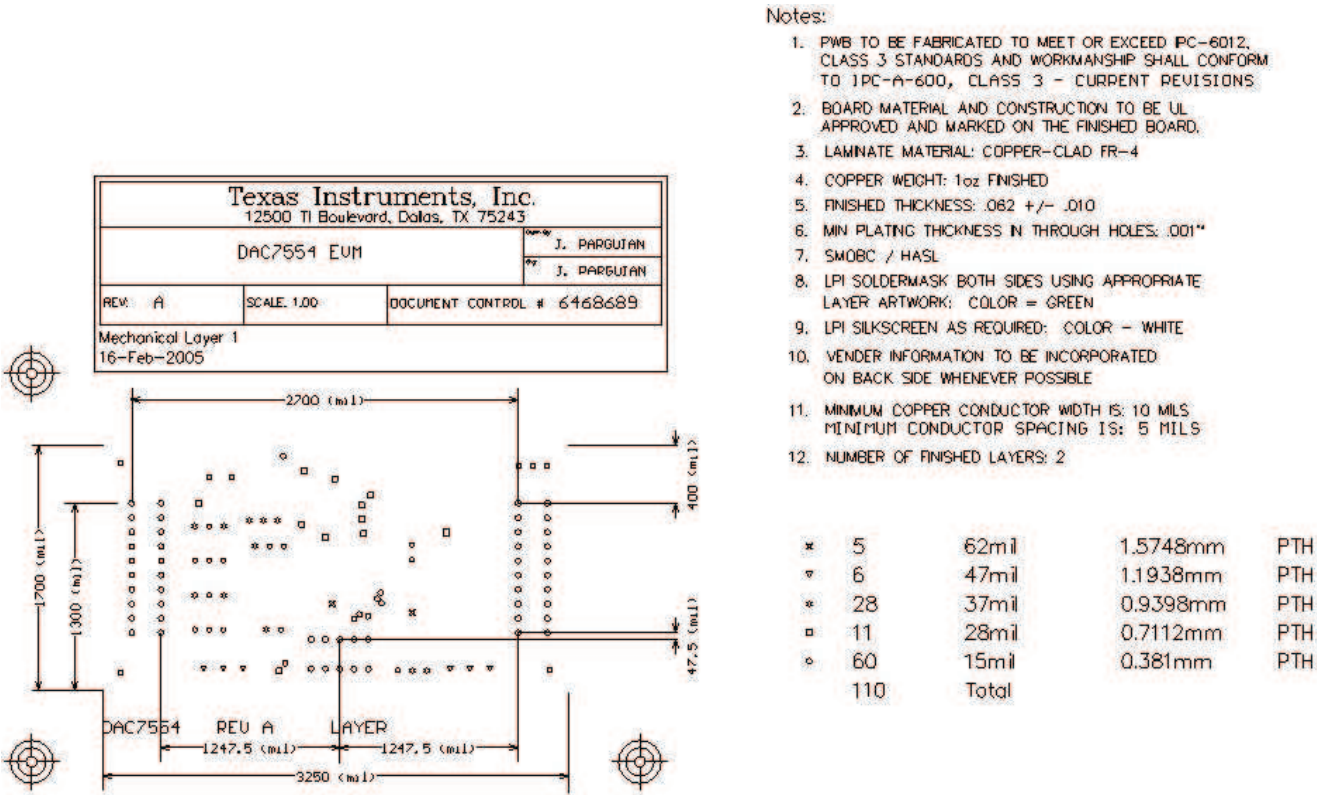


Figure 6. Drill Drawing

3 Bill of Materials

Table 1. Parts List

Item	QTY.	Designators	Description	Manufacturer	MFG. Part No.
1	2	C1, C2	0.1 µF, CAP 25 V, ceramic chip, 0603 SMD	TDK	C1608X7R1E104KT
2	2	C9, C10	0.01 µF, CAP 25 V, ceramic chip, 0603 SMD	TDK	C1608COG1E103KT
3	1	C12	1 nF, CAP 25 V, ceramic chip, 0603 SMD	TDK	C1608COG1E102KT
4	1	C3	0.47 pF, CAP 50 V, ceramic chip, 1206 SMD	TDK	C3216X7R1H474KT
5	1	C5	10 µF, CAP 25 V, ceramic chip, 1210 SMD	TDK	C3225X7R1E106KT
6	2	R6, R12	10K	Panasonic	ERJ-8ENF1002V
7	1	R14	10K POT	Bourns	3214W-1-103E
8	7	R8, R15 R16, R17 R21, R22, R25	0 Ω(1)	Panasonic	ERJ-8GEY0R00V
9	1	R24	100 Ω	Panasonic	ERJ-8GEYJ101V
10	2	J2, J4	20 PIN_IDC	Samtec	TSM-110-01-S-DV-M
11	1	J6	10 PIN_IDC	Samtec	TSM-105-01-T-DV
12	2	J1, J3	3-Pin terminal connector (2)	On-Shore Tech.	ED555/3DS
13	2	P2, P4	20-Pin_IDC(3)	Samtec	SSW-110-22-S-DVS-P
14	1	P6	10-Pin Isolated Power Socket, 0.100 (3)	Samtec	SSW-105-22-F-DVS-K
15	5	TP2, TP3, TP4, TP5, TP6	TP_TURRENT	Mill-Max	2348-2-01-00-00-07-0
16	1	U2	8-SOP(D) High Precision OP-Amp MSOP-10(DGS)	Texas Instruments	OPA277UA
17	1	U1	DAC7554, 12-Bit, 4-CH, SPI	Texas Instruments	DAC7554
18	1	U3	4.096V VOLTAGE REFERENCE SOT23-3	Texas Instruments	REF3140AIDBZT
19	2	W4, W7	2 CIRCUIT HEADER, 0.100 STRAIGHT	Molex	22-03-2021
20	8	W1, W2, W3, W5, W6, W11, W12, W13	3 CIRCUIT HEADER, 0.100 STRAIGHT	Molex	22-03-2031

(1) R21, R22, and R25 are not populated (1206 footprint).
(2) J1 and J3 are optional terminals and are not installed.
(3) P2, P4, and P6 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC board opposite the *J* designated counterpart. Example, J2 is installed on the topside while P2 is installed in the bottom side opposite of J2.

4 EVM Operation

This section covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

Refer to the DAC7554 data sheet, SLAS399A, for information about its serial interface and other related topics.

The EVM board is factory tested and configured to operate in the unipolar output mode.

4.1 Factory Default Setting

The EVM board is set to its default configuration from factory as described on the table below to operate in unipolar mode of operation. The jumper configuration is shown on figure 7 for clarity.

Table 2. Factory Default Jumper Setting

Reference	Jumper Position	Function
W1	2-3	Analog supply for the DAC7554 is +5VA.
W2	1-2	DAC output A ($V_{OUT}A$) is routed to J4-2.
W3	OPEN	External operational-amplifier, U2, is in unity gain configuration.
W4	CLOSED	Onboard external reference, U3, is routed to V_{ref}.
W5	1-2	Negative supply rail of U2 Op-Amp is supplied with V_{SS}.
W6	2-3	CS signal from J2 is routed through to drive the SYNC signal.
W7	OPEN	External reference source from J2-20 is not connected.
W11	1-2	DAC output B ($V_{OUT}B$) is routed to J4-4.
W12	1-2	DAC output C ($V_{OUT}C$) is routed to J4-6.
W13	1-2	DAC output D ($V_{OUT}D$) is routed to J4-8.
J4	1-2	DAC output A ($V_{OUT}A$) is connected to the noninverting input of the output operational-amplifier, U2.

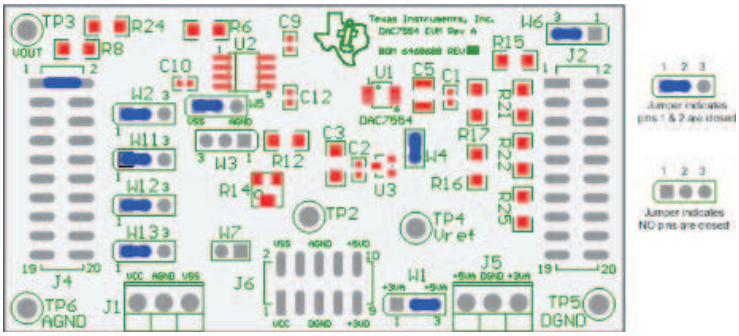


Figure 7. Factory Default Jumper Setting

4.2 Host Processor Interface

The host processor will basically drive the DAC, so the DACs proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J4 header connector.

An interface adapter card is also available for specific TI DSP starter kit as well as an MSP430 based microprocessor as mentioned in chapter 1 of this manual. Using the interface card alleviates the tedious task of building customize cables and allows easy configuration of a simple evaluation system.

The DAC7554 interfaces with any host processor capable of handling serial communication protocols or the popular TI DSP. For more information regarding the DAC7554 data interface, please refer to the data sheet (SLAS399A).

4.3 EVM Stacking

The stacking of EVM is possible if there is a need to evaluate two DAC7554 to yield a total of eight channel output. A maximum of two EVMs are allowed since the output terminal, J4, dictates the number of DAC channels that can be connected without colliding. Table 3 shows how the DAC output channels are mapped into the output terminal, J4, with respect to the jumper position of W2, W11, W12 and W13.

Table 3. DAC Output Channel Mapping

Reference	Jumper Position	Function
W2	1-2	DAC output A ($V_{OUT}A$) is routed to J4-2.
	2-3	DAC output A ($V_{OUT}A$) is routed to J4-10.
W11	1-2	DAC output B ($V_{OUT}B$) is routed to J4-4.
	2-3	DAC output B ($V_{OUT}B$) is routed to J4-12.
W12	1-2	DAC output C ($V_{OUT}C$) is routed to J4-6.
	2-3	DAC output C ($V_{OUT}C$) is routed to J4-14.
W13	1-2	DAC output D ($V_{OUT}D$) is routed to J4-8.
	2-3	DAC output D ($V_{OUT}D$) is routed to J4-16.

To allow exclusive control of each EVM when they are stacked together, each DAC7554 EVM must have its own unique SYNC signal. This is accomplished by implementing a decoder externally from the EVM board or the µC or DSP can generate each specific SYNC signal for the appropriate EVM board in the stack. These specific SYNC signals that comes into J2-1 and J2-7 must be selected via the jumper W6 of each EVM board.

4.4 The Output Operational Amplifier

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. Only one DAC output channel can be monitored at any given time for evaluation since the odd numbered pins (J4-1 to J4-7) are tied together. When the EVM board output operational-amplifier is used, the traces must be properly cut. The traces are visible on the edge of the EVM from the topside where the J4 header is assembled. The pin J4-1 on the EVM should not be used and should be left open because all the traces come to this point. This provides three other options (i.e., J4-3, J4-5, and J4-7) that can be used for signal routing and the other two unused traces should be cut. This option does not apply when stacking two EVMs, see section 1.3.

Nevertheless, the raw outputs of the DAC can be probed through the even pins of J4, the output terminal, which also provides mechanical stability when stacking or plugging into any interface card. In addition, it provides easy access for monitoring up to eight DAC channels when stacking two EVMs together. See section 4.3.

The following sections describes the different configurations of the output amplifier, U2.

4.4.1 Unity Gain Output

This is the default configuration that the EVM is set to from the factory. The buffered output configuration can be used to prevent loading the DAC7554 though it may present some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match their desired wave shape by simply desoldering R7 and C11 and replacing it with the desired values. You can also simply get rid of R7 and C11 altogether and just solder a zero ohm resistor in replacement of R7, if desired.

Table 4 shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar or bipolar mode.

Table 4. Unity Gain Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	OPEN	OPEN	Disconnect R12 (gain resistor) or any signals attached in TP2 from the inverting input of the operational-amplifier.
W5	2-3	1-2	Supplies V_{SS} to the negative rail of operational-amplifier or ties it to AGND.

4.4.2 Output Gain of Two

Table 5 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

Table 5. Gain of Two Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	1-2	1-2	Inverting input of the output operational-amplifier, U2, is connected to the gain resistor R12.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of operational-amplifier, U2, for bipolar mode, or ties it to AGND for unipolar mode.

4.4.3 Adding an Offset to the Output Operational-Amplifier

Another output configuration option is the capability to add an offset to the inverting input of the output operational-amplifier, U2. This is done by applying a voltage source into TP2 and adjusting the variable pot to the desired offset level. Table 6 shows the jumper setting configuration for adding an offset voltage.

Table 6. Jumper Settings to Add an Offset to the Output Op-amp

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	2-3	2-3	The offset voltage source is connected to the inverting input of the output operational-amplifier, U2.
W5	2-3	1-2	Supplies power, VSS, to the negative rail of operational-amplifier, U2, for bipolar mode, or ties it to AGND for unipolar mode.

4.5 Jumper Setting

Table 7 shows the function of each specific jumper setting of the EVM.

Table 7. Jumper Setting Function

Reference	Jumper Setting	Function
W1		3.3-V analog supply is selected for DUT V_{DD}.
		5-V analog supply is selected for DUT V_{DD}.
W2		Routes V_{OUT}A to J4-2.
		Routes V_{OUT}A to J4-10.
W3		Connects the gain resistor, R12, to the inverting input of the output operational-amplifier, U2. Use for 2x gain configuration.
		Configures the output operational-amplifier, U2, for unity gain.
		Connects any voltage source applied to TP2 to the inverting input of the output operational-amplifier, U2 for offsetting intentions.
W4		Routes the onboard 4.096-V reference to the V_{ref} input of the DAC7554.
		Disconnects the onboard +4.096V reference from the V_{ref} input of the DAC7554 and allows other external reference source to be applied via TP4 or J4-20 (with W7 closed).
W5		Negative supply rail of the output operational-amplifier, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output operational-amplifier, U2, is tied to AGND for unipolar operation.
W6		FSX signal from J2-7 is routed through to control the SYNC function of the DAC7554. Normally used for DSP operation.
		CS signal from J2-1 is routed through to control the SYNC function of the DAC7554. Normally used for µC operation.
W7		Disconnects the external reference source from J4-20 to the V_{ref} input of the DAC7554 and allows other external reference source to be applied via TP4 or from the onboard reference (with W4 closed).
		Routes the external reference source from J4-20 to the V_{ref} input of the DAC7554.

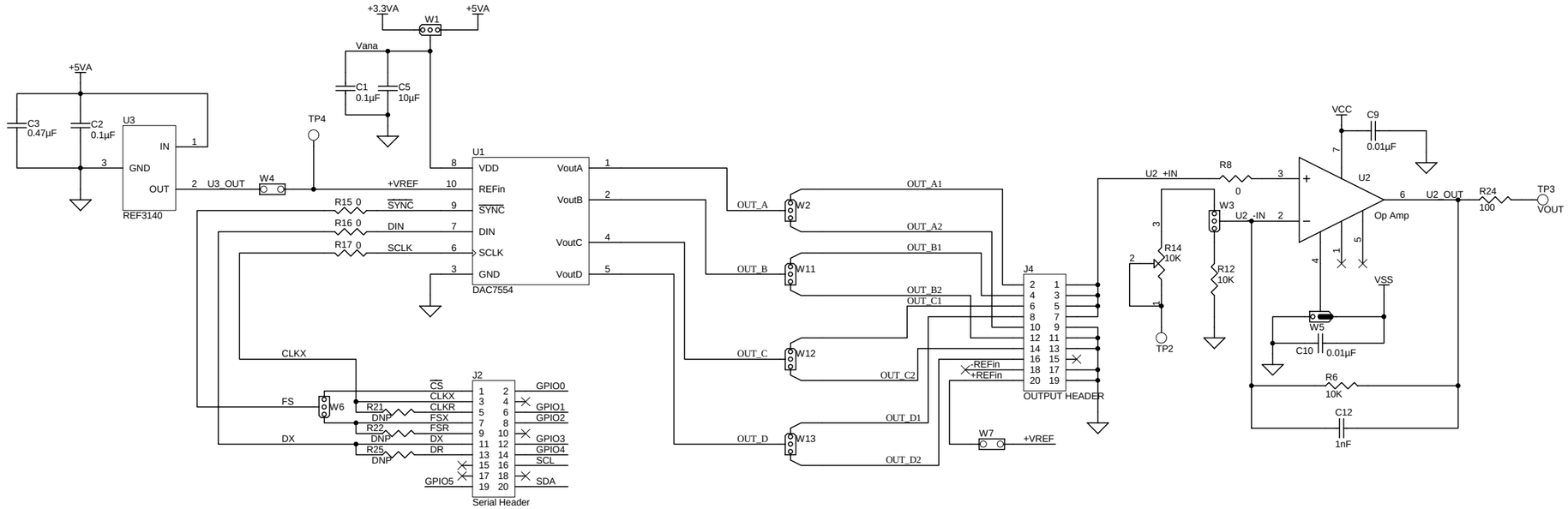
Table 7. Jumper Setting Function (continued)

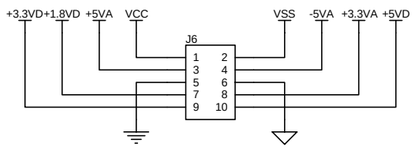
Reference	Jumper Setting	Function
W11		Routes $V_{OUT}B$ to J4-4.
		Routes $V_{OUT}B$ to J4-12.
W12		Routes $V_{OUT}C$ to J4-6.
		Routes $V_{OUT}C$ to J4-14
W13		Routes $V_{OUT}D$ to J4-8.
		Routes $V_{OUT}D$ to J4-16.
Legend:		Indicates the corresponding pins that are shorted or closed.

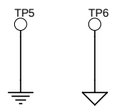
4.6 Schematics

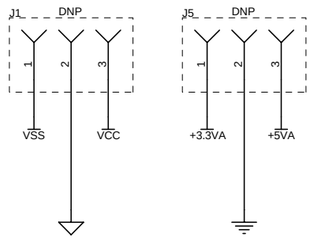
The DAC7554 schematics are shown on the following page.

Revision History		
REV	ECN Number	Approved









Notes:

DNP = Do Not Populate
VCC = +15V Analog Max
VDD = +2.7V to +5.5V Digital Max
VSS = 0V to -15V Analog Max

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Title: DAC7554 EVM			
Engineer: J. PARGUIAN	DOCUMENTCONTROL # 6468690		REV: A
Drawn By:			
FILE: DAC7554 Rev A.Sch	DATE: 14-Feb-2005	SIZE:	SHEET: 1 OF: 1

5 Related Documentation From Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center (PIC) at (972) 644–5580. When ordering, identify this manual by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

Data Sheets:	**Literature Number:**
DAC7554	SLAS399A
REF3140	SBVS046A
OPA277	SBOS079

5.1 Questions About This or Other Data Converter EVMs?

If you have questions about this or other Texas Instruments Data Converter evaluation modules, feel free to e-mail the Data Converter Application Team at dataconvapps@list.ti.com. Include in the subject heading the product you have questions or concerns with.

Trademarks

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Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

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TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.3 V to 5 V and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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