Texas Instruments

Application Report

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TUSB1064 Configuration Guide

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ABSTRACT

The TUSB1064 is a linear redriver that supports both USB3.1 Gen 2 up to 10Gbps and DisplayPort 1.4 up to 8.1Gbps over a USB Type-C interface. At these higher data rates, signal integrity issues place limitations on system trace length. The TUSB1064 provides several levels of receive linear equalization to compensate for cable and board loss due to inter-symbol interference (ISI). This document is intended to provide general guidelines on how to use the TUSB1064 in a sink application. The information in this document can also be applied to the TUSB564.

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Trademarks

1 Introduction

The TUSB1064 is a Type-C linear redriver mux intended for Type-C sink applications. The TUSB1064 demultiplexes between DP1.4 lanes and USB3.1 from a single Type-C receptacle. Both DisplayPort and USB standards define a minimum eye height and width at the end of a channel in which a compliant receiver must operate. Longer trace lengths and cables add ISI contributing to the loss of the channel which closes the eye such that the eye height and width are no longer compliant and the receiver cannot reliably recover the data on that channel. The TUSB1064 provides equalization gain to compensate for the board trace and cable loss due to ISI.

2 Equalization Selection

The TUSB1064 used in a sink application enables the system to pass both USB transmitter electrical compliance for USB3.1 Gen1/2 and receiver jitter tolerance compliance testing for USB3.1 Gen1/2 and DisplayPort 1.4. The TUSB1064 recovers incoming data by applying equalization that compensates for the channel loss. The equalization should be set based on the amount of insertion loss of the channel before the TUSB1064 receivers (Pre-Channel). The EQ value of each channel should be set independently based on the loss of the channel, the equalization selection is performed by configuring the EQ[1:0], SSEQ[1:0] and DPEQ[1:0] pins, or through programming the equivalent registers if the device is configured for I2C operation. The equalization values (For USB3.1 Gen2 and DisplayPort HBR3 data rates) are detailed in Table 1. Typical FR-4 trace losses are given in Table 2.

Table 1. TUSB1064 Equalization

Equalization Setting #	USB3.1 UPSTREAM FACING PORTS				USB 3.1 DOWNSTREAM FACING PORTS				ALL DISPLAYPORT LANES		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN @ 2.5GHz (dB)	EQ GAIN @ 5GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN @ 2.5GHz (dB)	EQ GAIN @ 5GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN @ 4.05 GHz (dB)
0	0	0	-0.9	-1.5	0	0	-2.4	-3.0	0	0	-0.3
1	0	R	0.2	0.7	0	R	-1.3	-0.8	0	R	1.6
2	0	F	1.2	2.2	0	F	-0.4	-0.7	0	F	3.0
3	0	1	2.2	3.7	0	1	0.7	2.2	0	1	4.4
4	R	0	3.1	4.7	R	0	1.5	3.3	R	0	5.4
5	R	R	4.0	5.8	R	R	2.5	4.3	R	R	6.5
6	R	F	4.8	6.6	R	F	3.2	5.1	R	F	7.3
7	R	1	5.6	7.4	R	1	4.0	6.0	R	1	8.1
8	F	0	6.3	8.1	F	0	4.8	6.7	F	0	8.9
9	F	R	7.0	8.7	F	R	5.5	7.3	F	R	9.5
10	F	F	7.5	9.2	F	F	6.0	7.8	F	F	10.0
11	F	1	8.1	9.7	F	1	6.6	8.3	F	1	10.6
12	1	0	8.5	10	1	0	7.1	8.6	1	0	11.0
13	1	R	9.1	10.4	1	R	7.6	9.0	1	R	11.4
14	1	F	9.5	10.7	1	F	8.0	9.3	1	F	11.8
15	1	1	9.9	11.1	1	1	8.5	9.7	1	1	12.1

Table 2. Example FR4 Trace Loss

4-mil Wide FR4 PCB Trace Length (Inches)	Loss @ 2.5GHz (0.49dB/inch) (dB)	Loss @ 4.05GHz (0.73dB/inch) (dB)	Loss @ 5GHz (0.87dB/inch) (dB)
1	0.5	0.7	0.9
2	1	1.5	1.7
3	1.5	2.2	2.6
4	2	2.9	3.5
5	2.5	3.7	4.3
6	2.9	4.4	5.2
7	3.4	5.1	6.1
8	3.9	5.9	7
9	4.4	6.6	7.8
10	4.9	7.3	8.7

3 EQ Configuration Example

Figure 1 below provides an example configuration of a sink system using a USB3.1 Gen 2 Hub operating at 10Gbps and a DisplayPort sink operating at 8.1Gbps.

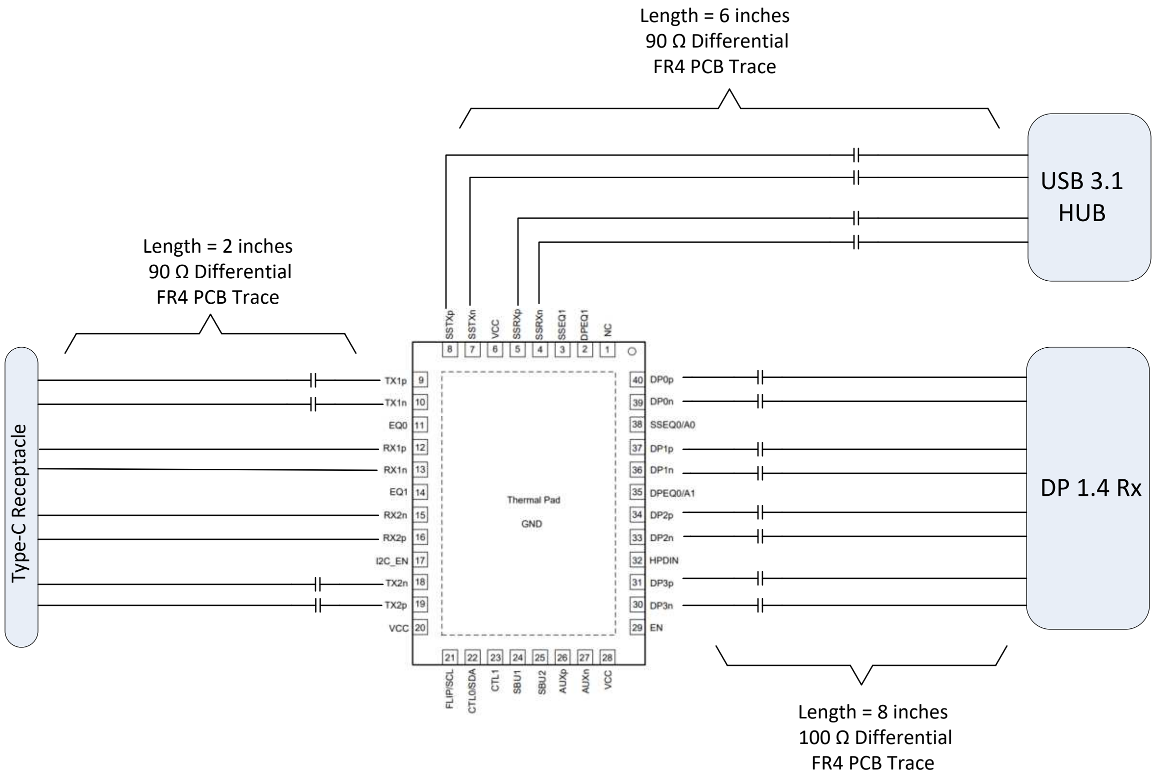

Figure 1. Sink System Trace Length Example

Using the given trace lengths and data rates in this example, the method to select the equalization values for SSEQ, DPEQ and EQ is to select the closest EQ gain value available to match the trace loss as seen as follows.

- USB Hub to TUSB1064 (SSTX) = 6 inches (5.2dB Loss @ 5GHz). SSEQ setting used = Setting #7 (6.0dB).
- DP1.4 RX to TUSB1064 (DP[3:0]) = 8 inches (5.9dB Loss @ 4.05GHz). DPEQ setting used = Setting #5 (6.5dB).
- Type-C Receptacle to TUSB1064 (RX1/2) = 2 inches (1.7dB @ 5GHz). EQ setting used = Setting #2 (3.0dB).

Other factors such as layout quality and Hub/DP driver and receiver quality may require the equalization settings to be adjusted higher or lower for best performance. The above method should be used for selecting initial configuration settings based on system board trace lengths.

For USB3.1 Gen2 Electrical Compliance testing, the USB-IF defines a total loss budget of 23dB with 8.5dB budgeted for the sink system PCB. To help ensure passing of electrical compliance testing, the best practice is to follow the recommended maximum trace lengths for Pre-Channel and Post-Channel. See Figure 2.

- Pre-Channel Maximum Trace Length = 4 inches.
- Post-Channel Maximum Trace Length = 6 inches.

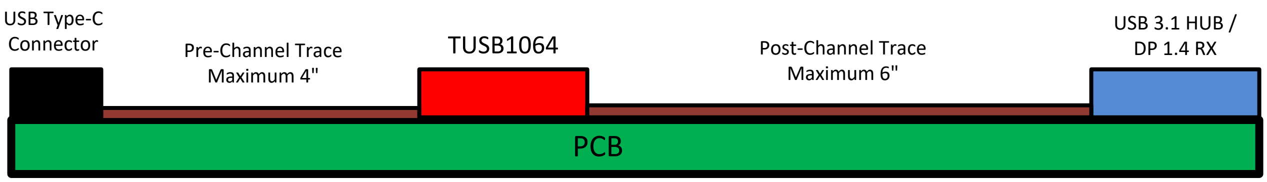

Figure 2. TUSB1064 Placement

4 Device Configuration

The TUSB1064 supports several configuration modes for Type-C applications, Table 3 details the different modes via configuration by pin-strapping, configuration over I2C is also available (See the datasheet for I2C configuration details and register mapping). A typical sink Type-C application uses USB3.1 + DP Alt Mode over Type-C. Table 3 shows an example configuration.

Table 3. TUSB1064 Configuration

CTL1 PIN	CTL0 PIN	FLIP PIN	CONFIGURATION	VESA DisplayPort ALT MODE UFP_D PIN Assignment
L	L	L	Power Down	-
L	L	H	Power Down	-
L	H	L	One Port USB 3.1 - No Flip	-
L	H	H	One Port USB 3.1 - With Flip	-
H	L	L	4 Lane DP - No Flip	C
H	L	H	4 Lane DP - With Flip	C
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip	D
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip	D

5 Layout Guidelines

The following layout guidelines should be used in routing the high-speed USB and DisplayPort signals to and from the TUSB1064.

- RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance (+/- 15%).
- Keep differential pairs away from other high-speed signals.
- Intra-pair routing should be kept to within 2 mils.
- DisplayPort lane inter-pair routing should be kept to within 50 mils.
- Differential pair length matching should be near the location of mismatch.
- Each pair should be seperated by at least 3x the signal trace width.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135º. This will minimize any length mismatch caused by the bends andminimize the impact bends have on EMI.
- Route all differential pairs on the same layer.
- Minimize the number of vias, it is recommended to keep the via count to 2 or less.
- Keep differential traces on layers adjacent to a ground plane.
- Do not route differential pairs over any split plane.
- If using a through-hole connector, route the high-speed signals on opposite side of the connector such

that the connector pin does not create a stub in the transmission line.

5.1 GND Stitching

The entirety of any high-speed signal trace should maintain the same GND reference plane from origination to termination. If the same GND reference plane is not maintained, via-stitch both GND planes together to ensure continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200 mils (Center-to-center, closer is better) of the signal transition vias. See Figure 3 for an example of GND stitching vias.

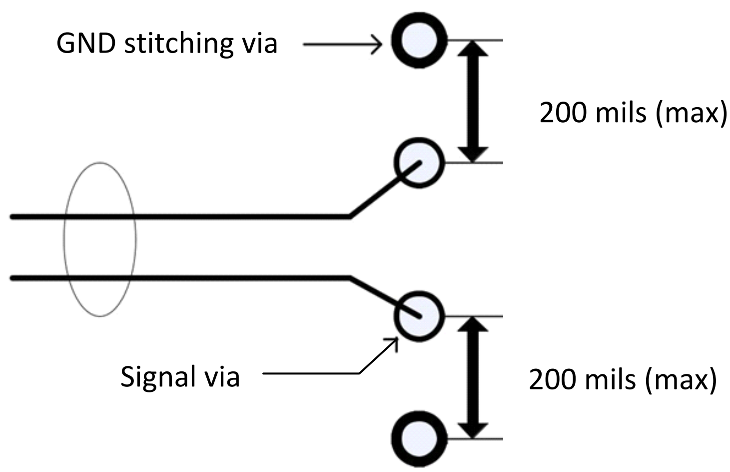

Figure 3. GND Stitching Vias Example

5.2 AC-Coupling Capacitors

When placing AC-Coupling capacitors, the maximum component size used should be 0402. During layout, the AC-Coupling capacitors should be placed close to the transmitter pins of the device with symmetrical placement to ensure optimum signal quality and to minimize reflections. See Figure 4 for AC-Coupling capacitor placement and Figure 5 for AC-Coupling capacitor layout symmetry.

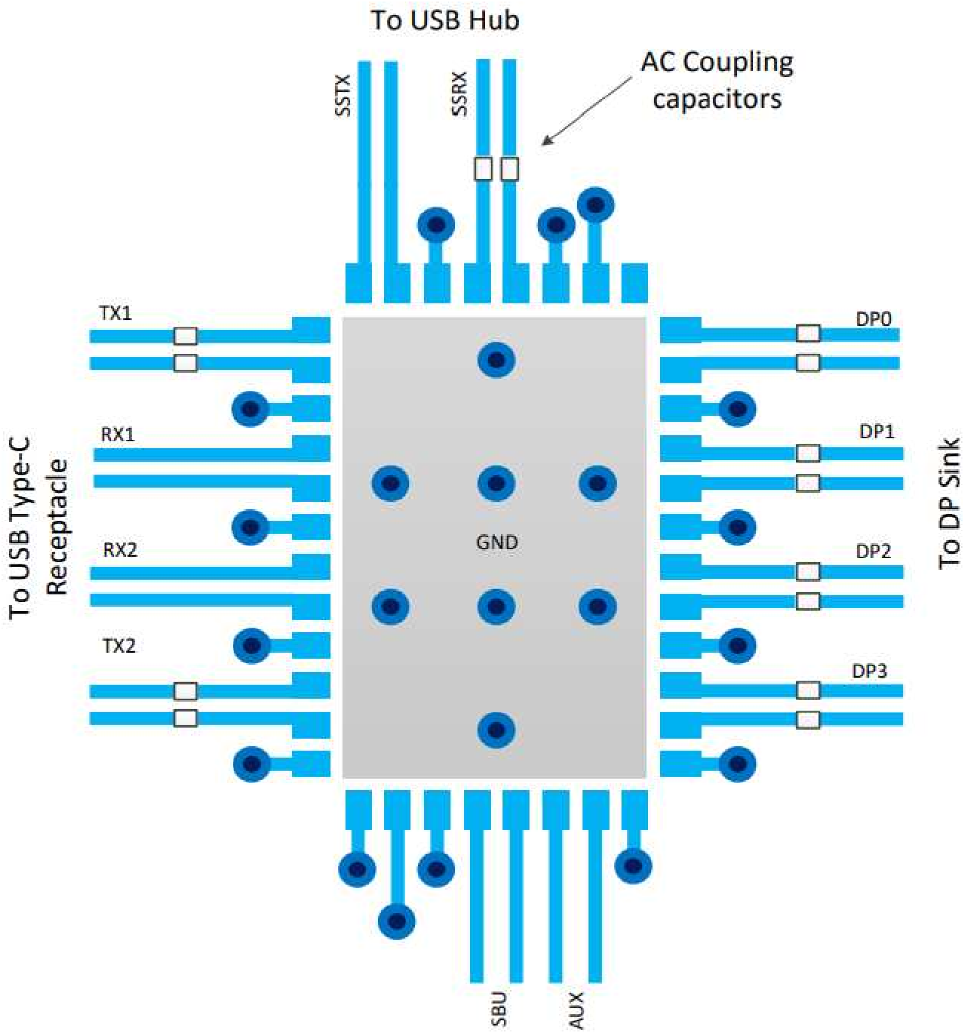

Figure 4. AC-Coupling Capacitor Placement

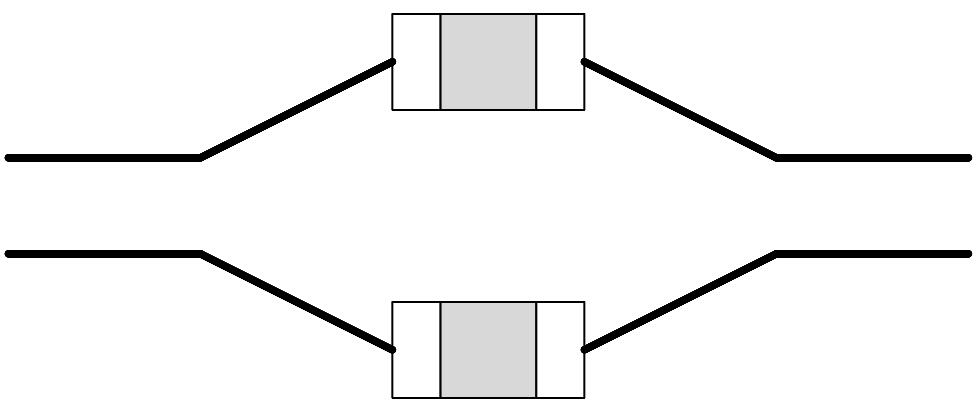

Figure 5. AC-Coupling Capacitor Layout Symmetry Example

NOTE: Adding test points to the high-speed traces can cause impedance discontinuity which negatively impacts signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

6 References

- Datasheet: TUSB1064 Type-C DP Alt Mode 10Gbps Sink-Side Linear Redriver Crosspoint Switch
- Datasheet: TUSB564 USB Type-C DP Alt Mode 8.1Gbps Sink-Side Linear Redriver Crosspoint Switch
- VESA DisplayPort Alt Mode on USB Type-C Standard, Version 1.0a, August 5, 2015