

Layout Guidelines for TPA300x Series Parts

High Performance Linear/Audio Power Amplifiers

ABSTRACT

This article provides a well-reinforced procedure for the PCB layout task as it pertains to the TPA300x series of class D amplifiers. This information can also be used in the layout of the TPA200x series, or any other class D audio amplifier.

This task needs a logical sequence. If we simply jump into the layout task, without understanding how the circuits work, we risk not having an optimal end result. Whether the design engineer does the layout on his or her own or hands the layout task off to the appropriate PCB specialist, there needs to be a clear understanding of the fundamentals of the circuit on the designer's part. As is true in most any engineering practice, there is no unique solution to a given problem. In this case, there is no unique solution to a given layout. However, several unique steps should be followed in order to achieve an optimal solution.

This article has four major parts. The first is the power train analysis and output inductor specification section. This is the most important section as well as the most involved. Second, there is a brief section on noise and grounding. Third, there is a detailed section on the component placement and layout tasks. The fourth section is an EMI mitigation example performed on the same principles illustrated in this document. From front to back this should be a two hour read. More importantly before, throughout, and after the process of building the end product, this application note serves as a reference to the designer.

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1 Introduction

2 Power Train Analysis

The first critical step is to map the power current flow through the system. In this case, the system includes the PCB, V_{CC} /Return header, and the output connections. The first thing that needs to be understood for any switchmode circuit is the current flow through the system in each switch state. Usually there are fixed physical aspects of the board that determine some of this, namely the board dimensions and the placement of the input, output and V_{CC} /Return connections. Once these physical constraints are known, it is important to look at the key elements in the power train and place them so that they can be optimally routed. The routing of every current path in this chain is critical to the over all performance of the amplifier. A good understanding of the operation of the amplifier proves invaluable in the placement task as well as the PCB layout.

Energy is switched from the input decoupling capacitors through the TPA300x, to the filter elements, to the load, through the other filter leg, through $OUT-/OUT+$, through the '300x, and back to the input decoupling capacitors. This power path is lengthy and complex. The nodes involved with this switching action are: Out_{\pm} , P_{vcc} , P_{gnd} . When positioning, it is a good idea to visualize the current flowing through various switching cycles. The switching waveforms and corresponding switch diagrams may serve to clarify the switching intervals and the current paths involved during various switching intervals. The state diagrams below illustrate a positive excursion. For a negative excursion, simply switch the half bridge legs.

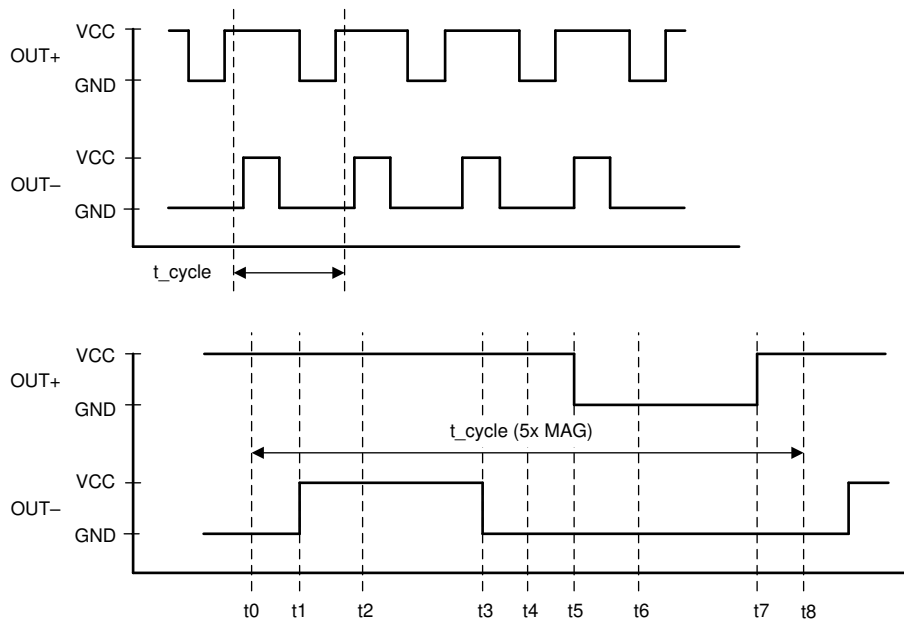


Figure 1. Switching Waveforms

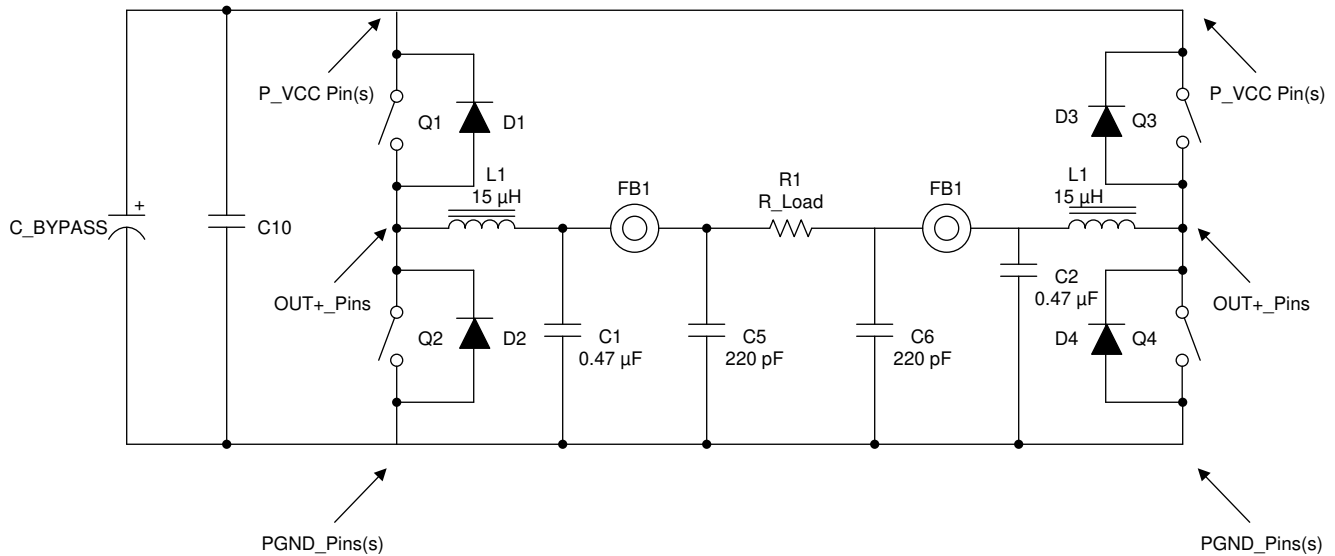
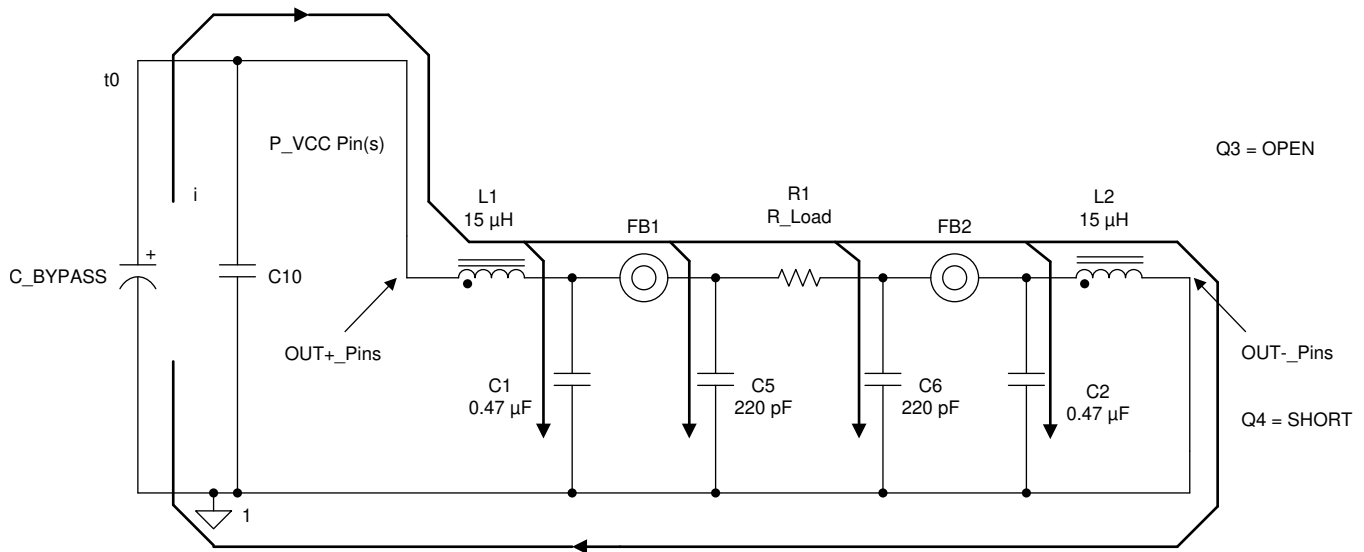
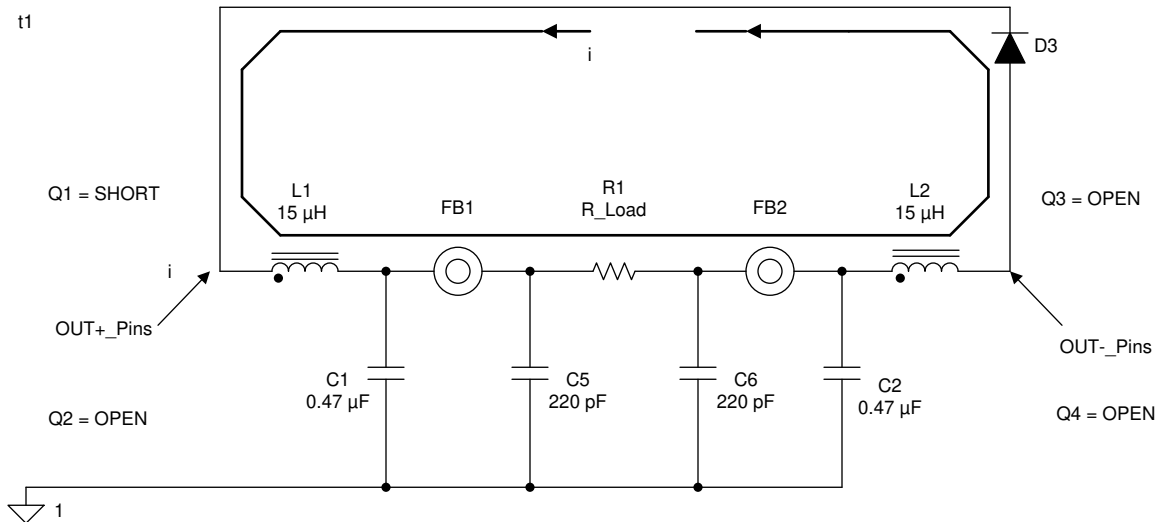


Figure 2. Power Train Schematic For 1 Channel of TPA300x

Note that the MOSFETS (Q1 thru Q4) are modeled with ideal switches, in parallel with ideal diodes (D1 thru D4), for this analysis.


Figure 3. Power Cycle

Time (t_0) is a power cycle. Energy from the decoupling capacitors is switched through the output inductors and through the load. The inductors are charged in this cycle, while the decoupling capacitors are discharged slightly. The current path consists of P_{VCC} , $OUTP$, the output filters, output capacitors, the load, $OUTN$, and P_{gnd} .


Figure 4. Dead Time

Time (t_1) occurs during the dead time between the high side and low side switches in the $OUTN$ leg of the bridge. At this time, both Q_3 and Q_4 are open. Since there is no connection to the decoupling capacitors, this is a freewheel cycle. At this time, both switches are off. The inductors are no longer being driven from the input decoupling capacitors. The current waveform changes slope at this instant. The voltage across the inductors changes instantaneously in an attempt to keep the current flowing. This polarity change forward biases the body diode of Q_3 . The channel of Q_3 is off, however, the body diode is conducting. The current path consists of $P_{V_{CC}}$, $OUTP$, the output filters, the load, and $OUTN$.

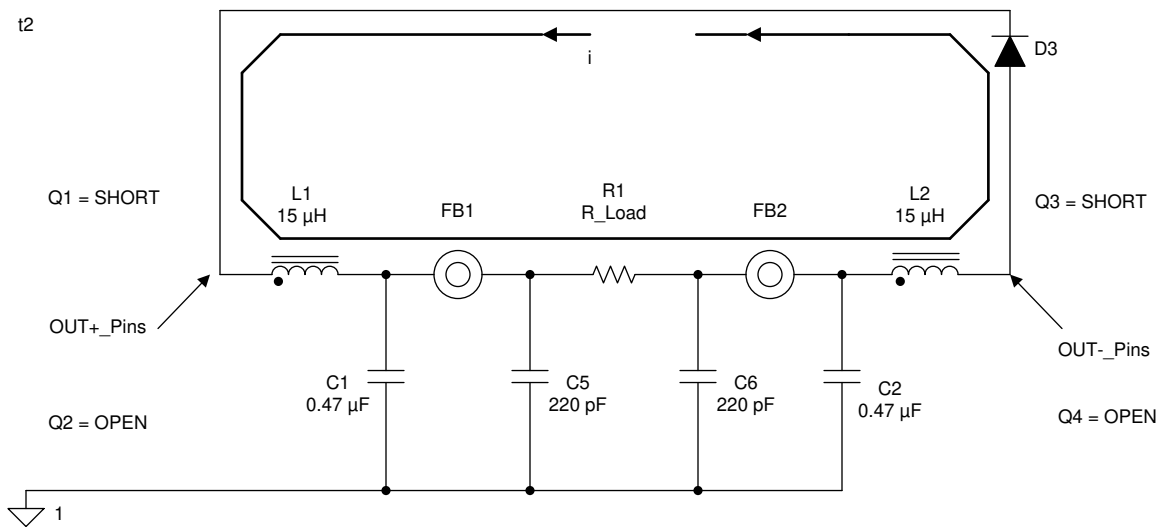


Figure 5. t_2 -Q3 Channel is Turned on

At time t_2 , the channel of Q_3 is turned on. Since current had been flowing through the body diode, the voltage drop across Q_3 is very low (V_f of the body diode) when Q_3 is turned on. The current path consists of PV_{CC} , $OUTP$, the output filters, the load, and $OUTN$.

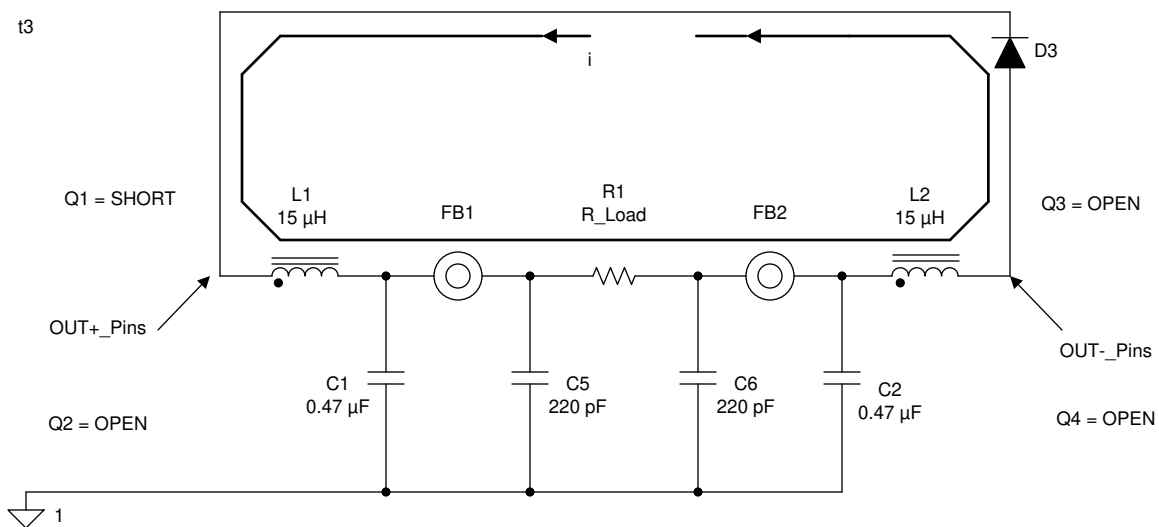


Figure 6. Time t_3 and t_1 - Equivalent Paths

Time t_3 and t_1 are equivalent paths. This is also a transition. The difference lies in the transition to t_4 . The transition from t_1 to t_2 was a soft transition. The output inductors forward biased the body diode of Q_3 before it turned on. In this case, the output inductors source current around the same loop; only the next transition turns on Q_4 . This is a hard transition.

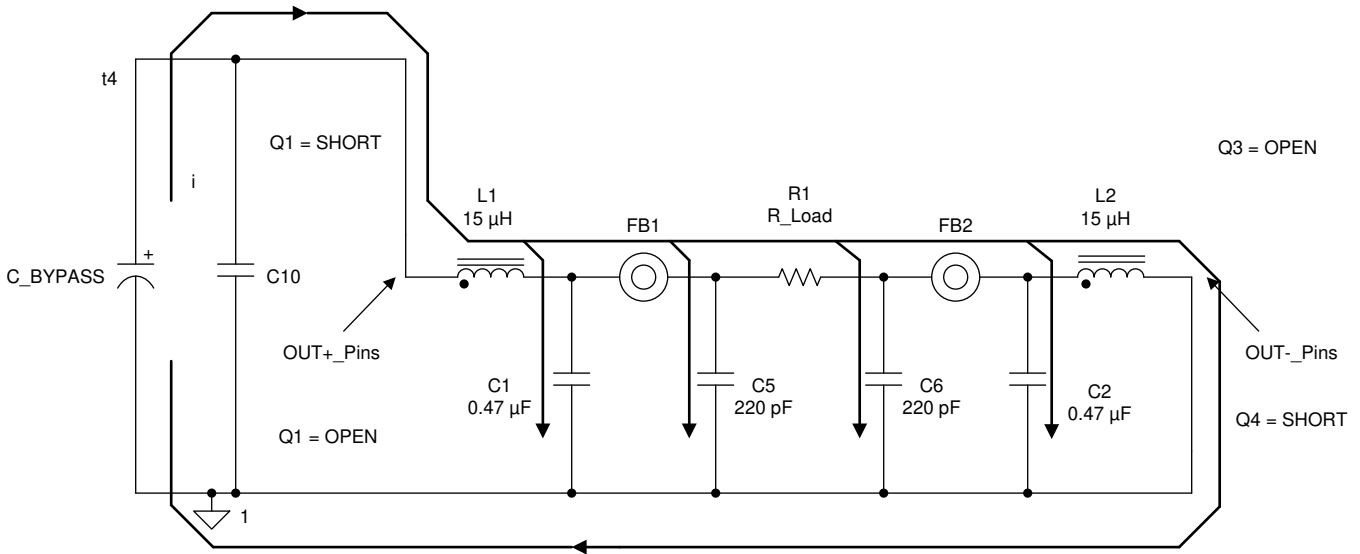


Figure 7. Time t4 Is The Same as t0

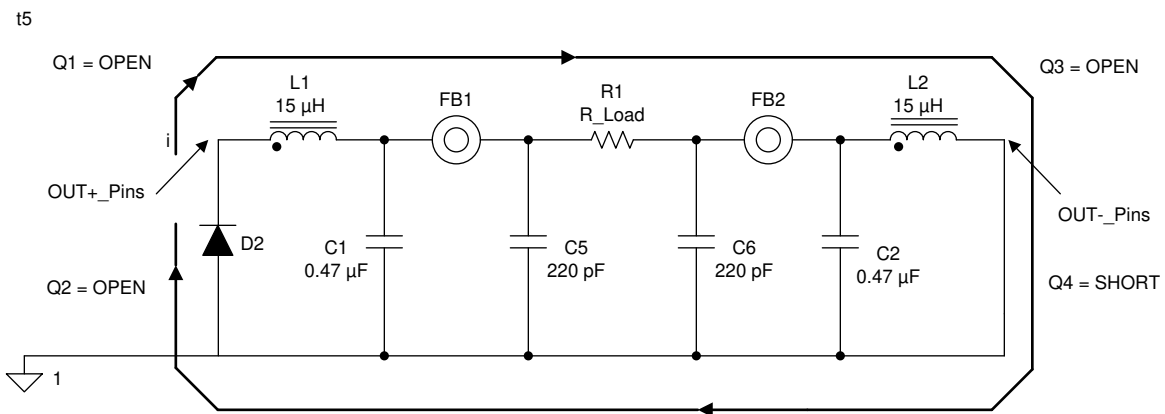


Figure 8. t5-Freewheel Cycle

Time t5 is a freewheel cycle that occurs during the dead time of the OUTP leg of the bridge. At this time, both switches are off in the OUTP leg and the current through the output inductors forward biases the body diode of Q2. The current path consists of P_{gnd}, OUTP, the output filters, the load, and OUTN.

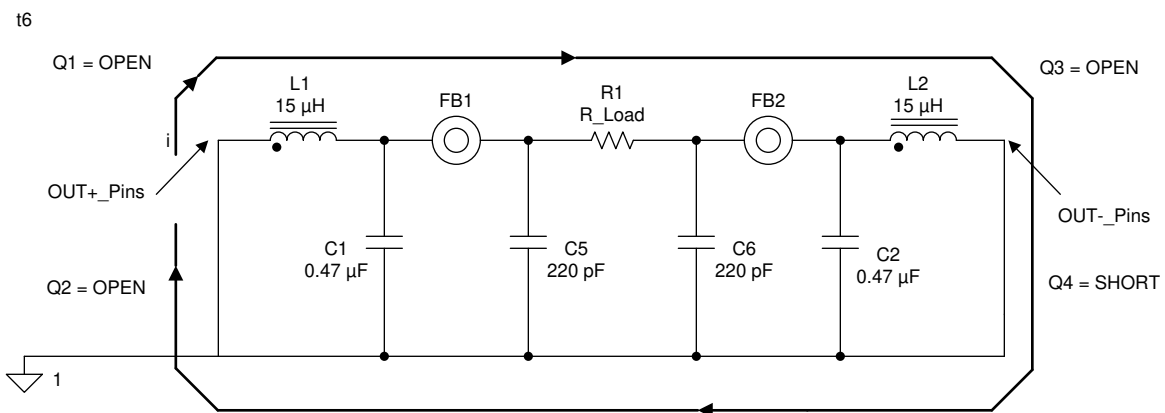


Figure 9. t6-Q2 Is Turned On

At time t6, Q2 is turned on. Since the body diode of Q2 was conducting, the voltage across Q2 is minimal when it is turned on (V_f of the body diode). The current path is the same as t4.

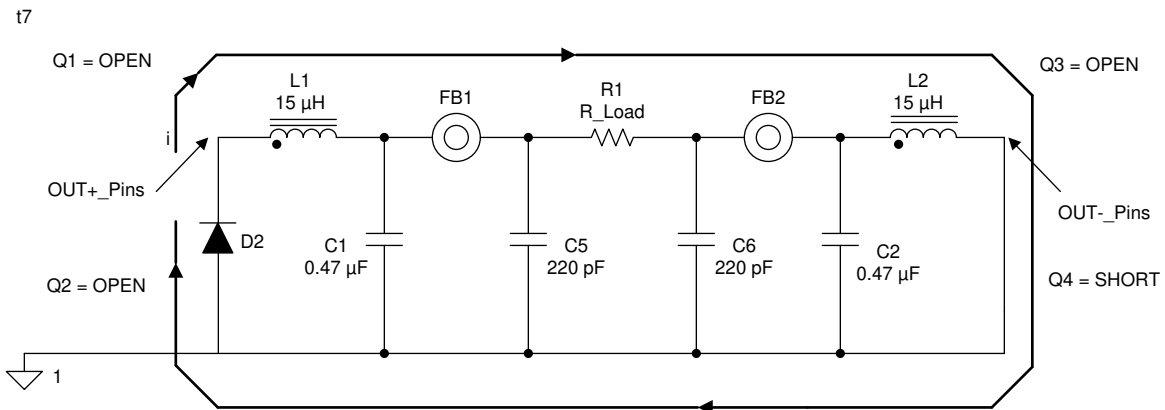


Figure 10. Time t7-Similar to t5

Time t7 is similar to t5. The only exception is in the next cycle. Time t4 to time t5 was a soft transition. Time t6 to t7 is a hard transition. The current path is the same as t5.

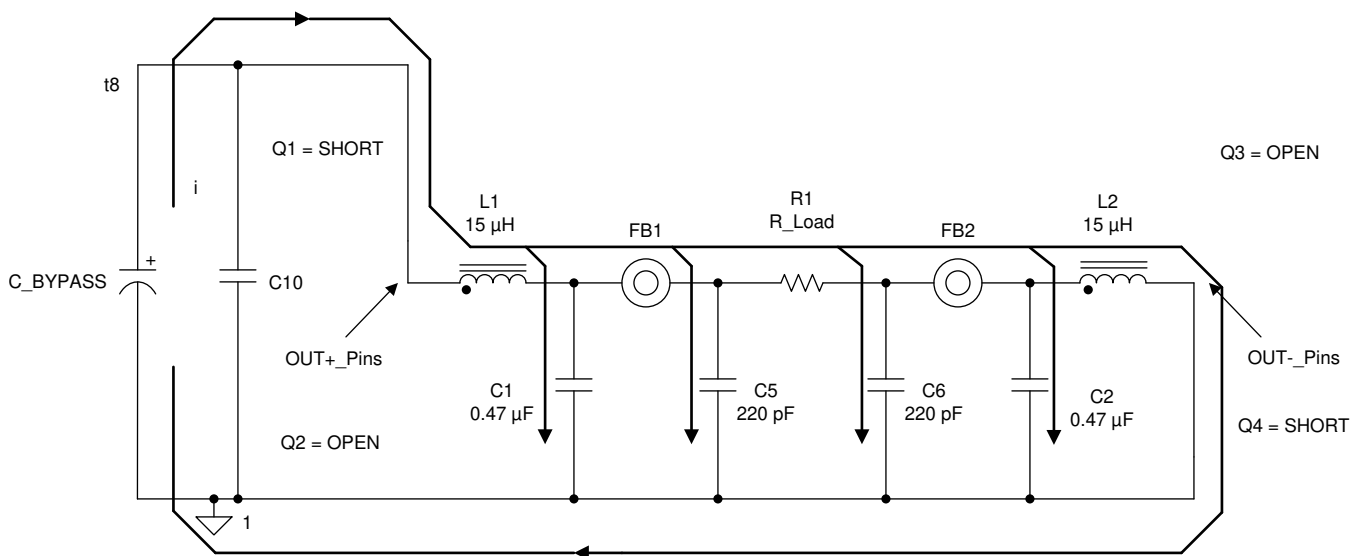
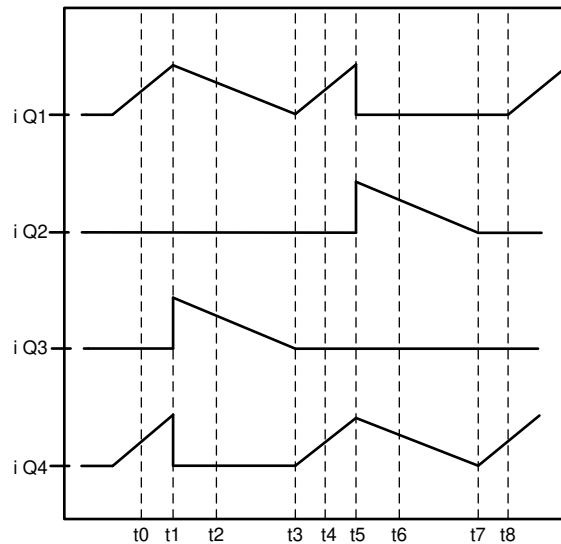


Figure 11. Time t8-A Power Cycle

Time t8 is the same as t0. This is a power cycle having the same current path as t0.

From the previous switching diagrams, the current waveforms through the power transistors are:


Figure 12. Current Waveforms

Note that FB1, FB2, C5, and C6 are for high frequency noise filtering and do not effect the power train operation.

In every switch state above, it is important to understand the role of the filter inductors (L1 and L2). These parts are excited with a square wave from the half bridge legs. We know that an inductor wants to look like a current source, that is, it opposes any change in current.

If we look into Ohm's law for an inductor, we see the equation:

$$V = - \frac{Ldi}{dt} \quad (1)$$

In the case of the switching amplifier, V across the inductor is known with each switch state, L is a constant value, and dt is the time spent in a particular cycle. There is then a dependant variable, di. If we approximate dt as Δt and di as Δi , we can rearrange the approximation:

$$\Delta i = \left(- \frac{V}{L} \right) \times \Delta t \quad (2)$$

This is the ripple current in the output inductor.

From the previous diagrams, it is clear that there are two states for the output inductors. When the inductors are switched to V_{CC} on one leg and ground on the other leg, they are charging. This is a charge cycle. When the output is switched any other way, the inductor begins to discharge, at this point the slope of the current in the inductor changes. The voltage across the inductor reverses polarity at this instant to oppose the change in current flow. We also know that an ideal inductor cannot sustain a dc voltage drop. This means that the volt-time product in the charge state of the inductor is equal to the volt-time product in the discharge state.

Building on the previous example, the duty cycle of OUTP is about 2/3 or 67%. The duty cycle of OUTN is then (1- 2/3) or 33%. If the switching frequency is 250 kHz then $t_{cycle} = 4 \mu s$. Looking at each half bridge leg on its own.

OUTP is tied to V_{CC} for 2.66 μs and then tied to ground for 1.33 μs . OUTN is tied to V_{CC} for 1.33 μs and then tied to ground for 2.66 μs .

Assuming that these duty cycles are steady state, if we look at L1:

- $V \times t \text{ (charge)} = (V_{CC} - VC1) \times 2.66 \mu s$
- $V \times t \text{ (discharge)} = (VC1) \times 1.33 \mu s$

Since these volt-time products are equal, we can combine these two equations to get:

- $VC1 = V_{CC} \times (2.66/4)$

To solve this equation for VC1, we get:

- $VC1 = V_{CC} \times D_{outp}$

This is the dc transfer function of the OUTP leg of this amplifier. In this example, this is $2 V_{CC}/3$.

We can do the same for L2 to get:

- $VC2 = V_{CC} \times (1.33/4)$
- $VC2 = V_{CC} \times (1 - D_{outp})$

In this example, this is $V_{CC}/3$. This is the dc transfer function for the OUTN leg of this amplifier.

So the output voltage across the bridge legs is then:

- $VC1 - VC2$ or $V_{CC}/3$

If we apply equation 2), and there is no interaction between the half bridges, the ripple current in the inductor (L1) is then:

- $\Delta i = ((V_{CC} - 2/3 \times V_{CC}) \times 2/3 \times 4 \mu s)/L1$

which can be simplified to:

- $\Delta i = (2/9) \times (V_{CC} \times t_{cycle}/L1)$

The same is true for L2. For this discussion, if $V_{CC} = 12 V$, $\Delta i = 711 mA$ in both L1 and L2.

Note that the ripple current can not be completely analyzed in this fashion. When the bridge traverses its various states, the inductors are actually charged in series. Due to our proprietary modulation scheme, there are two charge cycles for the inductors for each t_{cycle} . Both of these charge cycles are equivalent as are the discharge cycles. Relative to the output, the frequency is effectively doubled. The interaction between the two half bridge legs serves to reduce the ripple current dramatically.

If we work through this, we see that the inductors are charged in series for $0.66 \mu s$. They then discharge for $1.33 \mu s$. If the output has the same steady state value of $V_{CC}/3$, and we apply equation 2), it becomes clear that the ripple current is:

- $\Delta i = [(V_{CC} - V_{CC}/3) \times 0.66 \mu s]/2 \times L1$

which simplifies to:

- $\Delta i = (2/9) \times (V_{CC} \times t'_{cycle}) / (2 \times L1)$

Note: Due to the output frequency doubling, $t'_{cycle} = (t_{cycle})/2$

In this example, if $V_{CC} = 12 V$, $\Delta i = 177 mA$

By having the bridge legs interleaved, the ripple current dropped by a factor of 4.

While the switch diagrams and equations illustrate the complexity of the power train, the nodes involved are reasonably simple. The output filters, the load, P_{gnd}, P_{V_{CC}}, and the connections to the input decoupling capacitors. These node voltages and mesh currents need to be visualized for proper component placement. As we get beyond the placement task into the layout, the switch diagrams are useful for analyzing mesh currents to use the PCB traces to cancel noise.

2.1 Specifying the Output Inductors

There are a few important parameters that need to be addressed when specifying the output inductors. These specifications are:

- Inductance value
- Current carrying capability
- Saturation current
- Self-resonant frequency
- DC resistance (DCR)
- Max Volt-time product ($V \times \mu s$)

The current carrying capability is usually specified as two different values: I_{RMS} and I_{sat} . I_{RMS} is clearly the RMS current that the part can withstand. I_{sat} varies from manufacturer to manufacturer. It is usually specified as the dc current value that causes the inductance to drop 10%. Recall, a totally saturated inductor has a permeability of $1.0 \mu_0$, the same as free space, while the permeability of the core in an unsaturated state is much higher. Since μ is proportional to inductance, we can conclude that a saturated inductor has minimal inductance. This minimal inductance can cause excessive ripple currents in the bridge switches and premature failure of the TPA300x.

The worst-case I_{RMS} in our output is the root of the sums of the squares of peak output current as seen by the load and the RMS ripple current in the inductor. We use the peak output current because the amplifier may have to source this current to the load for several cycles in clipping. The saturation current indicates the maximum dc stress that the inductor can handle in a dc circuit.

$$I_{RMS} \text{ (worst case)} = \sqrt{\left[\left(\frac{V_{CC}}{RI}\right)^2 + \left(\frac{\Delta i}{\sqrt{3}}\right)^2\right]} (A_{RMS})$$

$$I_{peak} \text{ (worst case)} = \left(\frac{V_{CC}}{RI}\right) + \left(\frac{\Delta i}{2}\right) (A_{peak}) \quad (3)$$

In our example, if the load has a 4- Ω DCR, this is 3.002 A_{RMS} , and 3.11 A_{peak} .

The self resonant frequency (SRF) of the inductor is the parallel resonant frequency of the part. This exists due to the parasitic capacitance between the windings. At frequencies above the SRF, the inductor looks like a coupling capacitor. This frequency should be much higher than the switching frequency of the amplifier.

- SRF > 10 \times fsw

The volt-time product indicates how much stress the inductor can handle in the AC domain. Recall that any given inductor in a circuit has a BH curve. The curve has a linear region and a saturated region. For the purpose of this discussion, I_{sat} determines the H axis boundary, and B_{sat} determines the B axis boundary. B is proportional to the volt-time product seen by the core. Most inductor manufacturers do not readily specify this data in their data sheets. I strongly suggest verifying that the inductor you choose is specified to safely handle the volt time product applied.

- Volt \times time = worst case on time $\times V_{CC}$ [V \times μ s]

In our example, the core needs to withstand a max volt \times time product of 48 V \times μ s.

The DCR should be kept to a minimum to maximize output swing under load.

Summary of specifications:

- I_{RMS} (worst case) = 3.002 A
- I_{peak} (worst case) = 3.11 A
- SRF > 5 MHz
- Max V \times t = 48 V \times MM μ s

For the sake of margin, TI recommends an inductor with an I_{sat} rating of greater than 4.5 A, an I_{RMS} rating of 4 A, an SRF above 2.5 MHz, and a max volt-time product handling of 200 V \times μ s or greater. (All of the temperature rise in the core, and most of the temperature rise in the windings can be derived from the ac flux in the core—the volt-time product. It is worthwhile to specify a much larger value to keep the ac heating to a minimum)

3 Noise

Noise as it pertains to switching circuitry resides in the fast rising edges of the voltage and current waveforms at various switching cycles. With the bridge switches constantly switching and the output inductors charging and discharging, we have both electric and magnetic fields to mitigate as part of our design task. From a near field standpoint, transmitting magnetic noise in a magnetic field requires a current loop while transmitting noise in an electric field requires surface area.

To minimize the noise transmitters in a given circuit, keep the loop areas of the power train as small as possible. Ideally, this means that the current into a component flows as close to the current out of the component as possible. This scenario not only minimizes loop area, but the magnetic fields associated with the opposing currents are cancelled to a large degree. Bruce Carsten has developed an excellent seminar series on this topic that can be viewed in most any of the APEC literature from 1997 on. We also need to keep the nodes from capacitively radiating energy through large copper areas tied to high dv/dt switching nodes. There has to be some compromise on copper area since we need a given trace width for a given RMS current through the trace.

The noise receivers are necessary evils. In this example, the noise receivers are the signal components around the amplifier: the inputs, the oscillator connections, the shutdown pins, headphone outputs (if on IC), and so forth. All we can do in this case is try to minimize the loop area and keep the copper traces short and narrow.

Oddly, the output and input cables can be either noise transmitters or noise receivers. In most applications of the TPA300X series, the output cable needs to be addressed as a noise transmitter.

The higher level EMI textbooks, such as *Controlling Radiated Emissions by Design* by Michel Mardiguian, and *Noise Reduction Techniques in Electronic Systems* by Henry Ott get into modeling and noise sources. For the purposes of this discussion, I truncate most of the modeling techniques and assume that any noise above 1 MHz is common to the cables and traces (a common mode source), and that any noise source below 1 MHz is a differential source. This is a gross truncation that only works due to the simplicity, small area, and low parts count of this circuit.

3.1 Grounding

At this stage it is paramount that we acknowledge the need for separate grounds. Noise currents in the output power stage need to be returned to output noise ground and nowhere else. Were these currents to circulate elsewhere, they may get into the power supply, the signal ground, and so forth; worse yet, they may form a loop and radiate noise. Any of these instances results in degraded amplifier performance. The logical returns for the output noise currents associated with class D switching are the respective P_{gnd} pins for each channel. The switch state diagram illustrates that P_{gnd} is instrumental in nearly every switch state. This is the perfect point to which the output noise ground trace should return. Also note that output noise ground is channel specific. A two channel amplifier has two mutually exclusive channels and consequently must have two mutually exclusive output noise ground traces. The layout of the IC offers separate P_{gnd} connections for each channel and in some cases each side of the bridge. Output noise ground(s) must tie to system ground at the PowerPAD™ exclusively. Signal currents for the inputs, oscillator, and so forth, need to be returned to quiet ground. This ground only ties to the signal components and the A_{gnd} pin(s). A_{gnd} then ties to the PowerPAD. System ground is the connection between the power pad and the main decoupling capacitors. These ground connections should all tie together in a Kelvin or star fashion at the PowerPAD connection. Ground planes are strongly discouraged due to the noise currents in the ground plane having the ability to circulate wherever they choose. The main decoupling capacitor may be fed from a ground plane, but system ground, output noise ground, and quiet ground must not tie to the ground plane. The PowerPAD requires as much copper connection as possible for heat dissipation. This copper flood is usually connected to system ground.

4 Component Placement

Now that we have mapped the current paths, we have a good idea of how current circulates in the power train. The placement task is greatly simplified. The first elements to be placed are the power train elements. When placing these elements, it is important to remain focused on the whole amplifier circuit. Clearly the V_{CC} decoupling capacitors need to be close to the P_{vcc} and P_{gnd} pins. The output filters need to be close to the O_{UTP} and O_{UTN} pins. The load needs to be close to the output filters. However, the signal level pins of the IC also need real estate consideration. The inputs need to be routed away from the power train, yet they need to remain close to the IC to maintain a small loop area to maximize the noise immunity of the amplifier. So just when we think we've got it figured out, there is a compromise.

4.1 Design Example

4.1.1 Design Example Constraints

Below, I have included an example of the schematic, placement, and layout of a basic amplifier application. The IC featured is the TPA3004D2. I have explained the major decisions throughout the process. The constraints for this placement were:

- 4 layer board, 1-oz. copper (1.4 mil thick) on each layer. Inside layers are reserved for +Vcc and ground flood, nothing else
- Inputs and outputs combined on a two row Molex Cgrid connector. Pin placement and pin count is negotiable.
- Component placement allowed only on top of the PCB
- Amplifier inputs are single ended
- Amplifier circuitry must occupy minimal real estate
- 4-Ω speakers

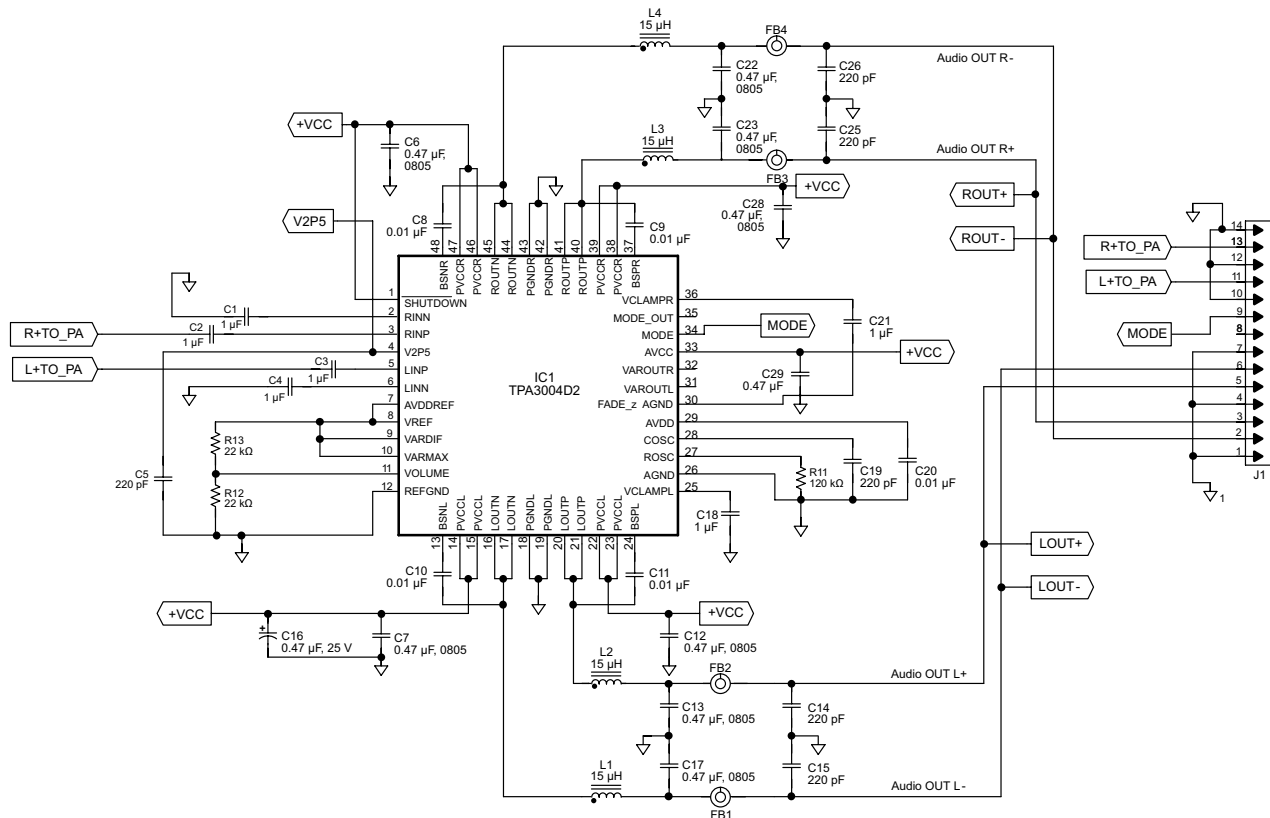


Figure 13. Schematic

4.1.2 Placement

In the component placement of the TPA3004D2 circuit, we first place the header. This header accommodates the outputs and the inputs. Precautions must be taken to avoid crosstalk between the output and the input sections. I have segmented the header such that the outputs are on one extreme end and the inputs are on the other extreme end. If we could place Rout+ next to Rout- , we could maximize the cancellation of the noise fields around Rout+ and Rout- by minimizing the loop area between Rout+ and Rout- . The same holds true for Lout+ and Lout- . Additionally, if we could place ground connections between the right and left connections, this would further reduce the chance of right or left channel noise coupling into the inputs.

So we have some tentative notions on how the output structure should be positioned. The outputs should be next to each other, each output should be guarded, the inputs should be on the other end of the header, and the output loop areas should be as small as possible.

On the schematic, if we spend a little time envisioning the output traces, we quickly realize a few things, namely: if the output traces and output ground are to be routed for a short trace length, and minimal loop area, one side of the IC is *trapped* in the output area. This is either pins 25 thru 36, or pins 1 thru 12. Pins 1 thru 12 are the signal inputs, and as such they are far more noise sensitive than pins 25 thru 36. I have chosen to *trap* pins 25 thru 36 in the output area and leave the inputs as far from the output current paths as possible.

The pinout of the output side of the header was an iterative process. It took a couple of iterations to get the pins to flow without traces having to jump over one another. The header was finally pinned out as:

Table 1. Header Pinout - Output Side

Pin Number	Node
1	Output ground
2	Right out+
3	Right out-
4	Output ground
5	Left out+
6	Left out-
7	Output ground
8	NC
9	Mode
10	Quiet ground
11	Left + input
12	Quiet ground
13	Right + input
14	Quiet ground

Once the schematic looks reasonable, we move on to the placement task. It is worthwhile to note that the output inductor is a coupling cap for all purposes beyond its self-resonant frequency. The ferrite beads (FB1 thru FB4) should be located as near to the output leads as possible in this example. They are used as secondary filters to filter out noise above the self resonant frequency of the output inductor. The shunt capacitors (C22, C23, C26, C25, C13, C14, C15, and C17) provide a path for noise energy to output noise ground. This helps with noise reduction both at the output inductors and at the ferrite beads. The shunt capacitors (C14, C15, C25, C26) need to be close to both the ferrite beads and the output pins of the '3004D2 IC. The shunt capacitors (C13, C17, C22, and C23) need to be between the output inductor and the ferrite beads. All shunt capacitors need to be tied to the output noise ground with the shortest, lowest impedance traces possible.

Wrapping up the placement of the output structure, we still have the bootstrap capacitors (C8, C9, C10, and C11) and the PVcc capacitors (C6, C7, C12, and C28). These capacitors need to be placed as close to the IC as possible. Noise currents flow through the bootstrap capacitors as the high side switches in the output bridge are switched on and off. Similarly noise currents flow through the PVcc capacitors as the bridge transitions through its switching states. In the positioning sketch, I compromised a little trace length in the bootstrap capacitors to allow the best possible placement of the PVcc capacitors. From the switching diagrams above, these capacitors are a vital part of the power train and need to have as little loop area as possible. The bootstrap capacitors are also a vital path, but the power currents through the switches have to flow from the PVcc capacitors. The bootstrap capacitors were given second priority in the placement.

C16 is the main decoupling capacitor for the whole circuit. The PVcc feeders and the Avcc feeder should connect to C16 through a Kelvin or 'star' connection. This eliminates any noise currents on PVcc from getting into the signal components tied to AVcc. The ground connection from C16 is the system ground. This should tie from C16 to the PowerPAD. The pad of C16 may tie to the system ground plane as this is the purest point to reference.

The *trapped components* that tie to the *trapped pins* are C18, C19, C20, C21, C29, and R11. These components form the relaxation oscillator that determines the switching frequency of the amplifier, the clamp circuits for the right and left channel, and the decoupling for the 5-V output line. The relaxation oscillator components (C19, R11) and the Avcc decoupling capacitor (C29) get first priority in placement. These parts need to be located as close to their respective pins as possible. The ground connection for all *trapped components* is to be a quiet ground whose only tie to system ground is at the power pad of the IC. All other *trapped components* are then placed as close to their respective pins as possible.

The only components left are the input components (C1 thru C5, R12, and R13). These components are placed as near to their respective pins as possible. All grounds pertaining to the input are to be on a quiet ground whose only tie to system ground is at the power pad.

The PCB layout illustrated in [Figure 14](#) shows how these steps were followed through the placement task. For scaling purposes, the header is on a 0.100" grid. The asymptotic box around the entire positioning is about 2.0" x 2.2".

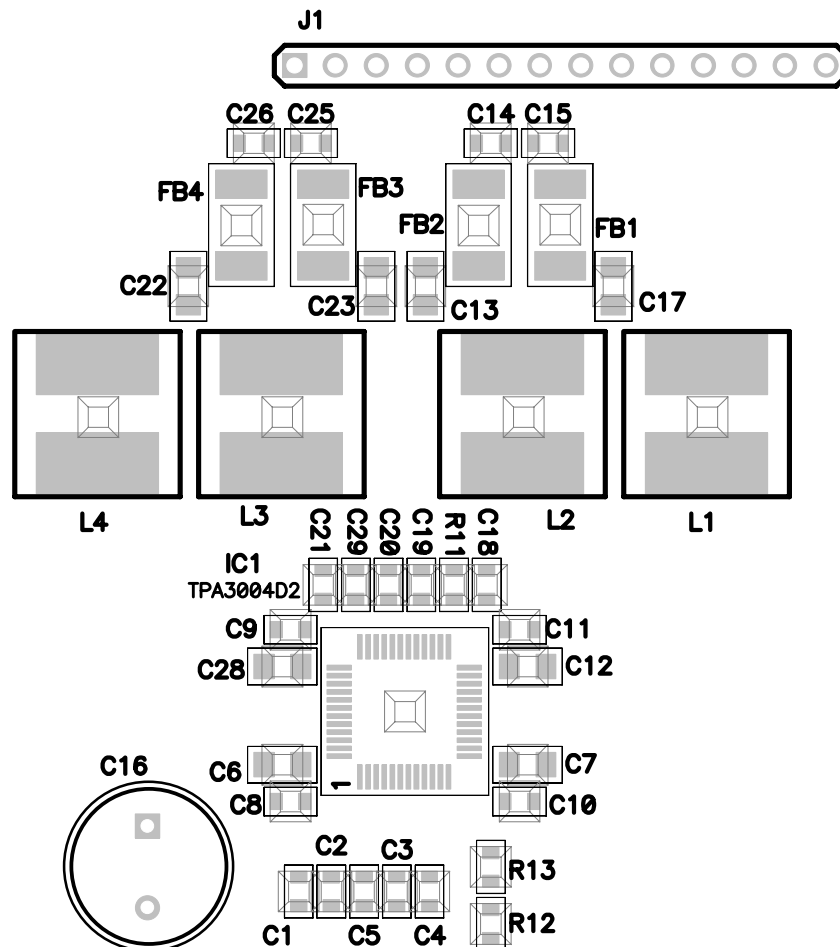


Figure 14. PCB Layout

4.2 PCB Layout

4.2.1 Trace, Via, and Wire Consideration

Similar to the component placement, the first portion of the circuit to be routed is the output portion. It is easiest to start at one end and work through the other. I chose to start at the output header and work back through the IC. For maximal field cancellation through all switching states, the best layout we can have is Out+ next to Out-, with output noise ground flowing under these traces back to the IC. From the specifications called out above, the board will have 1-oz copper on all layers. The load impedance is 4 Ω .

If the IC can deliver 10-W RMS into a 4- Ω load, there is approximately 1.6 A_{RMS} flowing through each output trace at the fundamental frequency. Additionally, in the traces between the TPA300x and the output inductors, the RMS current is somewhat larger. This is due to the ripple current flowing into the output inductor of ΔI (p-p) where $\Delta I = (V_{in} - V_{out}) \times \Delta t/L$. The RMS contribution of this ripple current is approximately $\Delta I/\sqrt{12}$. While we should not forget about this ripple current, it is negligible.

Per [Appendix A](#), a good safe current density in the output trace is 100 CM/A (circular mils per amp) or greater. If we look down the 100 CM/A column, our 1.6 A_{RMS} current falls right on the values corresponding to #28 AWG wire. In 1 oz copper, we can use about 90 mil trace width (2.3 mm). This is only a guideline. It is always safer to use wider traces. The PVcc lines should be much thicker to minimize voltage ripple. No current density on the PC board should ever fall below 30 CM/A for any trace length. The current density in the output cable from the header should be much higher to avoid losses. A good current density for the wire harness is 300CM/A. From the table this corresponds to a #23 AWG wire. For design purposes, #22 AWG wire is much more readily available.

4.2.2 Routing

The routing task should start at the output pins. The output filters, inductors, capacitors and so forth, should be routed first. This may need to be an iterative process to get the noise currents returned to output noise ground through as short and wide of a trace as possible. Note that this same trace is used to shield the output traces, inductors, and so forth.

The next traces to be considered are the Pvcc traces. Recall from the switch diagrams that Pvcc is the critical node in the power train. In this example there are 4 different connections to Pvcc (C6, C7, C12, and C28). We need a very low impedance trace to all 4 of these connection points. This trace should be considered noisy in that it carries ripple current to the power train. Consequently it should be routed as far away from the amplifier inputs as possible. It should also have a ground trace flowing under it.

The next task is to route the trapped pins. These pins have a separate connection to system ground. While it is difficult to minimize loop area, we can keep the components as close to the IC as possible, and flood the underside of these components with quiet ground.

The last task is to route the inputs. These pins are the most susceptible to noise. They should be surrounded by as much quiet ground copper as possible. In this case, I routed guard traces around and between the inputs, and quiet ground under the inputs. This should keep any incident noise out of the inputs.

[Appendix B](#) contains printouts of each layer of the PCB. These printouts can be photocopied to transparencies for viewing purposes.

5 EMC-The Final Word: Did Those Tricks Really Work?

5.1 The Arsenal

Before undertaking the mitigation task, we need to put together an arsenal. Most of the time the EMI test chamber is located somewhere else and very seldom do they have all the comforts of your home lab. I strongly suggest bringing along a few items to assist in mitigation and modeling. These items include:

- Bruce Carsten's EMI probe—Plans for this probe are available at www.bcarsten.com and included in Appendix C of this article. It allows an ordinary analog oscilloscope to be used to pinpoint the source of radiated energy.
- Copper Tape—It is nice because it can quickly be used to create a stick on ground plane. Note that terminations to the copper tape need to be soldered and the adhesive should not be assumed to be either a good insulator or a good conductor. 3M® is a good source for this material.
- Ferrites—I would suggest bringing along a kit consisting of various high current beads, toroids, surface mount common mode filters, clam shells, and so forth, in various ferrite materials. The clamshells are often too expensive for mass production; however, they are a very fast way to determine a common mode radiator. If you suspect that a cable is radiating, place a clam shell around it. If the levels drop, your suspicion was correct. You should then begin looking for the source that is coupling the energy into the cable.
- Spare parts—as the models grow in complexity, you may wish to try different inductors from different

manufacturers, all having the proper ratings for your circuitry. Perhaps manufacturer A has a better shielded part than Manufacturer B.

- Spare boards—you might get into a lengthy modeling/modification that is irreversible. A few virgin spares are always a good idea.
- Solder wick—for desoldering and ground strap, trace-thickening agent, and so forth. Solder wick is a great low impedance conductor and it remains flexible until it is consumed or in the case of a wiring mod, tinned.
- X-Acto® knife and spare blades—just in case you need to alter a current path on the board
- Dremel® tool and a good selection of bits—just in case you REALLY need to alter a current path.
- Soldering Irons—bring a couple. A small one for surface-mount work, a large one for grounding large copper masses, and so forth.
- Solder—it is the glue that holds our world together.
- Various electronic tools—Cutters, screwdrivers, picks, pliers, and so forth

5.2 Mitigation Task

The layout included in this article is very similar to the final layout of an internal project that we recently did. The goal of this project was to pass the EMI limits put forth by CISPR22. Initially the layout had a ground plane where all connections to ground returned. There was no segmentation, or attempts to isolate output noise ground, quiet ground and system ground. The outputs were lengthy, employed little or no field cancellation and had no ground running underneath them. I have included an initial plot of the radiated noise from this layout:

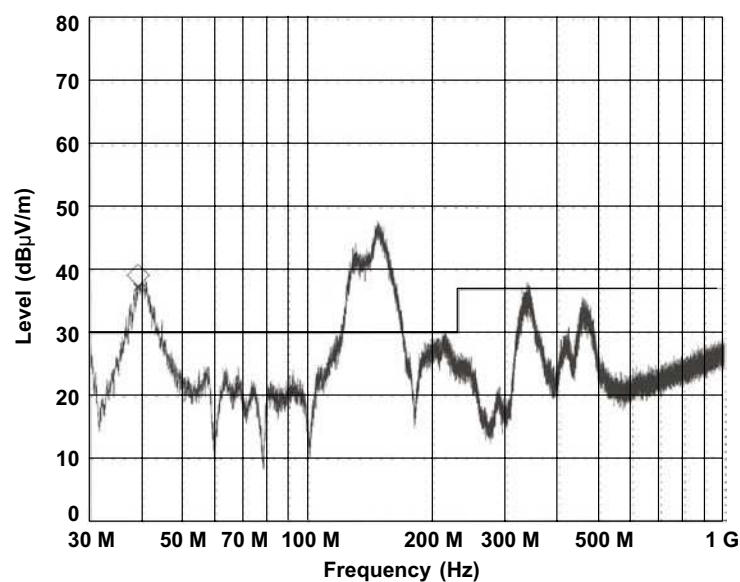


Figure 15. Initial Layout Noise

The first change I made to this layout was to segment the ground plane layer such that all output noise currents returned to P_{gnd} and then tied to the power pad. The results of this segmentation are shown in [Figure 16](#).

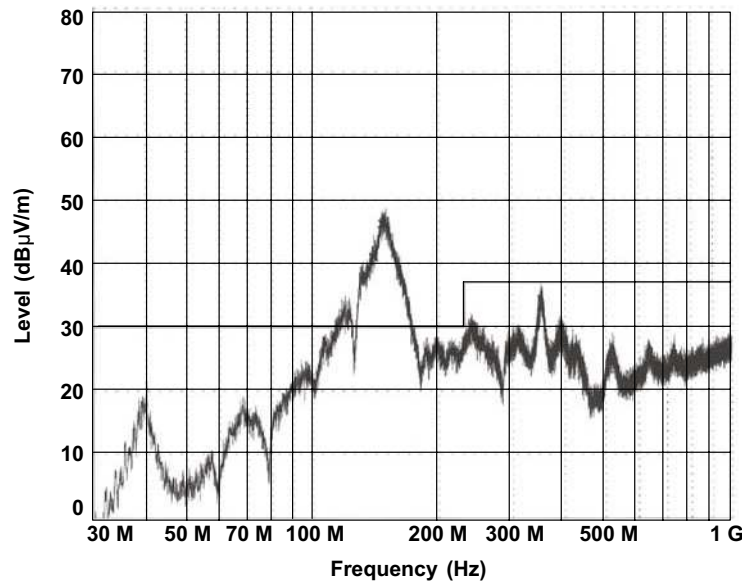


Figure 16. Noise-First Segmentation Change

From this point, I decided to investigate the broadband noise source around 150 MHz. I did this with the use of Bruce Carsten’s EMI probe. (Plans for this probe are available at www.bcarsten.com and included in Appendix C). I regularly use this probe in mitigating EMI noise. It is easy to build, works best with an oscilloscope, and gets within 1/32” of the offender. I strongly recommend this probe for finding noise sources on PCB’s. The probe showed that the thin trace connecting the PvcC decoupling capacitors was radiating fiercely. I added a few MLCCs, staggered along the length of the trace, to get the plot shown in Figure 17.

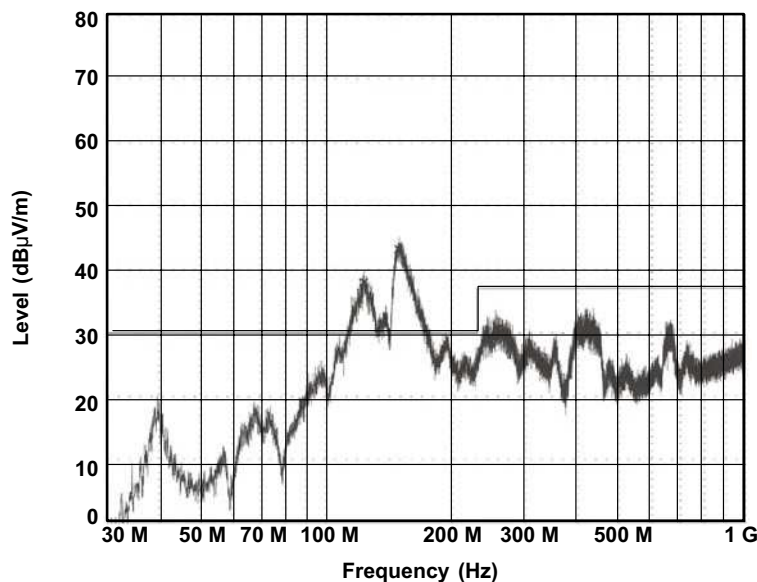


Figure 17. Noise-With Staggered MLCCs Along the Trace Length

Note the change in signature. While the MLCC’s did not resolve the problem, they did alter the signature significantly. This is a strong hint that we are on the right track in assuming that the PvcC trace is the offender. I did not have the ability to reroute the offending trace properly; however, we did add a common mode choke to the outputs on the theory that the noisy PvcC trace was combining with noise coming through the output filters. The results of this are shown in Figure 18.

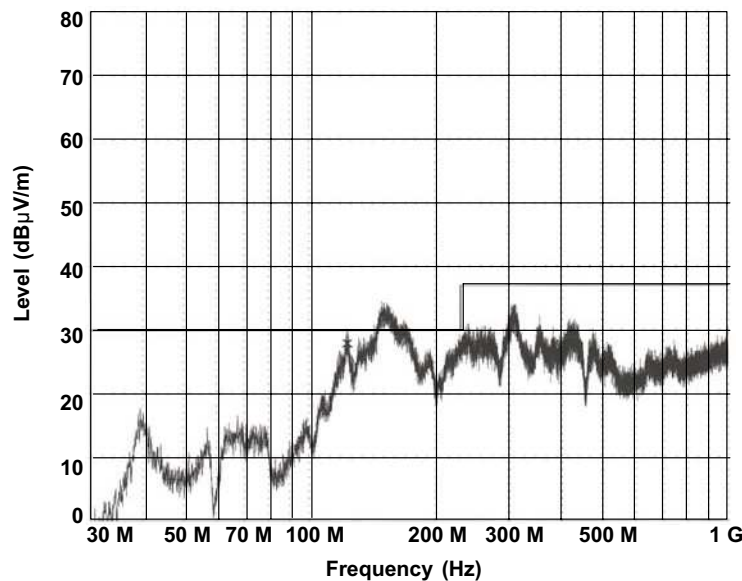


Figure 18. Noise Signature-After Adding a Common Mode Choke

Later, when the offending P_{vcc} trace was thickened and rerouted, we passed the CISPR 22 requirements with 5 dB of margin in the 150 MHz area and much more margin everywhere else.

Clearly there is some method to the madness. Four of the five nuisance peaks were brought down to passable levels by simply segmenting the ground layer. With some analysis and first order modeling, we were able to bring the remaining noise peak down to nearly passing. Finally, by rerouting the P_{vcc} trace and minimizing its loop area, the problem was resolved.

While the techniques in this article were applied to the TPA300x series of parts, they are useful in any switchmode amplifier or power converter. Power train analysis is often lengthy, but vital to the designer's understanding of how the circuit works and should be performed on any power converter before the design stage is started. From this point the designer can begin the design process. The data sheet supports the paper design process and the calculation of values. This collateral should serve to support the PC board level design and the debugging of the design as it pertains to EMI. If care is taken in the layout task, and these guidelines are understood and adhered to, the EMI stage of the design should require minimal change. I strongly recommend allowing enough time in the product schedule to allow for one full EMI screening and a quick respin to implement any fixes. As the output power level increases, these techniques become increasingly important. I have written this based on my own past design experiences and with customers. All of these techniques are tried and true. The extent to which they are practiced and enforced determines their success.

6 References

- Carsten, Bruce. Professional Advancement courses and seminars at APEC, and so forth. Appears in Apec literature from 1995 on.
- Mardiguian, Michel. Controlling Radiated Emissions By Design, Second Edition. Boston: Kluwer Academic Publishers, 2001.
- Ott, Henry. Noise Reduction Techniques in Electronic Systems. New York: Wiley, 1988.
- Texas Instruments, [TPA3004D2 12-W STEREO CLASS-D AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL](#)

Copper Wire Current Density

A.1 Current-Density Table

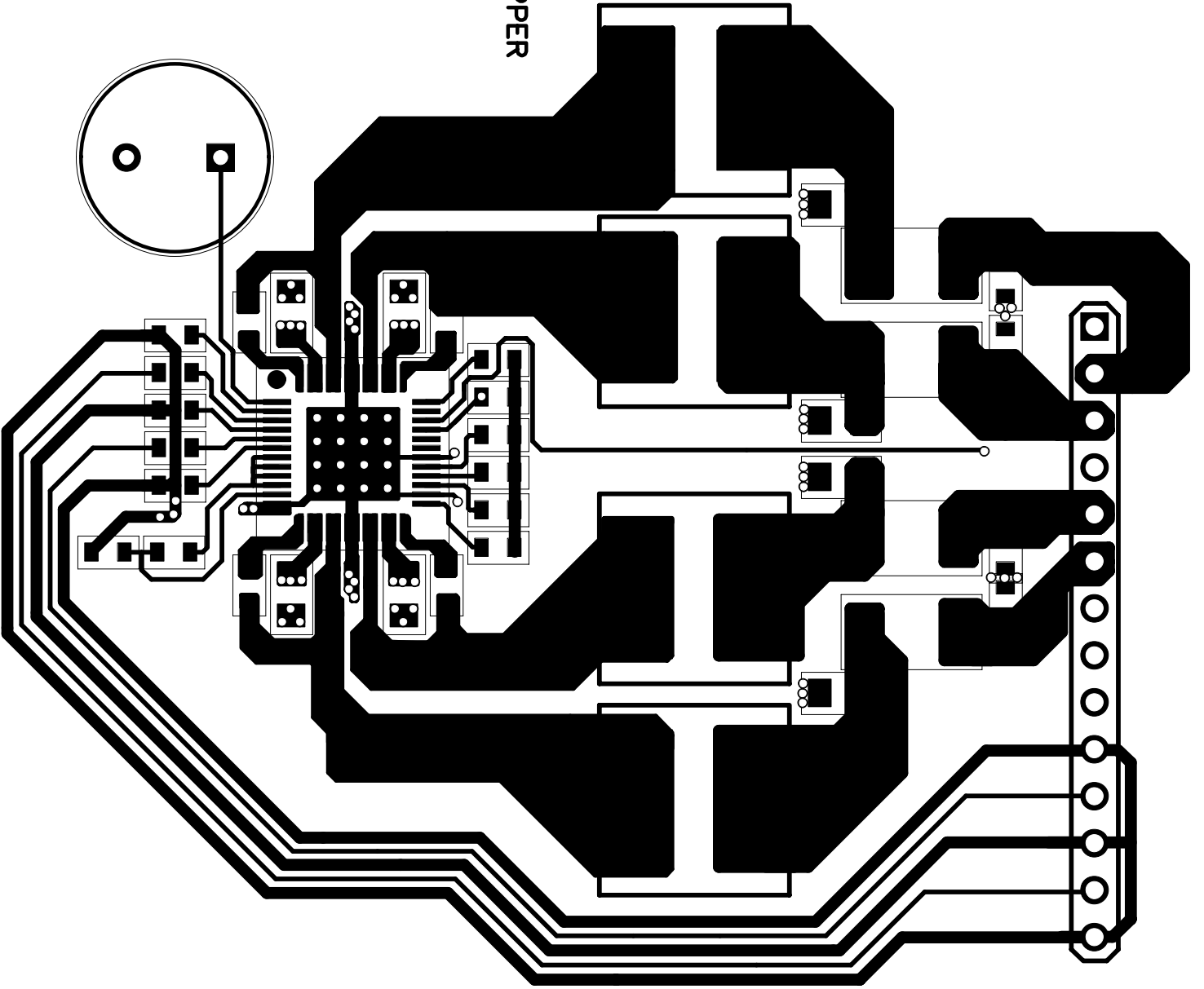
See the following page for the current density table.

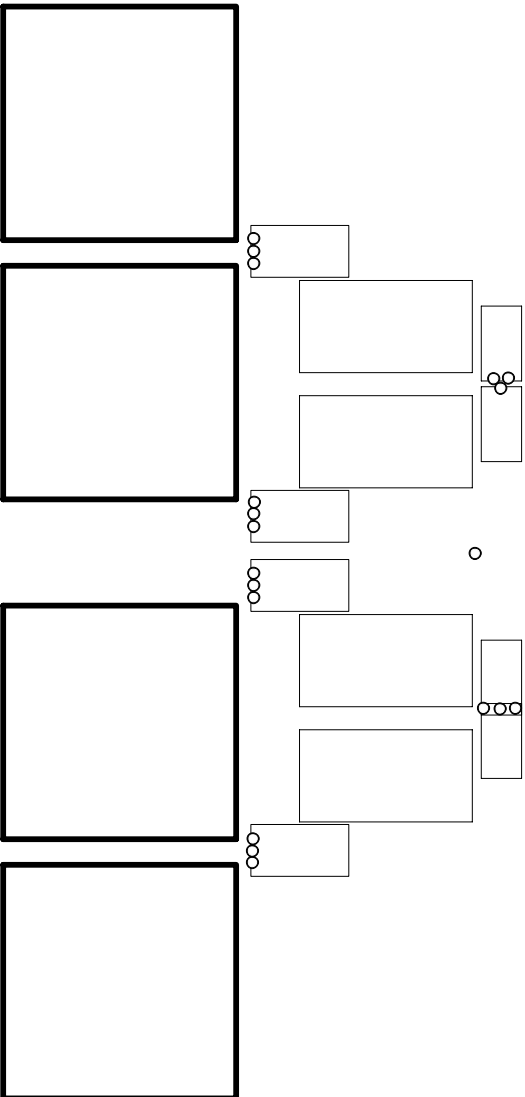
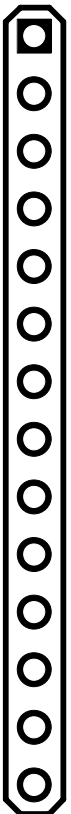
PCB Layers

B.1 Board Layers

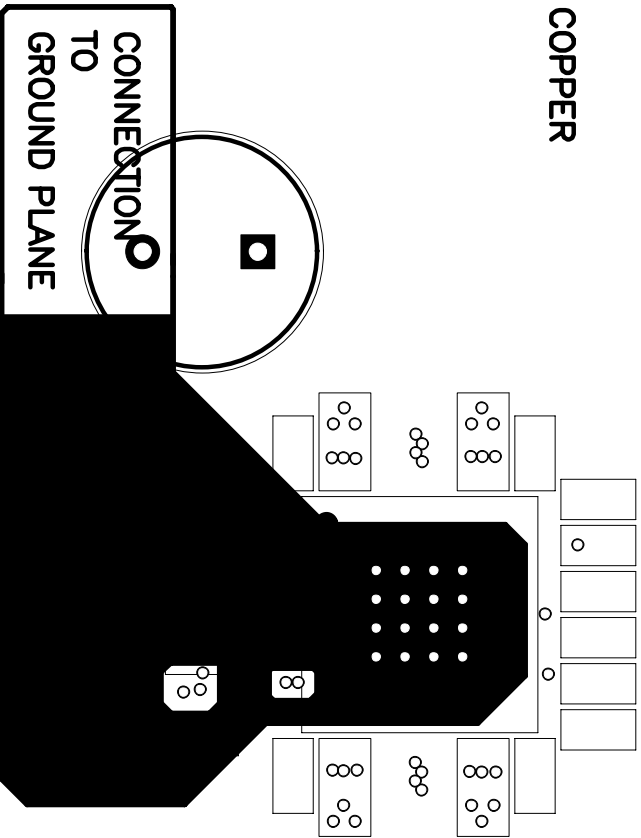
See the following pages for the PCB layers.

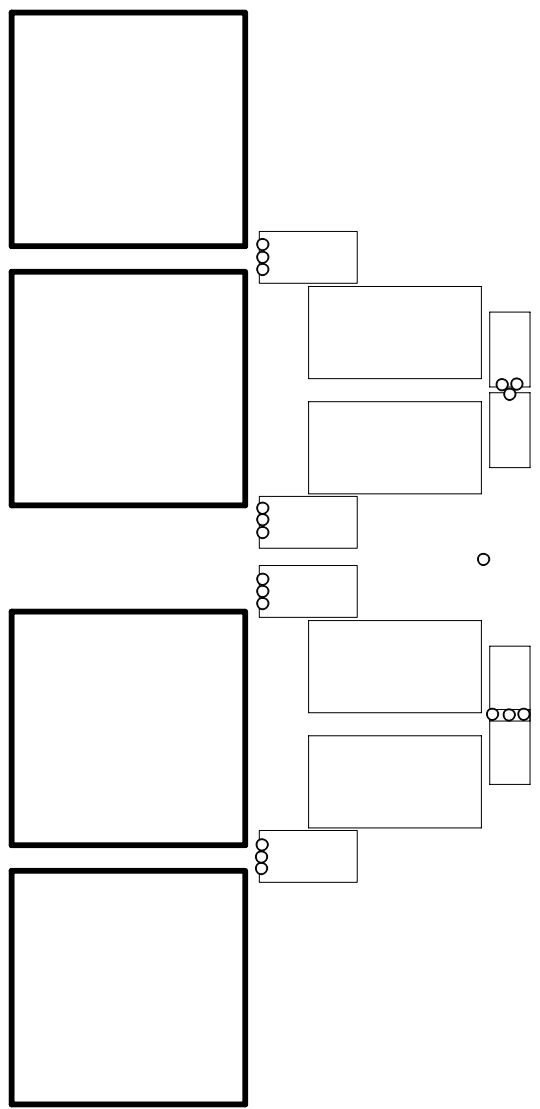
TOP COPPER



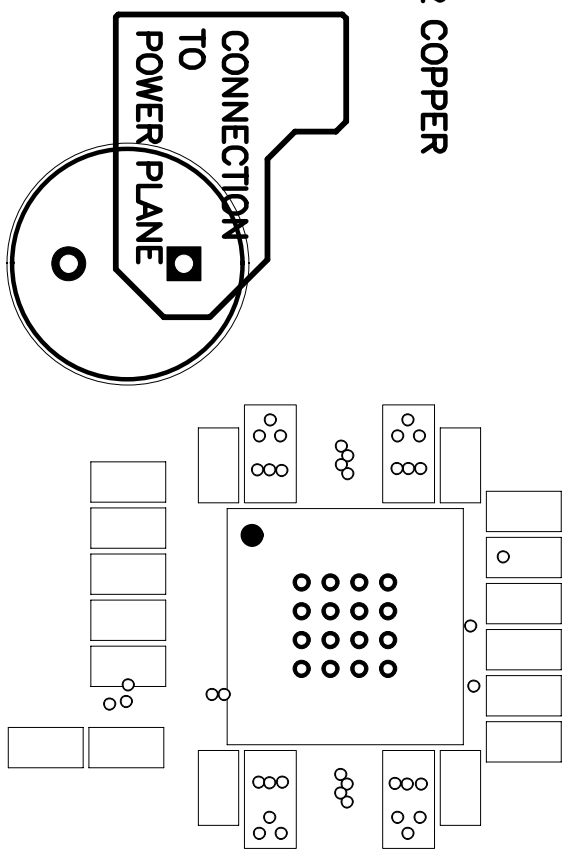


MID1 COPPER

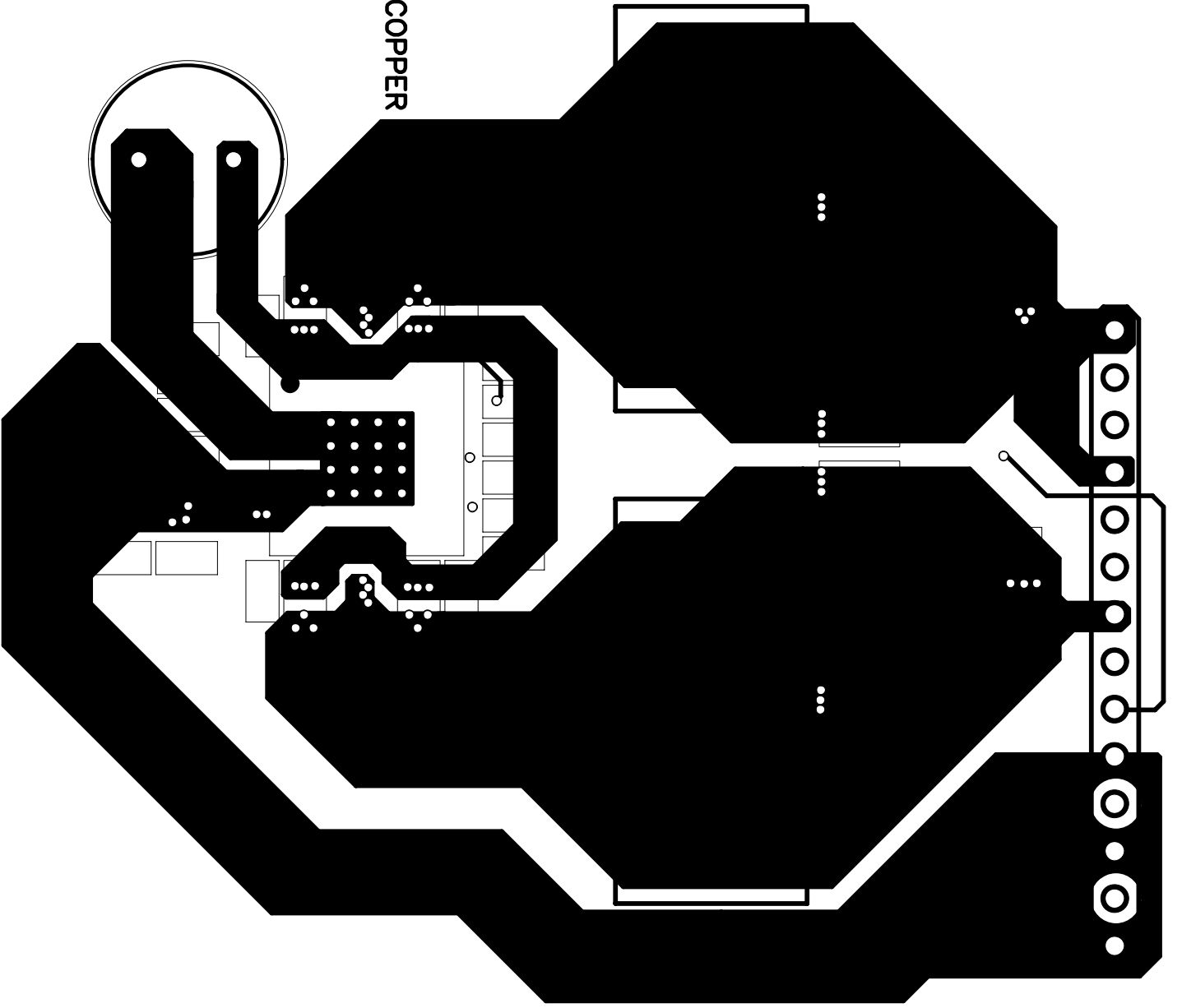


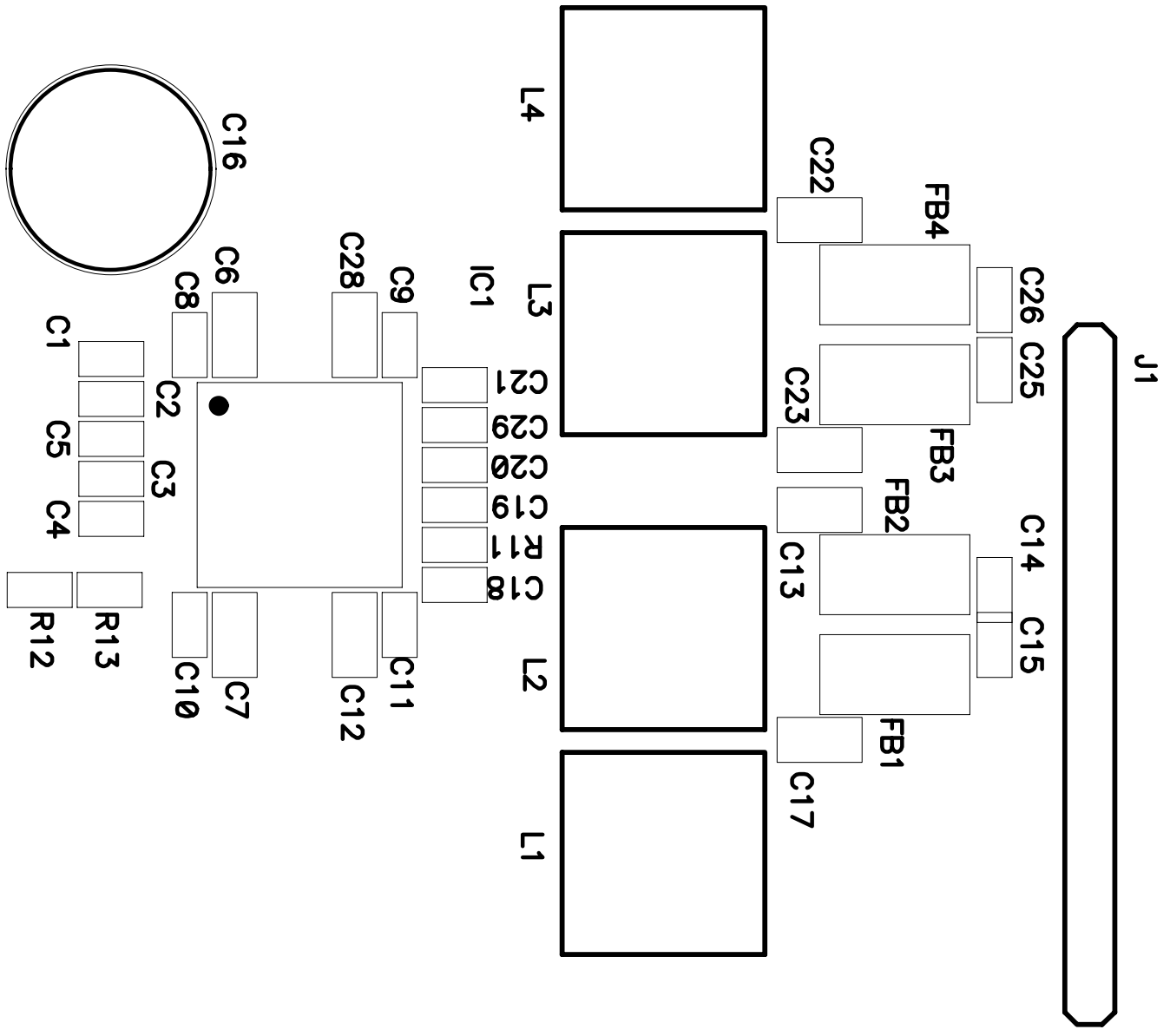


MID2 COPPER



BOTTOM COPPER





Bruce Carsten Associates, Inc.

C.1 Appnote

See the following pages for Bruce Carsten Associates, Inc. Appnote.



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Products and Services for the Power Electronics Design Engineer

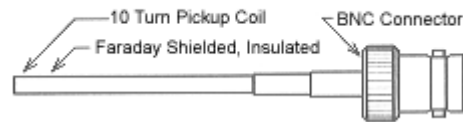
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APPNOTE

EMI SNIFFER™ PROBE - APPLICATION NOTE

MINIATURE EMI 'SNIFFER PROBE'



The EMI Sniffer™ Probe is used with an oscilloscope to locate and identify magnetic field sources of electromagnetic interference (EMI) in electronic equipment. The probe consists of a miniature 10 turn pickup coil located in the end of a small shield tube, with a BNC connector provided for connection to a coaxial cable.

The EMI Sniffer™ Probe output voltage is essentially proportional to the rate of change of the ambient magnetic field, and thus to the rate of change of nearby currents.

The principal advantages of the EMI Sniffer™ Probe over simple pickup loops are:

1. Spatial resolution of about a millimeter;
2. Relatively high sensitivity for a small coil;
3. A 50 ohm source termination to minimize cable reflections with unterminated scope inputs;
4. Faraday shielding to minimize sensitivity to electric fields.

The EMI Sniffer™ Probe was developed to diagnose sources of EMI in switchmode power converters, but it can also be used in high speed logic systems and other electronic equipment.

SOURCES OF EMI

Rapidly changing voltages and currents in electrical and electronic equipment can easily result in radiated and conducted noise. Most EMI in switchmode power converters is thus generated during switching transients, when power transistors are turned on or off.

Conventional scope probes can readily be used to see dynamic voltages, which are the principal sources of common mode conducted EMI. (High dV/dt can also feed through poorly designed filters as normal mode voltage spikes, and may radiate fields from a circuit without a conductive enclosure.)

Dynamic currents produce rapidly changing magnetic fields which radiate far more easily than electric fields, as they are more difficult to shield. These changing magnetic fields can also induce low impedance voltage transients in other circuits, resulting in unexpected normal and common mode conducted EMI.

These high dI/dt currents and resultant fields can not be directly sensed by voltage probes, but are readily detected and located with the EMI Sniffer™ Probe. While current probes can sense currents in discrete conductors and wires, they are of little use with printed circuit traces, or in detecting dynamic magnetic fields.

PROBE RESPONSE CHARACTERISTICS

The EMI Sniffer™ Probe is sensitive to magnetic fields only along the probe axis. This directionality is useful in locating the paths and sources of high dI/dt currents. The resolution is usually sufficient to locate which trace on a printed circuit board, or which lead on a component package, is conducting the EMI generating current.

For "isolated" single conductors or PC traces, the Probe response is greatest just to either

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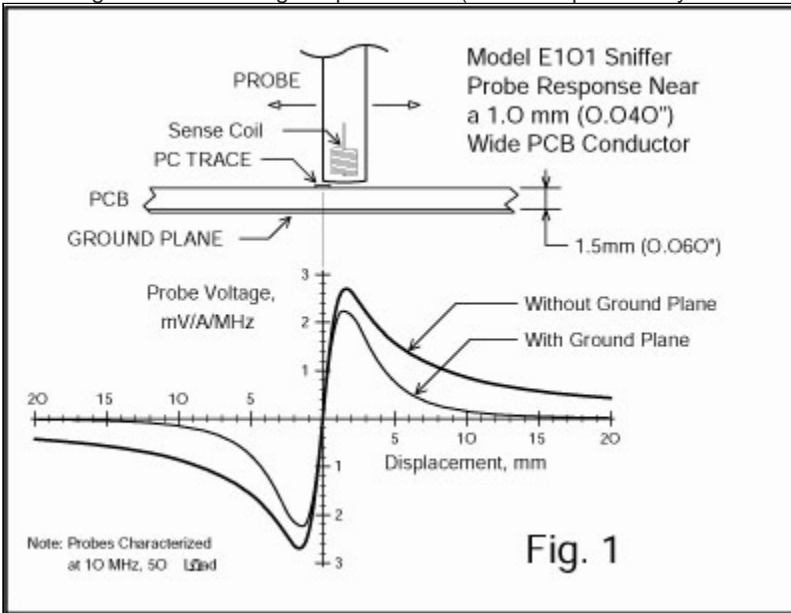
info@bcarsten.com

Tel: (541) 745-3935

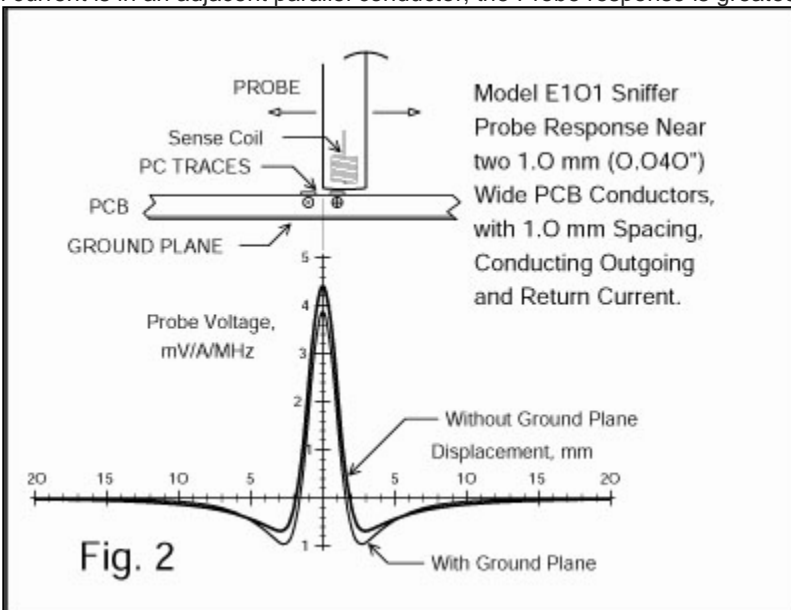
Fax: (541) 745-3923

6410 NW Sisters Pl.
 Corvallis, OR 97330

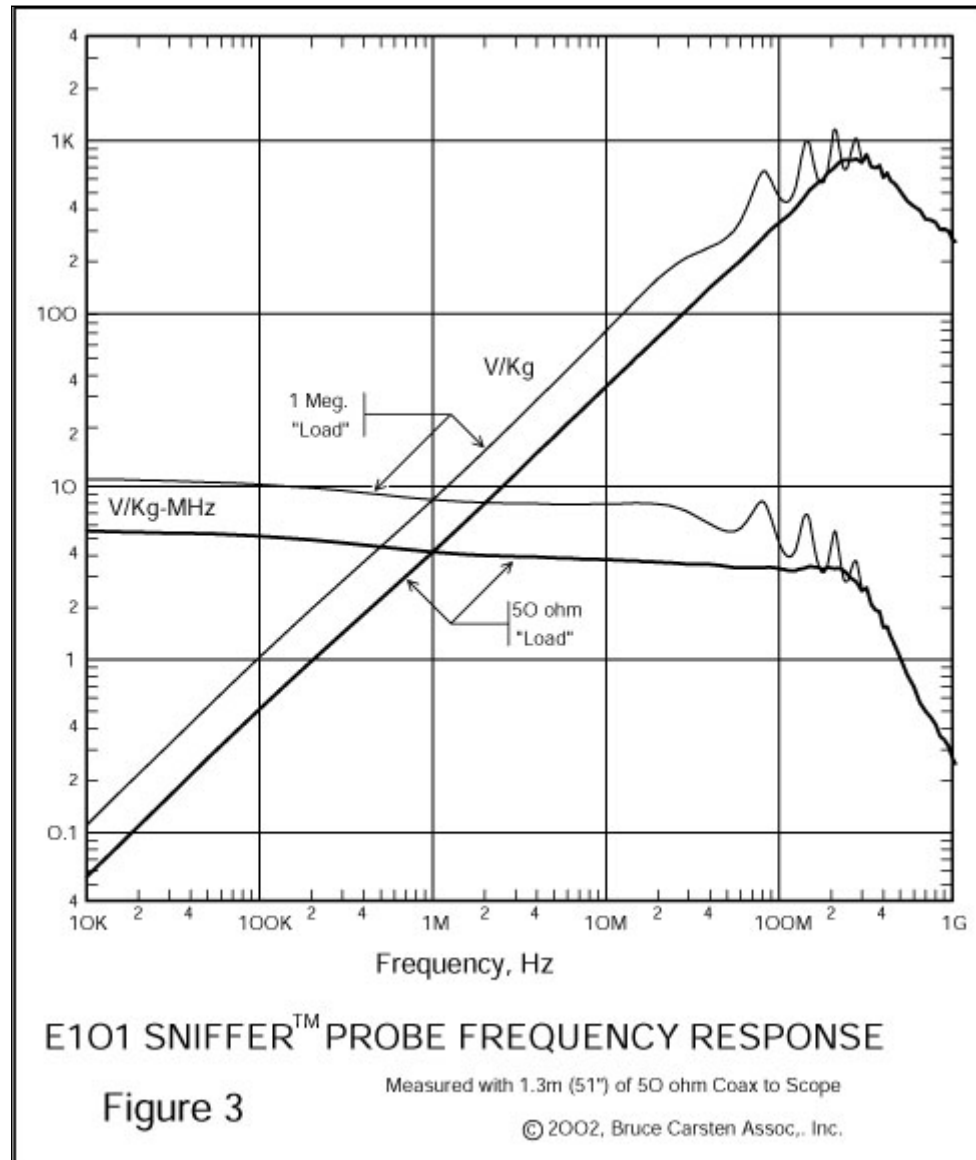
side of the conductor where the magnetic flux is along the probe axis. (Probe response may be a little greater with the axis tilted towards the center of the conductor.) As shown in Figure 1, there is a sharp response null in the middle of the conductor, with a 180 degree phase shift to either side and a decreasing response with distance. The response will increase on the inside of a bend where the flux lines are crowded together, and is reduced on the outside of a bend where the flux lines spread apart.



When the return current is in an adjacent parallel conductor, the Probe response is greatest between the two conductors as shown in Figure 2. There will be a sharp null and phase shift over each conductor, with a lower peak response outside the conductor pair, again decreasing with distance.



The response to a trace with a return current on the opposite side of the board is similar to that of a single isolated trace, except that the probe response may be greater with the Probe axis tilted away from the trace. A "ground plane" below a trace will have a similar effect, as there will be a counter-flowing "image" current in the ground plane.



The Probe frequency response to a uniform magnetic field is shown in Figure 3. Due to large variations in field strength around a conductor, the Probe should be considered as a qualitative indicator only, with no attempt made to "calibrate" it. The response rolloff near 300 MHz is due to the pickup coil inductance of 75nH driving the total terminated impedance of 100 ohms, and the mild resonant peaks (with a 1 M ohm scope termination) at multiples of 80 MHz are due to transmission line reflections.

PRINCIPLES OF PROBE USE

The EMI Sniffer™ Probe is used with at least a two channel scope. One channel is used to view the noise whose source is to be located (which may also provide the scope trigger), and the other channel is used for the EMI Sniffer™ Probe. The probe response nulls make it inadvisable to use this scope channel for triggering.

A third scope trigger channel can be very useful, particularly if it is difficult to trigger on the noise. Transistor drive waveforms (or their predecessors in the upstream logic) are ideal for triggering; they are usually stable, and allow immediate precursors of the noise to be viewed.

Start with the Probe at some distance from the circuit with the Probe channel at maximum sensitivity. Move the probe around the circuit, looking for "something happening" in the circuit's magnetic fields at the same time as the noise problem. A precise "time domain" correlation between EMI noise transients and internal circuit fields is fundamental to the

diagnostic approach.

As a candidate noise source is located, the Probe is moved closer while the scope sensitivity is decreased to keep the Probe waveform on-screen. It should be possible to quickly bring the probe down to the PC board trace (or wiring) where the Probe signal seems to be a maximum. This may not be near the point of EMI generation, but it should be near a PC trace or other conductor carrying the current from the EMI source. This can be verified by moving the Probe back and forth in several directions; when the appropriate PC trace is crossed at roughly right angles, the probe output will go through a sharp null over the trace, with an evident phase reversal in probe voltage on each side of the trace (as noted above).

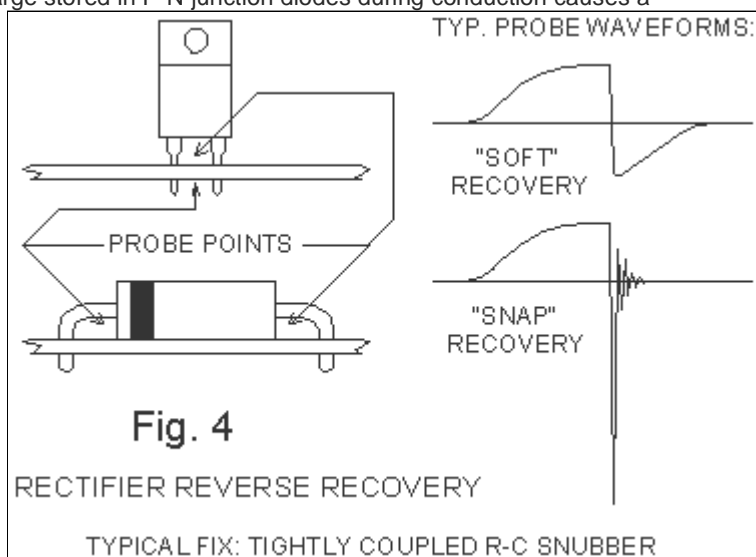
This EMI "hot" trace can be followed (like a bloodhound on the scent trail) to find all or much of the EMI generating current loop. If the trace is hidden on the back side (or inside) of the board, mark it's path with a felt pen and locate the trace on disassembly, on another board, or on the artwork. From the current path and the timing of the noise transient, the source of the problem usually becomes almost self-evident.

Some of the more common EMI problems are discussed in this short form ap-note to illustrate typical probe uses.

TYPICAL di/dt EMI PROBLEMS

Rectifier Reverse Recovery

Reverse recovery of rectifiers is the most common source of di/dt related EMI in power converters; the charge stored in P-N junction diodes during conduction causes a momentary reverse current flow when the voltage reverses. This reverse current may stop very quickly (<1 ns) in diodes with a "snap" recovery (more likely in devices with a PIV rating of less than 200V), or the reverse current may decay more gradually with a "soft" recovery. Typical EMI Sniffer™ Probe waveforms for each type of recovery are shown in Fig. 4.



The sudden change in current creates a rapidly changing magnetic field, which will both radiate external fields and induce low impedance voltage spikes in other circuits. This reverse recovery may "shock" parasitic L-C circuits into ringing, which will result in oscillatory waveforms with varying degrees of damping when the diode recovers. A series R-C damper circuit in parallel with the diode is the usual solution.

Output rectifiers generally carry the highest currents, and are thus the most prone to this problem, but this is often recognized and they may be well snubbed. It is not uncommon for unsnubbed catch or clamp diodes to be more of an EMI problem. (The fact that a diode in an R-C-D snubber may need its own R-C snubber is not always self evident, for example).

The problem can usually be identified by placing the EMI Sniffer™ Probe near a rectifier lead. The signal will be strongest on the inside of a lead bend in an axial package, or between the anode and cathode leads in a TO-220, TO-247 or similar type of package, as shown in Fig. 4.

Using "softer" recovery diodes is a possible solution, and Schottky diodes are ideal in low voltage applications. However, it must be recognized that a P-N diode with soft recovery is also inherently lossy (while a "snap" recovery is not), as the diode simultaneously develops

a reverse voltage while still conducting current. The fastest possible diode (lowest recovered charge) with a moderately soft recovery is usually the best choice. Sometimes a faster, slightly "snappy" diode with a tightly coupled R-C snubber works as well or better than a soft but excessively slow recovery diode.

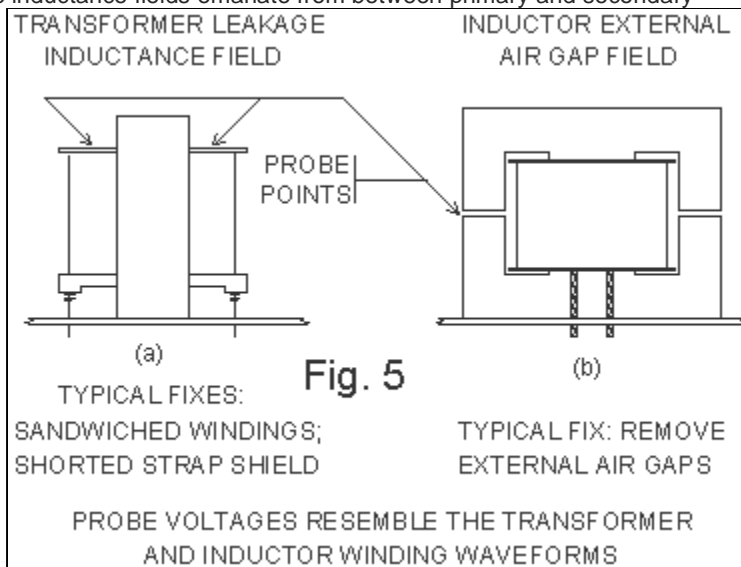
If significant ringing occurs, a "quick-and-dirty" R-C snubber design approach works fairly well: increasingly large damper capacitors are placed across the diode until the ringing frequency is halved. We know that the total ringing capacity is now quadrupled, or that the original ringing capacity is 1/3 of the added capacity. The damper resistance required is about equal to the capacitive reactance of the original ringing capacity at the original ringing frequency. The "frequency halving" capacity is then connected in series with the damping resistance and placed across the diode, as tightly coupled as possible.

Leakage Inductance Fields

Transformer leakage inductance fields emanate from between primary and secondary windings. With a single primary and secondary, a significant dipole field is created, which may be seen by placing the EMI Sniffer™ Probe near the winding ends as shown in Fig. 5a. If this field is generating EMI problems, there are two principal fixes available:

1. Split the Primary or Secondary in two, to "sandwich" the other winding, and/or:

2. Place a shorted copper strap "electromagnetic shield" around the complete core and winding assembly. Eddy currents in the shorted strap largely cancel the external magnetic far field.



The first approach creates a "quadrapole" instead of a dipole leakage field, which significantly reduces the distant field intensity. It also reduces the eddy current losses in any shorted strap electromagnetic shield used, which may or may not be an important consideration.

External Air Gap Fields

External air gaps in an inductor, such as those in open "bobbin core" inductors or with "E" cores spaced apart (Fig. 5b), can be a major source of external magnetic fields when significant ripple or AC currents are present. These fields can also be easily located with the EMI Sniffer™ probe; response will be a maximum near an air gap, or near the end of an open inductor winding.

"Open" inductor fields are not readily shielded, and if they present an EMI problem the inductor must usually be redesigned to reduce external fields. The external field around spaced E cores can be virtually eliminated by placing all of the air gap in the center leg. Fields due to a (possibly intentional) residual or minor outside air gap can be minimized with the shorted strap electromagnetic shield of Fig. 11, if eddy current losses prove not to be too high.

A less obvious problem may occur when inductors with "open" cores are used as second stage filter chokes. The minimal ripple current may not create a significant field, but such an inductor can "pick up" external magnetic fields and convert them to noise voltages, or be an EMI susceptibility problem.

Poorly Bypassed High Speed Logic

Ideally, all high speed logic should have a tightly coupled bypass capacitor for each IC, and/or have power and ground distribution planes in a multi-layer PCB.

At the other extreme, I have seen one bypass capacitor used at the power entrance to a logic board, with power and ground led to the ICs from opposite sides of the board. This created large spikes on the logic supply voltage, and produced significant electromagnetic fields around the board.

With an EMI Sniffer™ Probe I was able to show which pins of which ICs had the larger current transients in synchronism with the supply voltage transients. (The logic design engineers were accusing the power supply vendor of creating the noise. I found that the supplies were fairly quiet; it was the poorly designed logic power distribution system that was the problem.)

SPURIOUS CAPACITIVE RESPONSE

The electrostatic Faraday shielding of the EMI Sniffer™ Probe is excellent, despite the open end of the Probe. (This end of the pickup coil is grounded to enhance shielding.) The spurious capacitive pickup is only about 4 fF (0.004 pF), based on the measured capacitive feedthrough. The effect is so slight that it can be ignored in virtually all applications; it is actually very difficult to measure, requiring a special test jig to minimize pickup of associated capacitive "displacement" currents in the vicinity, while maximizing the "true" capacitive coupling.

Due to the 75 nH inductive "loading" of the pickup coil the capacitive response is not proportional to the derivative of the voltage (dV/dt) but to the second derivative of the voltage up to about 200 MHz.

NOTES ON SIGNAL INJECTION

Some EMI sensing probes have also been used to test for EMI susceptibility by injecting a current into the probe and placing it near potentially sensitive circuits. This miniature probe is not particularly suitable for this application, due to its small coil and limitation to low drive levels; more than 1/8W input can cause damage.

EMI Diagnostic Test Equipment, Design Seminars, Consulting, and Technology Development Services

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Last updated Saturday, November 9, 2002. Website design and development by Josie Nutter.

Project management and additional development by Loren DeLaOsa.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2003) to A Revision	Page
• Updated document to latest format.	1

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