

Phase-Shifted Full-Bridge, Zero-Voltage Transition Design Considerations

Application Report



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PHASE SHIFTED FULL BRIDGE, ZERO VOLTAGE TRANSITION DESIGN CONSIDERATIONS

ABSTRACT

This Application Note will highlight the design considerations incurred in a high frequency power supply using the Phase Shifted Resonant PWM control technique. An overview of this switching technique including comparisons to existing fixed frequency non-resonant and variable frequency Zero Voltage Switching is included. Numerous design equations and associated voltage, current and timing waveforms supporting this technique will be highlighted. A general purpose Phase Shifted converter design guide and procedure will be introduced to assist in weighing the various design tradeoffs. Considerations will be given to the details of the magnetic and power switching areas. A summary of comparative advantages, differences and tradeoffs to other conversion alternatives is included.

UCC28950 CONTROL CIRCUIT SCHEMATIC

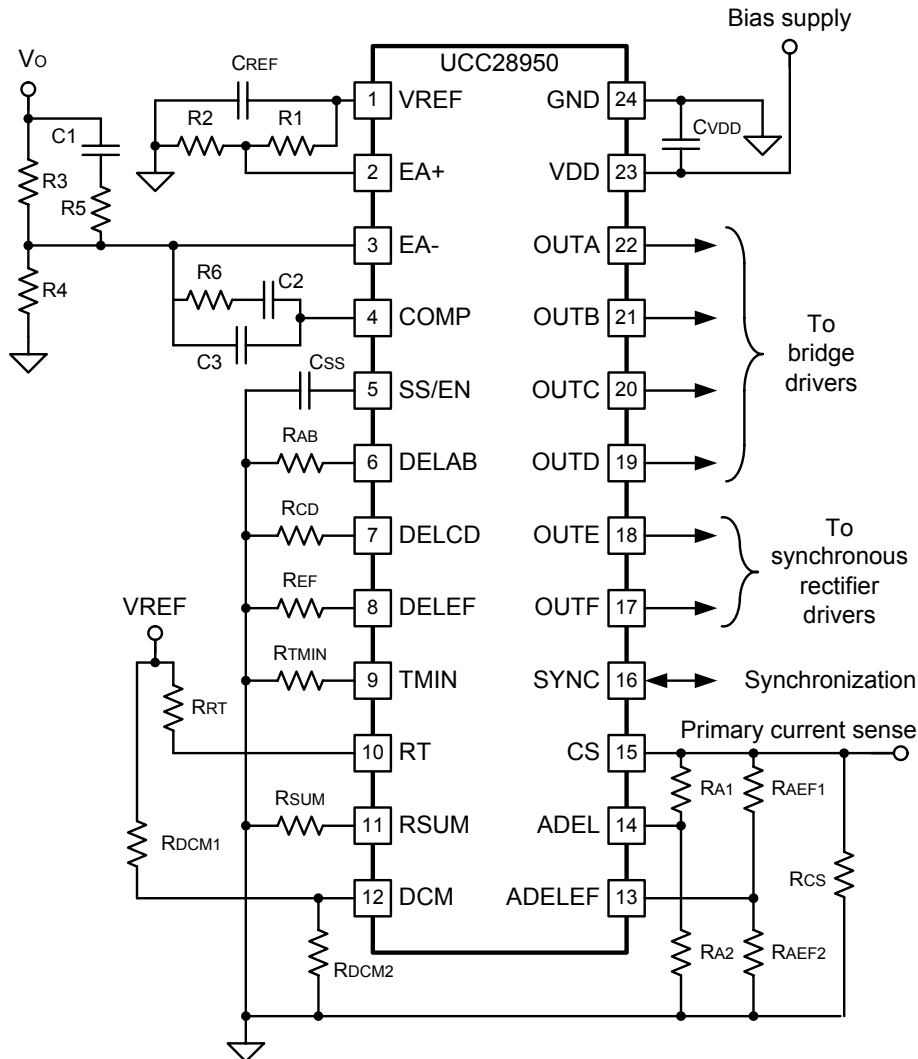


Figure 1

INTRODUCTION

The merits of lossless transitions using Zero Voltage Switching techniques have already been established in power management applications, [1-5]. Effects of the parasitic circuit elements are used advantageously to facilitate the resonant transitions as opposed to being dissipatively snubbed. This resonant tank functions to position zero voltage across the switching device prior to turn-on, eliminating any power loss due to the simultaneous overlap of switch current and voltage at each transition. High frequency converters operating from high voltage input sources stand to gain significant improvements in efficiency with this technique. The full bridge topology as shown in figure 2 will be the specific focus of this presentation, with an emphasis placed on the fixed frequency, phase shifted mode of operation.

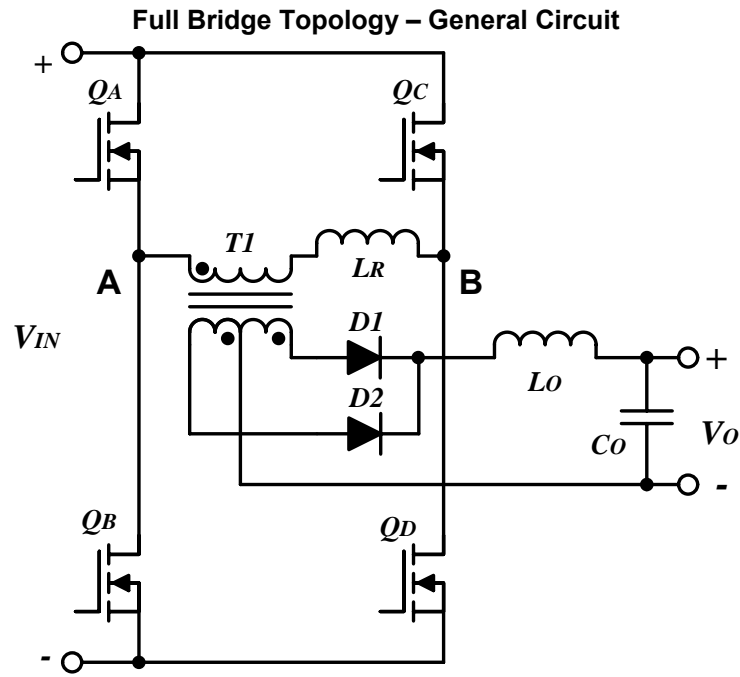


Figure 2

SWITCH DRIVE COMMANDS

The diagonal bridge switches are driven together in a conventional full bridge converter which alternately places the transformer primary across the input supply, V_{in} , for some period of time, t_{ON} as shown in figure 3.

Power is only transferred to the output section during the ON times of the switches which corresponds to a specific duty cycle when operated at fixed frequency. Additionally, the complete range of required duty cycles is unique to the application, and can be estimated from the power supply input and output voltage specifications.

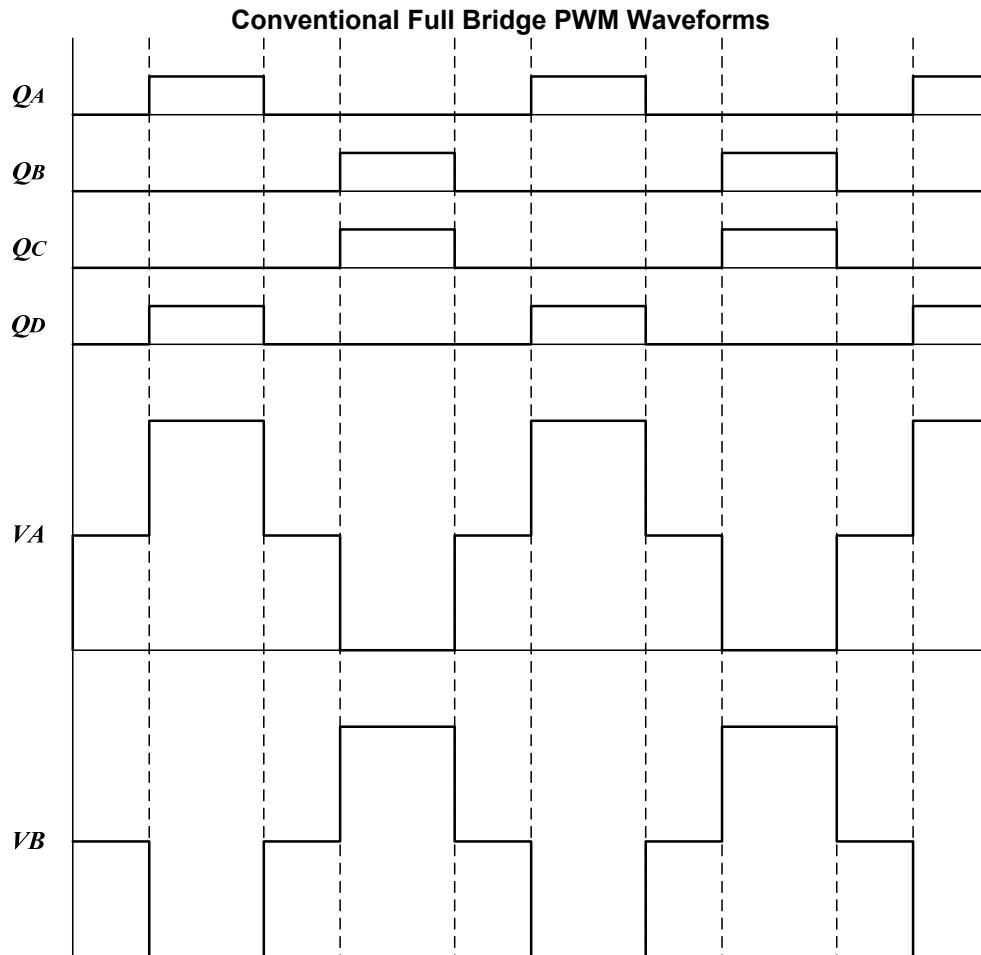


Figure 3

Rather than driving both of the diagonal full bridge switches together, a deliberate delay will be introduced between their turn-on commands with the Phase Shifted approach. This delay will be adjusted by the voltage loop of the control circuitry, and essentially results as a phase shift between the two drive signals. The effective duty cycle is controlled by varying the phase shift between the switch drive commands as shown in figure 4.

Unique to this Phase Shifted technique, two of the switches in series with the transformer can be ON, yet the applied voltage to the transformer is zero. These are not diagonal switches of the full bridge converter, but either the two upper or two lower switches. In this mode the transformer primary is essentially short circuited and clamped to the respective input rail. Primary current is maintained at its previous state since there is no voltage available for reset to take place. This dead-band fills the void between the resonant transitions and power transfer portion of the conversion cycle. Switches can be held in this state for a certain period of time which corresponds to the required off time for that particular switching cycle.

When the correct one of these switches is later turned off, the primary current flows into the switch output capacitance (C_{oss}) causing the switch drain voltage to resonate to the opposite input rail. This aligns the opposite switch of the particular bridge “leg” with zero voltage across it enabling Zero Voltage Switching upon its turn ON.

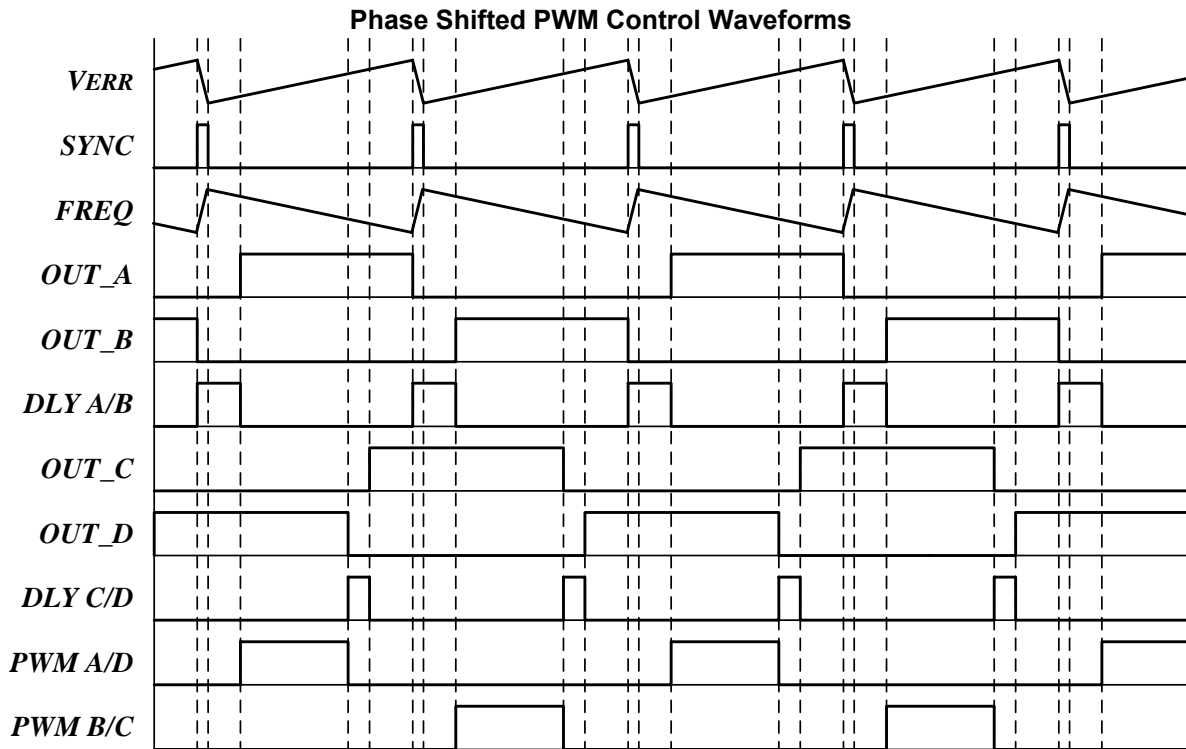


Figure 4

ZVS FUNDAMENTALS

An intentional dead-time can be introduced in the power conversion cycle whereby the switch remains off and is clamped at zero voltage by the resonant tank. Rather than turn the switch on instantly when zero voltage is attained, the switch is held off while the primary current circulates into the shorted primary through the body diode and the opposite leg switch, which is still on. This off time is used to fill in the voids between the point where zero voltage has been reached where the switch needs to be turned on to achieve fixed frequency operation.

Fixed frequency operation is obtainable over an identified range of input voltages and output currents. For reference purposes, the variable frequency ZVS technique has similar limitations for proper operation which occur at minimum output load and maximum input line as shown in figure 5.

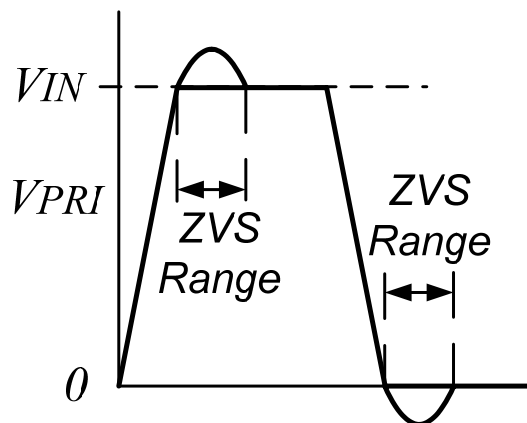


Figure 5

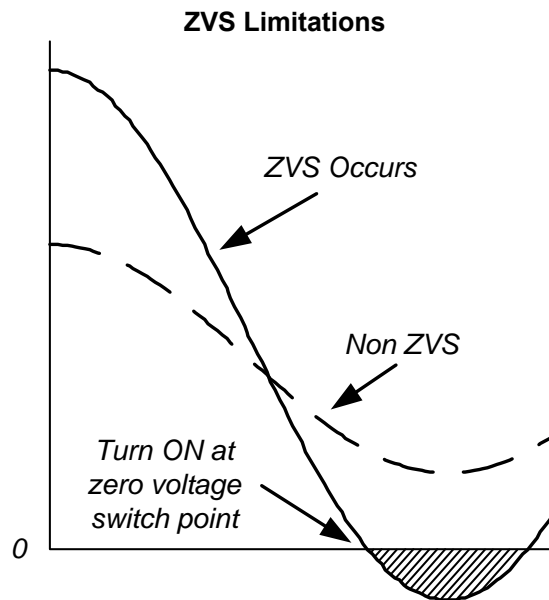


Figure 6

PHASE SHIFTED FUNDAMENTALS

Switches within the Phase Shifted full bridge converter will be utilized differently than those of its non-resonant counterpart. Instrumental to this technique is the use of the parasitic elements of the MOSFET switch's construction. The internal body diode and output capacitance (C_{oss}) of each device (in conjunction with the primary current) become the principal components used to accomplish and commutate the resonant transitions.

CIRCUIT SCHEMATIC AND DESCRIPTION

Detailed operation of the Phase Shifted Converter operation will begin following a description of the circuit elements. The circuit schematic of this technique is shown in figure 7 including voltage and current designations.

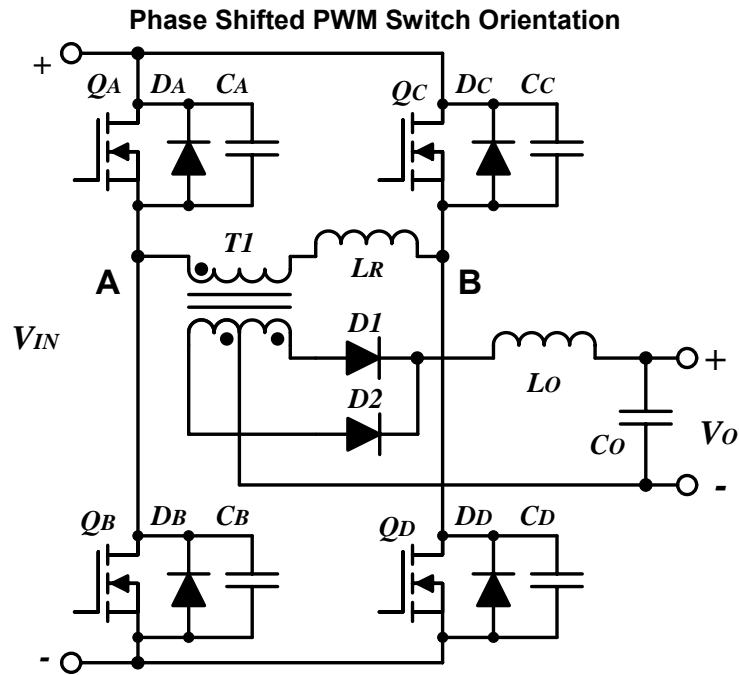


Figure 7

The basic circuit is comprised of four switches labeled Q_A through Q_D and is divided up into two “legs”, the right and left hand legs. Each switch is shown shunted by its body diode (D_A through D_D) and parasitic output capacitance, (C_A through C_D). These have been identified separately to clarify the exact elements and current paths during the conversion interval.

A detailed model of the transformer primary section is presented which separately indicates the leakage and magnetizing inductances and currents of the primary. The reflected secondary contributors to primary current are also shown for completeness, and divided into two components. The DC primary current (I_P) is the secondary DC output current divided by the transformer turns ratio (N). The secondary AC current should also be accounted for by multiplying the output inductance by the turns ratio squared (N^2), or dividing the secondary AC ripple current $I_{SEC(ac)}$ by the turns ratio (N) as shown in figure 8.

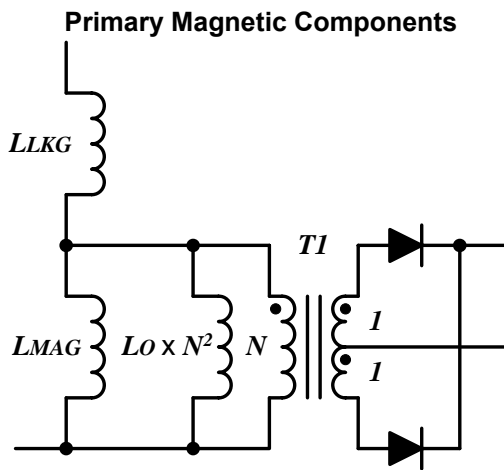
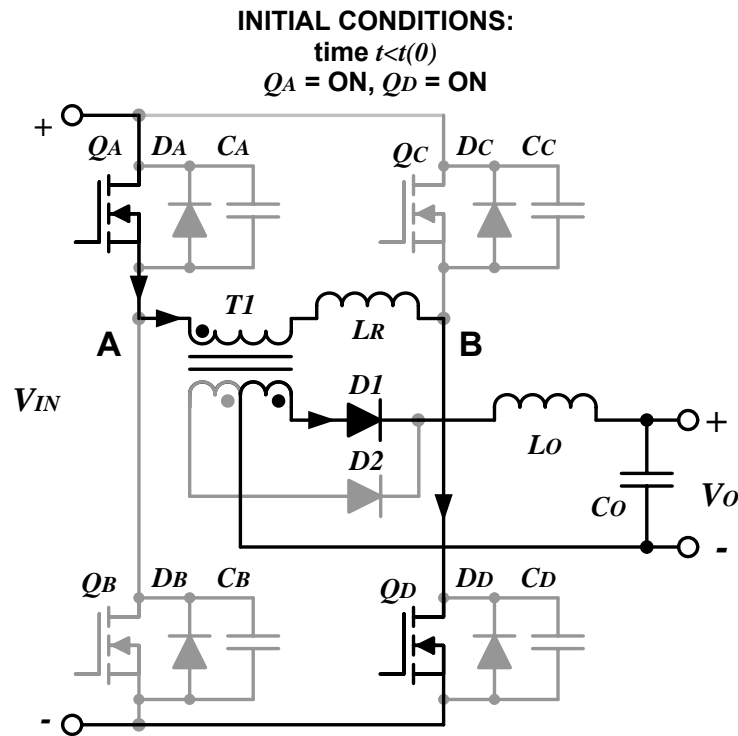


Figure 8

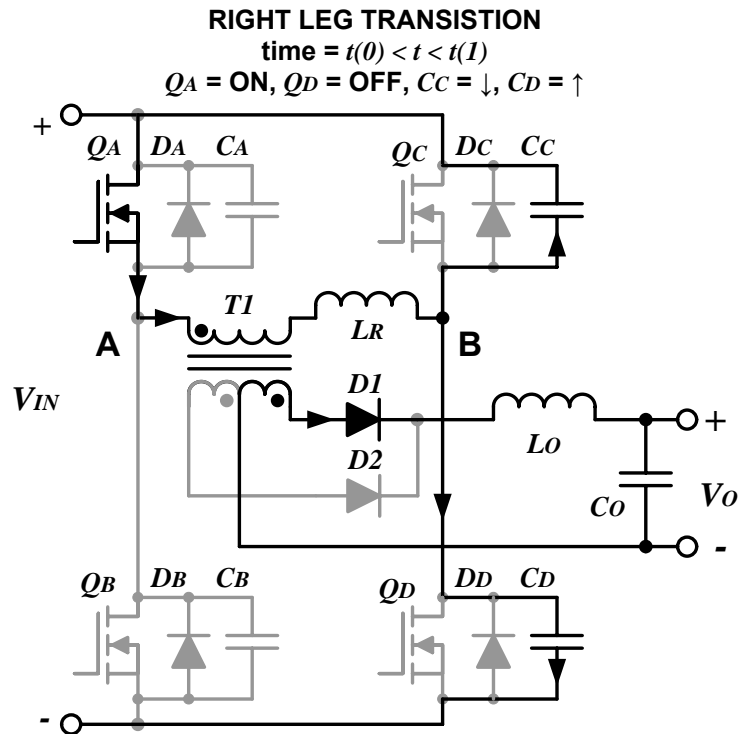
INITIAL CONDITIONS
Time: $t = t(0)$

The description of the Phase Shifted operation will begin with the conclusion of one power transfer cycle. This occurs when the transformer had been delivering power to the load and two of diagonal switches of the converter were conducting. The initial current flowing in the primary can be designated as $I_P(t(0))$.


Figure 9
RIGHT LEG RESONANT TRANSITION INTERVAL
Time: $t(0) < t < t(1)$

The primary current flowing at time $t(0)$ is equal to $I_P(t(0))$ and was being conducted through the diagonal set of transistors Q_A in the upper left hand corner of the bridge and transistor Q_D in the lower right. Instantly, at time $t(0)$ switch Q_D is turned off by the control circuitry which begins the resonant transition of the right hand leg of the converter.

The primary current flowing is maintained nearly constant at $I_P(t(0))$ by the resonant inductance of the primary circuit, often referred to as the transformers leakage inductance. Since an external series inductance can be added to alter the effective leakage inductance value, this presentation will refer to the lumped sum of these inductors as the resonant inductance, L_R . In a practical application it may be difficult to accurately control the transformers leakage inductance within an acceptable ZVS range, necessitating an external “shim” inductor to control the accuracy. It’s also possible that the transformer leakage inductance can be too low to provide the desired transition times for the application so an external inductor can be introduced to modify the resonant inductance.


Figure 10

With switch Q_D turned off, the primary current continues to flow using the switch output capacitance, C_D to provide the path. This charges the switch capacitance of Q_D from essentially zero volts to the upper voltage rail, V_{in+} . Simultaneously, the transformer capacitance (C_{xfmr}) and the output capacitance of switch Q_C is discharged as its source voltage rises from the lower to the upper rail voltage. This resonant transition positions switch Q_C with no drain to source voltage prior to turn-on and facilitates lossless, zero voltage switching.

The primary current causing this right leg transition can be approximated by the full load primary current of $I_P(t(0))$. The small change due to the barely resonant circuit contribution is assumed to be negligible in comparison to the magnitude of the full load current.

During this right leg transition the voltage across the transformers primary has decreased from V_{IN} to zero. At some point in the transition the primary voltage drops below the reflected secondary voltage, $V_O \times N$. When this occurs the primary is no longer supplying full power to the secondary and the output inductor voltage changes polarity. Simultaneously, energy stored in the output choke begins supplementing the decaying primary power until the primary contribution finally reaches zero.

Once the right leg transition has been completed there is no voltage across the transformer primary. Likewise, there is no voltage across the transformers secondary winding and no power transferred, assuming ideal conditions. Note that the resonant transition not only defines the rate of change in primary and secondary voltages dV/dt , but also the rate of change in current in the output filter network, dI/dt .

CLAMPED FREEWHEELING INTERVAL

Time: $t(1) < t < t(2)$

Once the right leg transition is complete the primary current free wheels through transistor Q_A and the body diode of switch Q_C . The current would remain constant until the next transition occurs

assuming that the components were ideal. Switch Q_C can be turned on at this time which shunts the body diode with the FET $R_{ds(on)}$ switch impedance thus lowering conduction losses. Although current is flowing opposite to the normal convention (source to drain) the channel of Q_C will conduct and divide the current between the switch and body diode.

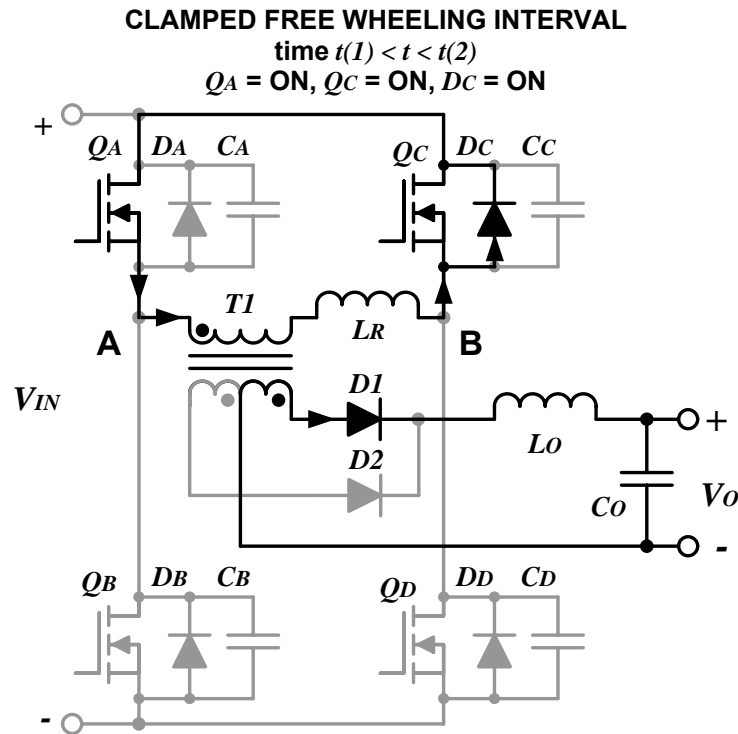


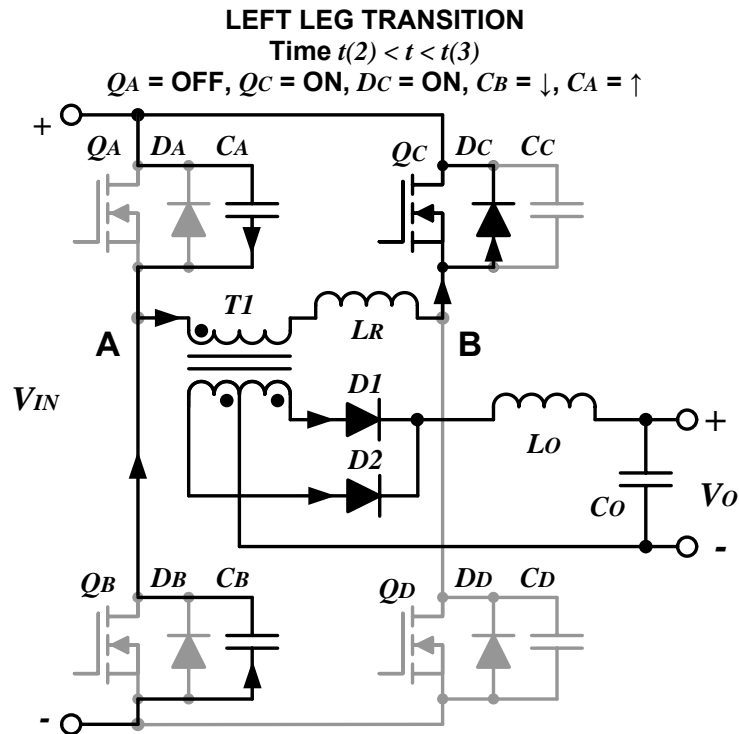
Figure 11

LEFT LEG TRANSITION INTERVAL

Time: $t(2) < t < t(3)$

At time $t(2)$ a residual current was flowing in the primary of the transformer which is slightly less than $I_P(t(0))$ due to losses. Switch Q_C has been previously turned ON and switch Q_A will now be turned OFF. The primary current will continue to flow but the path has changed to the output capacitance (C_A) of switch Q_A instead of its channel. The direction of current flowing causes the drain to source voltage of switch Q_A to increase and lowers its source from the upper to lower rail voltage. Just the opposite conditions have occurred to switch Q_B which previously had the full input across its terminals. The resonant transition now aligns switch Q_B with zero voltage across it, enabling lossless switching to occur.

Primary current continues to flow and is clamped by the body diode of switch Q_B , which is still OFF. This clamping into a short circuit is a necessary condition for fixed frequency, zero voltage switching. Once switch Q_B is turned ON, the transformer primary is placed across the input supply rails since switch Q_C is already ON and will begin to transfer power. Although zero voltage switching has already been established, turning ON switch Q_B the instant it reaches zero voltage will cause variable frequency operation.



Note that this left leg transition will require more time to complete than the right leg transition. Conduction losses in the primary switches, transformer winding and interconnections result in a net DC voltage drop due to the flowing primary current. Energy stored in the series resonant inductor and magnetizing inductance is no longer ideally clamped to zero voltage. This loss, in addition to the losses incurred during the previous transition, reduce the primary current below its initial $I_P(t(0))$ value, thus causing a longer left leg transition time than the right leg.

Unlike conventional power conversion, one transistor in the diagonal pair of the phase shifted full bridge converter is ON just before power is transferred which simplifies the gate drive. An additional benefit is realized by designating these commutating switches as the high side switches of the converter, usually far more difficult to drive than their lower side counterparts.

POWER TRANSFER INTERVAL

Time: $t(3) < t < t(4)$

This interval of the phase shifted cycle is basically identical to that of conventional square wave power conversion. Two diagonal switches are ON which applies the full input voltage across the transformer primary. Current rises at a rate determined by V_{IN} and the series primary inductance, however starts at a negative value as opposed to zero. The current will increase to a DC level equal to the output current divided by the turns ratio, I_O/N . The two time variant contributors to primary current are the magnetizing current (I_{MAG}) and the output inductor magnetizing contribution reflected to the primary, $L_O \times N^2$. The exact switch ON time is a function of V_{IN} , V_O and N the transformer turns ratio, just as with conventional converters.

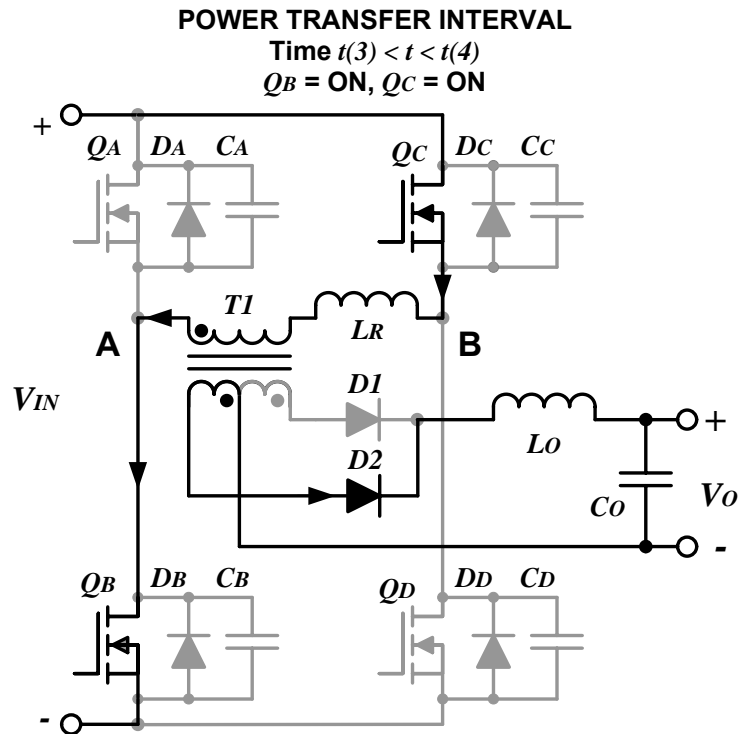
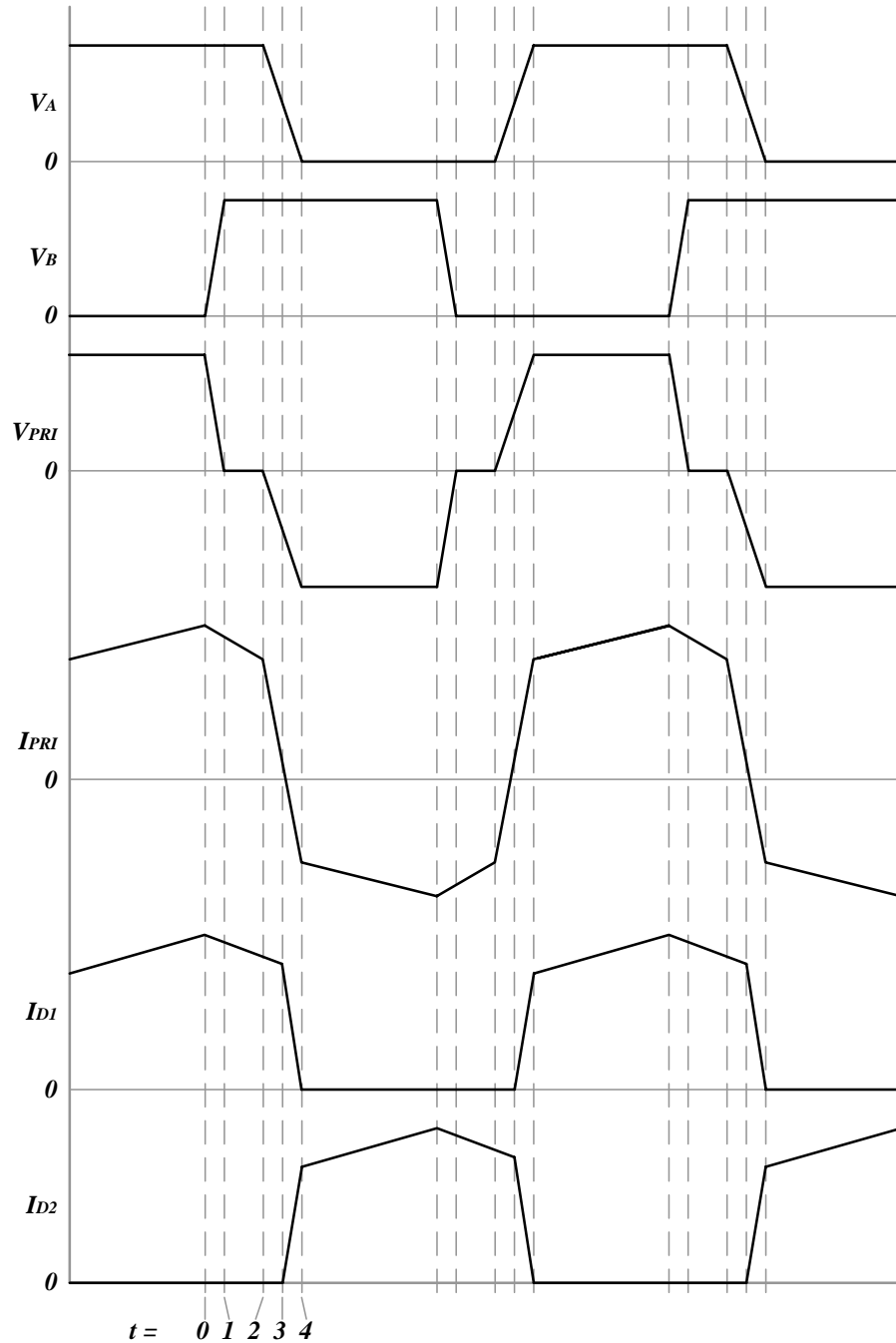


Figure 13

SWITCH TURN OFF

Time: $t(4)$

One switching cycle is concluded at time $t(4)$ when Q_C the upper right hand corner switch is turned OFF. Current stops flowing in Q_C 's semiconductor channel but continues through the parasitic output capacitance, C_C . This increases the drain-to-source voltage from essentially zero to the full input supply voltage, V_{IN} . The output capacitance of the lower switch in the right hand leg (Q_D) is simultaneously discharged via the primary current. Transistor Q_D is then optimally positioned for zero voltage switching with no drain-to-source voltage. The current during this interval is assumed to be constant, simplifying the analysis. In actuality, it is slightly resonant as mentioned in the left leg transition, but the amplitude is negligible in comparison to the full load current. The power conversion interval is concluded at this point and an identical analysis occurs as for the opposite diagonal switch set which has thoroughly been described for the switch set Q_A and Q_D .

OPERATIONAL WAVE FORMS

Figure 14
RESONANT TANK CONSIDERATIONS

The design of the resonant tank begins with the selection of an acceptable switching frequency; one selected to meet the required power density. Second, the maximum transition time must also be established based on achievable duty cycles under all operating conditions. Experience may provide the best insight for acceptable results.

The maximum transition time will occur during the converters left leg transition operating at the minimum output load current.

RESONANT CIRCUIT LIMITATIONS

Two conditions must be met by the resonant circuit at light load, and both relate to the energy stored in the resonant inductor. One, there must be enough inductive energy stored to drive the resonant capacitors to the opposite supply rail. Two, this transition must be accomplished within the allocated transition time. Lossy, non-zero voltage switching will result if either, or both are violated. The first condition will always be met when the latter is used as the resonant circuit limitation.

Designers can argue that some switching loss may be of little consequence in a practical application at very light loads - especially considering that there is a significant benefit at heavy loads. While this may be a pragmatic approach in many applications, and a valid concern, this presentation will continue using the fully lossless mode as the ultimate design goal.

The stored inductive energy requirement and specified maximum transition time have also defined the resonant frequency (ω_R) of the tank circuit. Elements of this tank are the resonant inductor (L_R) and capacitor (C_R), formed by the two switch output capacitors, also in parallel with the transformer primary capacitance C_{xfmr} . The maximum transition time cannot exceed one-fourth of the self resonant period, (four times the self resonant frequency) to satisfy the zero voltage switching condition.

The resonant tank frequency, ω_R :

$$\omega_R = \frac{1}{\sqrt{L_R \times C_R}}$$

$$t(\text{max})\text{transistion} = \frac{\pi}{2 \times \omega_R}$$

C_{oss} , the specified MOSFET switch output capacitance will be multiplied by a 4/3 factor to accommodate the increase caused by high voltage operation. During each transition, two switch capacitances are driven in parallel, doubling the total capacitance to $8/3 \times C_{oss}$. Transformer capacitance (C_{xfmr}) must also be added as it is **NOT** negligible in many high frequency applications.

The resonant capacitance, C_R :

$$C_R = \frac{8}{3} \times C_{oss} + C_{xfmr}$$

The capacitive energy required to complete the transition, $W(C_R)$ is:

$$W(C_R) = \frac{1}{2} \times C_R \times V_{Pr} i^2$$

This energy can also be expressed as:

$$W(C_R) = \left(\frac{4}{3} \times C_{oss} + \frac{1}{2} C_{xfmr} \right) \times V_{IN}^2$$

STORED INDUCTIVE ENERGY

The energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output and transformer capacitances of the leg in transition within the maximum transition time.

Inside the transformer, all of the energy is stored in the leakage inductance since the secondary current has clamped the transformers primary voltage to essentially zero. This causes high circulating primary current (as shown in figure 8) in the physical winding but has no effect on the stored energy used to perform the ZVS transition. More detail about the tradeoffs and design optimization is presented in the Design Procedure.

The energy stored in the resonant inductor, L_R :

$$W(L_R) = \frac{1}{2} \times L_R \times I_{PRI}^2$$

RESONANT CIRCUIT SUMMARY

There are several ways to arrive at the solutions for the resonant inductor value and minimum primary current required for any application. Each of these is based upon the following fundamental relationships. The resonant tank frequency must be at least four times higher than the transition time to fully resonate within the maximum transition time t_{MAX} at light load.

$$T_{RES} = 4 \times t_{MAX}$$

$$f_{RES} = \frac{1}{T_{RES}} \text{ or}$$

$$\text{where } \omega_R = 2 \times \pi \times f_{RES}$$

$$\omega_R = \frac{2 \times \pi}{T_{RES}}$$

Reorganizing and combining these relationships;

$$\omega_R = \frac{2 \times \pi}{4 \times t_{MAX}}$$

$$\omega_R = \frac{\pi}{2 \times t_{MAX}}$$

The resonant radian frequency (ω_R) is related to the resonant components by the equation:

$$\omega_R = \frac{1}{\sqrt{L_R \times C_R}}$$

Both sides of this can be squared to simplify the calculations and reorganized to solve for the exact resonant inductor value.

$$L_R = \frac{1}{\omega_R^2 \times C_R}$$

Previously outlined relationships for ω_R and C_R can be introduced to result in the following specific equation.

$$L_R = \frac{1}{\left(\frac{\pi}{2 \times t_{MAX}}\right)^2 \times \left(\frac{8}{3} \times C_{oss} + \frac{1}{2} C_{xfmr}\right)}$$

Note that this figure indicates the exact resonant inductor value required to satisfy only the task of resonant transitions. This resonant inductor is in series with the transformer primary hence also defines the maximum primary current slew rate, dI/dt as a function of input voltage.

$$\frac{dI_{PRI}}{dt} = \frac{V_{IN}}{L_R}$$

If the resonant inductor value is too large it may take too long to reach the necessary load current within the conversion cycle. The calculated inductor value satisfies the light load condition, however full load operation must also be evaluated. Details of possible solutions to this are highlighted in the Practical Applications section of this paper.

STORED ENERGY REQUIREMENTS

As detailed, the energy stored in the resonant inductor must be greater than the capacitive energy required for the transition to occur within the allocated transition time. The governing equations are summarized below.

$$\frac{1}{2} \times L_R \times I_{PRI(MIN)}^2 = \frac{1}{2} \times C_R \times V_{IN(MAX)}^2 \text{ or}$$

$$L_R \times I_{PRI(MIN)}^2 > C_R \times V_{IN(MAX)}^2$$

Since C_R and V_{IN} are known or can be estimated for a given application, this term becomes a constant and L_R has been quantified.

MINIMUM PRIMARY CURRENT

The minimum primary current required for the phase shifted application can now be determined by reorganizing the previous equation.

$$I_{PRI(MIN)} = \sqrt{\frac{C_R \times V_{IN(MAX)}^2}{L_R}}$$

This value can be supported by the calculating the average current required to slew the resonant capacitor to the full rail voltage. Although this figure will be lower than $I_{P(MIN)}$ it can be used as a confirmation of the mathematics.

$$I_{R(AVERAGE)} = C_R \times \frac{V_{IN}}{t_{MAX}}$$

Obtaining the necessary amount of primary current can be done in several ways. The most direct approach is to simply limit the minimum load current to the appropriate level. One alternative, however, is to design the transformer magnetizing inductance accordingly. Also assisting the magnetizing current is the reflected secondary inductor current contribution which is modeled in parallel. Any duty cycle variations modifying the peak charging current must also be taken into account.

Generally the magnetizing current alone is insufficient in many off-line high frequency converters. The transformer is usually core loss limited which means numerous primary turns and a high magnetizing inductance. Shunting the transformer primary with an external inductor to develop the right amount of primary current is one possibility. Incorporating the output filter inductor magnetizing current to assist resonance on the primary side is also an alternative.

SUMMARY

The fixed frequency phase shifted control technique of the full bridge converter offers numerous performance advantages over the conventional approach. Switching losses due to the simultaneous overlap of voltage and current disappear along with the dissipative discharge of the FET output capacitance. EMI/RFI is significantly lower, also due to the "soft" switching characteristics which incorporate parasitic elements of the power stage advantageously. For most applications, there is little reason to consider the traditional square wave counterpart of this phase shifted PWM technique for future designs.

Very high frequency operation of this technique, beyond 500 KHz, is probable above the optimal operating point. Transition times quickly erode the usable duty cycle to a point where the transformer turns ratio has been compromised. This could result in unreasonably high primary currents and power loss in the switches. Any incremental gains in cost or power density by reducing the size of the output filter are probably nullified by the need for larger MOSFETs and heatsinks. This phase shifted PWM technique does excel in the overall majority of mid to high power, off-line applications. Peak efficiency will be obtained in applications with moderate load ranges, however excellent results can also be obtained in most designs with load ranges of ten-to one. A subgroup of applications may exist where non ZVS operation extremely light loads is acceptable, especially when the advantages under all other operating conditions are considered.

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