Application Report
SLUA310 - April 2004

Effect of Programmable UVLO on Maximum Duty Cycle Achievable With the TPS4005x and TPS4006x Family of Synchronous Buck Controllers

System Power

ABSTRACT

The programmable UVLO function and the voltage feed-forward function are set by a single resistor and the interaction of these functions place constraints on the maximum duty cycle achievable as the input voltage is increased from the UVLO set point. This application note provides guidelines on using the programmable UVLO when high duty cycle conversion ratios are desired.

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1 Introduction

Two of the very powerful functions implemented in the TPS4005x/6x families of DC/DC controllers are programmable UVLO and voltage feed-forward. However, interaction of these functions make it necessary to understand the implementation in order to use them effectively.

Programmable UVLO allows the user to select, or program, the voltage at which the device begins to operate. For example, in a 24-V system, the user may not want the device to operate below 18 V. Setting the UVLO to 18 V keeps the device off until the input voltage is 18 V or greater. Otherwise, the device would start operating at an input voltage of 8 V to 10 V.

Voltage feed-forward is a technique to improve the stability and transient response of the feedback loop by maintaining a constant modulator gain as the input voltage varies. The implementation increases the slope of the ramp into the comparator so the COMP voltage does not have to change in order to change the duty cycle.

The device implementation of the circuits is shown in Figure 1. The dependency of the R_{KFF} value to R_T can be seen since the current charging C1 comes from R_{KFF} and the reset time of C1 is determined by R_T. The resistor R_T sets the switching frequency and the timing for the UVLO detection. A description of the functional blocks is given.

- U1 is the error amplifier that varies the voltage on the COMP pin to control the duty cycle and maintain regulation.
- U2 is the comparator that generates the PWM information from the COMP voltage and the RAMP signal.
- U3 is an up/down counter and generates an output (UVLO) when it has counted down to zero. An up count means that the output of U4 is HIGH when the output of the CLOCK GEN is HIGH. If the output of U4 is low when the CLOCK GEN output is HIGH, the count is decremented. At start-up the count is reset to zero and a UVLO signal keeps the output of the PWM comparator low by turning on SW1. As the input voltage is increased, the output of U4 is HIGH at the end of the clock cycle and an up count increments U3. When 7 counts have accumulated, the UVLO signal is cleared, SW1 is turned off, and the PWM outputs allow the controller to start producing output voltage.
- U4 is the comparator that compares the amplitude of the RAMP to a 1.8-V reference and declares an under voltage event if the ramp in not at least 1.8-V at the end of the clock cycle. The RAMP amplitude is determined by the amount of current delivered to C1 in a clock interval. The minimum input voltage (and hence minimum current charging C1) that produces 1.8 V on C1 during a clock cycle is called the UVLO voltage. For voltages higher than this UVLO voltage, the current into C1 ensures the voltage at the end of the clock cycle is always greater than 1.8 V and the output of U4 HIGH.
- U5 is the comparator that limits the RAMP amplitude to 2V. If the current into C1 causes the RAMP amplitude to reach 2 V in a clock cycle, the output of U5, through OR gate, U6, discharges C1 with SW2. If the RAMP voltage does not reach 2 V in a clock cycle, the output of the CLOCK GEN discharges C1 through U6.
- I1 is a current controlled current source that generates a current equal to one tenth of the I_{KFF} current.
- V1 is an active 3.5-V clamp that scales the I_{KFF} current by one tenth and controls the current generated by I1.
- I_{KFF} is the feed forward current and is determined by the difference (V_{IN} − 3.5 V) and R_{KFF}.

2 Programmable UVLO

When a UVLO condition is detected, the soft-start capacitor is discharged to about 200 mV, the COMP pin is pulled to ground, and another soft-start cycle commences.

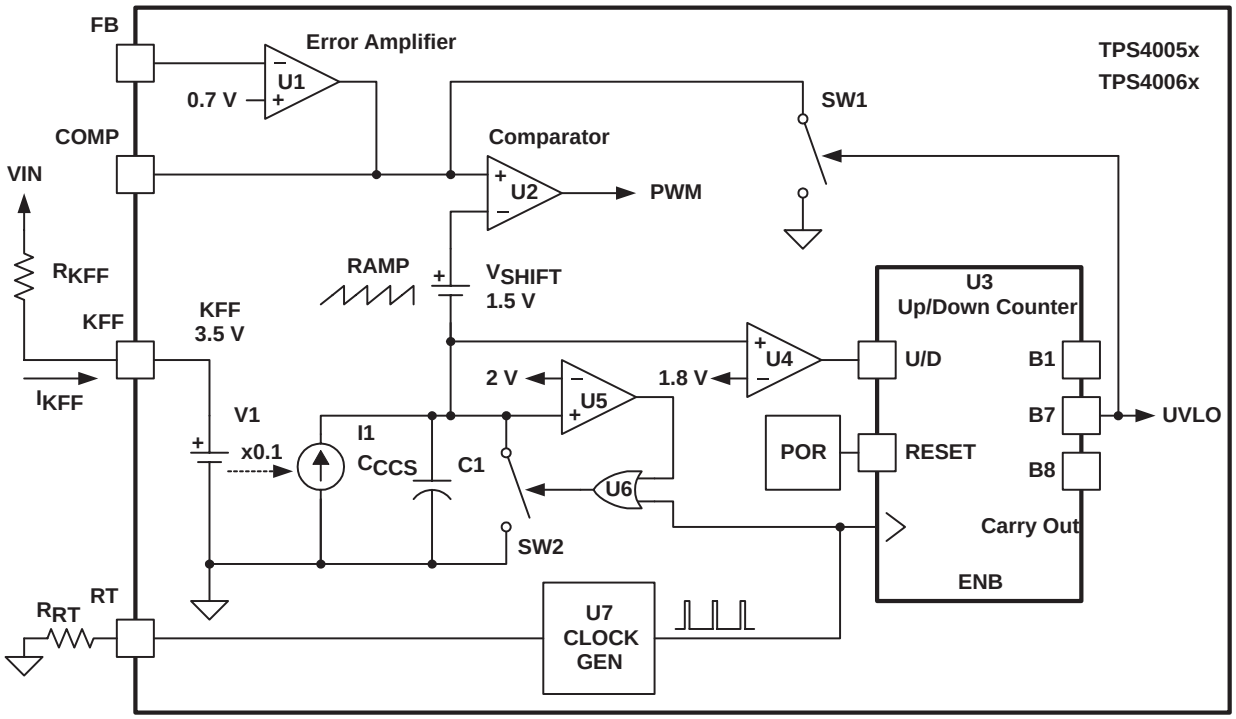

Figure 1. Programmable UVLO Implementation

The selection of the UVLO set-point, at a given switching frequency, is determined by external resistor, R_{KFF}. The equation, given in the respective data sheets, provides the proper current to charge capacitor C1 to 2 V. The equation allows for a margin of about 10% in the nominal start-up value of V_{IN}. This is because at an input voltage of about 10% lower than calculated, the capacitor voltage reaches 1.8 V and the up/down counter, U3, stops decrementing the up/down counter as the input voltage increases.

The CLOCK GEN function, U7, determines the switching frequency and is set by external resistor, R_{RT}. The current that generates the RAMP signal for the PWM comparator, U2, is determined by the I_{KFF} current which is determined by the difference between the input voltage and the KFF voltage of 3.5 V. The KFF current (I_{KFF}) is scaled by one tenth and charges the ramp capacitor, C1. The amplitude of the ramp is limited to 2 V by comparator U5 which resets the voltage on C1 to zero. In addition, capacitor C1 is reset by the CLOCK GEN if the ramp amplitude is not reset by U5.

After C1 is discharged, it does not start charging again until the falling edge of the CLOCK GEN signal.

The UVLO output signals an undervoltage condition if the up/down counter, U3, decrements to zero. When the comparator output is low during the clock interval, capacitor C1 does not reach a charge of 1.8 V. This results when V_{IN} is too low to provide the necessary charge current to C1 and therefore falls below the UVLO set point.

This current controls the slope of the RAMP and therefore effects the voltage feed forward function described below.

3 Input Voltage Feed Forward

The TPS4005x/6x family of dc-to-dc controllers is used in many applications converting from a relatively high input voltage, 12 V or 24 V, to output voltages of 1.5 V to 2.5 V. For these applications the duty cycle is less than 30% and the voltage feed forward does not constrain the duty cycle as the input voltage increases.

However, if the input is 12 V and the desired output voltage is 10 V, the nominal duty cycle is 83% and the duty cycle is affected by the voltage feed-forward, as the input voltage increases. The resultant effect, for large duty cycle implementations, is that the output voltage could fall out of regulation as the input voltage increases.

Figure 2 shows the ideal voltage feed-forward waveforms. PWM1 represents the duty cycle at input voltage, V_{IN1}, which generates RAMP1. As the input voltage, V_{IN}, is doubled, the resultant increase in the I_{KFF} current causes the RAMP2 slope to double and the resultant duty cycle to be one-half of PWM1 as shown in the PWM2 waveform.

However, because the voltage on the KFF pin is 3.5 V, the variation in I_{KFF} current is not linear as V_{IN} increases from the UVLO set point.

For example, the equation for the feed forward current, I_{KFF} is:

$$I_{KFF} = \frac{V_{IN} - 3.5\ V}{R_{KFF}} \quad (1)$$

If the UVLO is set to V_{IN} = 10 V, the I_{KFF} current is:

$$I_{KFF} = \frac{6.5\ V}{R_{KFF}} \quad (2)$$

when V_{IN} is doubled to 20 V, the I_{KFF} current is

$$I_{KFF} = \frac{16.5\ V}{R_{KFF}} \quad (3)$$

Note that I_{KFF} has increased by more than 2.5 times for a 2 times increase in V_{IN}.

The result of having excess current charging C1, is excessive slope of RAMP3 as shown in Figure 3. This increased slope would produce a duty cycle that is too small. Therefore, the output would fall out of regulation unless the COMP voltage increases to provide the proper duty cycle. However, as shown in Figure 1, comparator U5 clamps the maximum ramp excursion to 2 V. Figure 3 shows the ramp amplitude reaching the maximum 2 V (3.5 V into PWM comparator U2 due to the 1.5 V, V_{SHIFT}) before the COMP voltage is reached. Therefore, the duty cycle is terminated by the 3.5 V clamp instead of COMP and the duty cycle does not continue to increase, causing the output voltage to fall out of regulation.

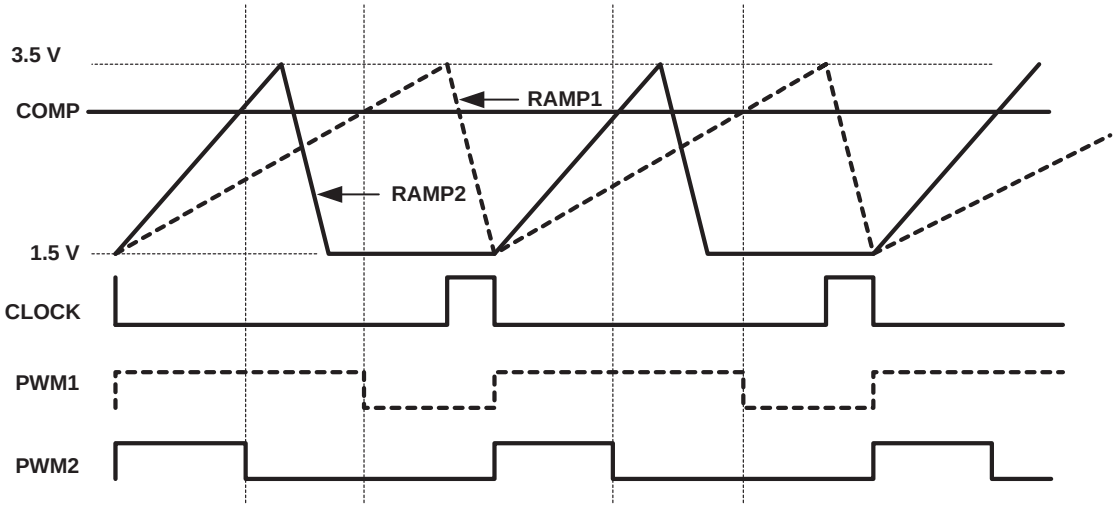

Figure 2. Ideal Variation in Duty Cycle Affected by Voltage Feed-Forward

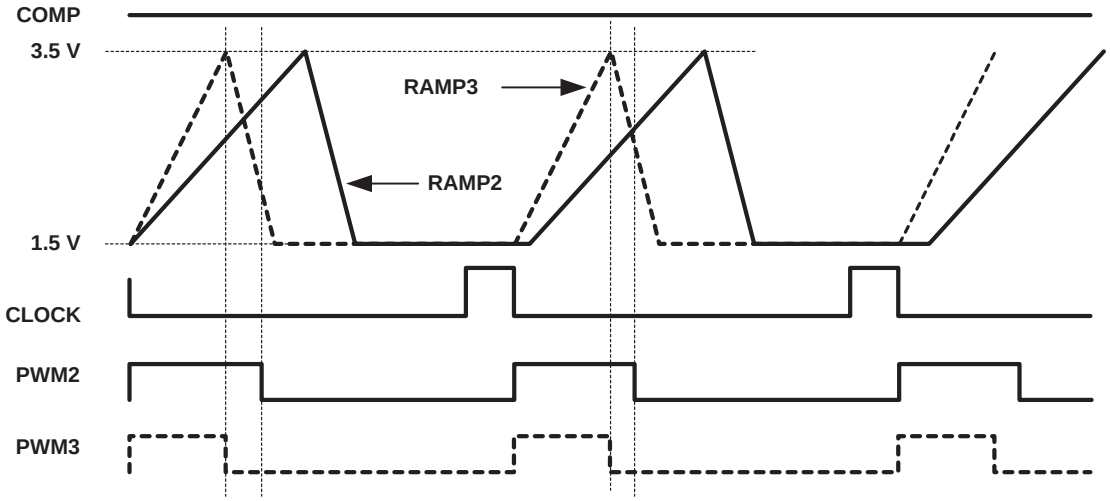

Figure 3. Variation in Duty Cycle Affected by Excessive Current in Voltage Feed-Forward

For 300 kHz and 520 kHz designs, the maximum duty cycle versus input voltage for various UVLO set points is shown in Figures 4 and 6 respectively.

In general, the maximum duty cycle at a given input voltage, V_{IN}, is calculated from:

$$D_{MAX} = \frac{R_{KFF} \times \Delta V \times C}{0.1 \times \left(V_{IN} - 3.5\ V\right) \times t_{SW}} \quad (4)$$

where

- R_{KFF} is the UVLO set resistor
- Δ V is the maximum voltage of the ramp, 2.0 V
- C is the ramp capacitor, 13.5pF
- V_{IN} is the voltage where the maximum duty cycle is desired
- t_{SW} is switching period

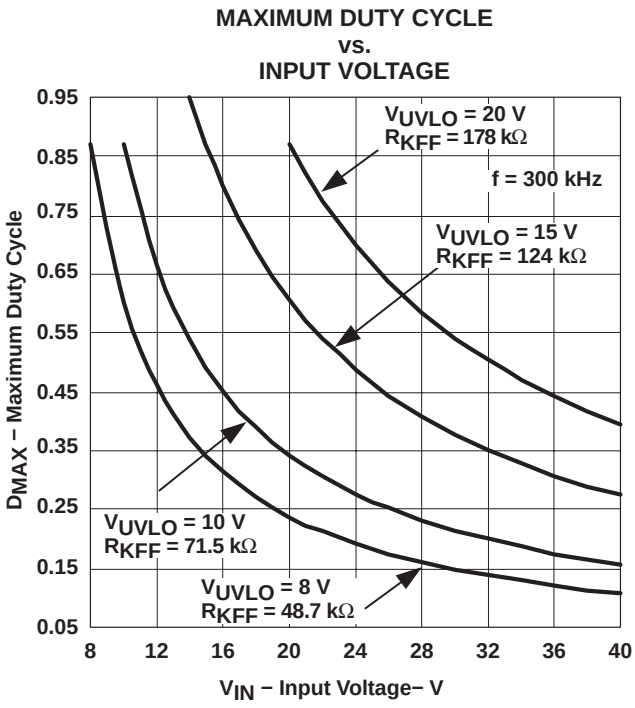

Figure 4.

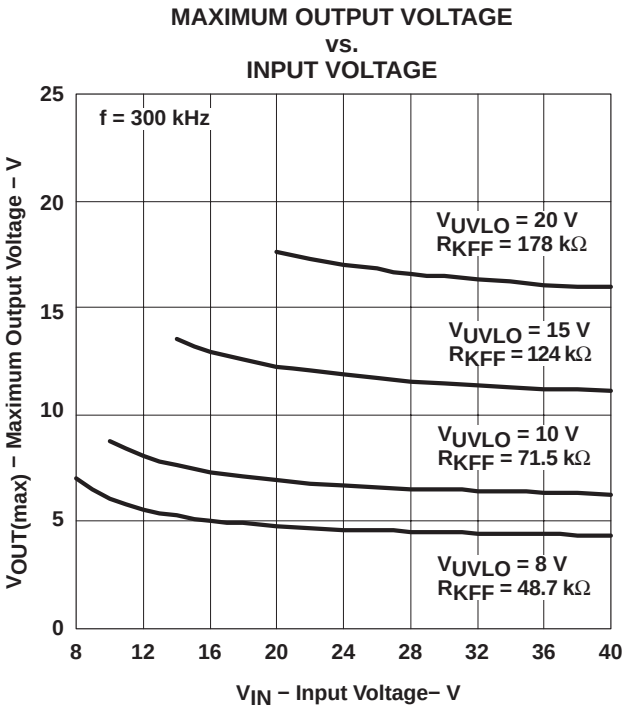

Figure 5.

Another way to show this data is the maximum obtainable output voltage for a given input voltage and UVLO set point (by multiplying maximum duty cycle by V_{IN}) as in Figure 5 and Figure 7.

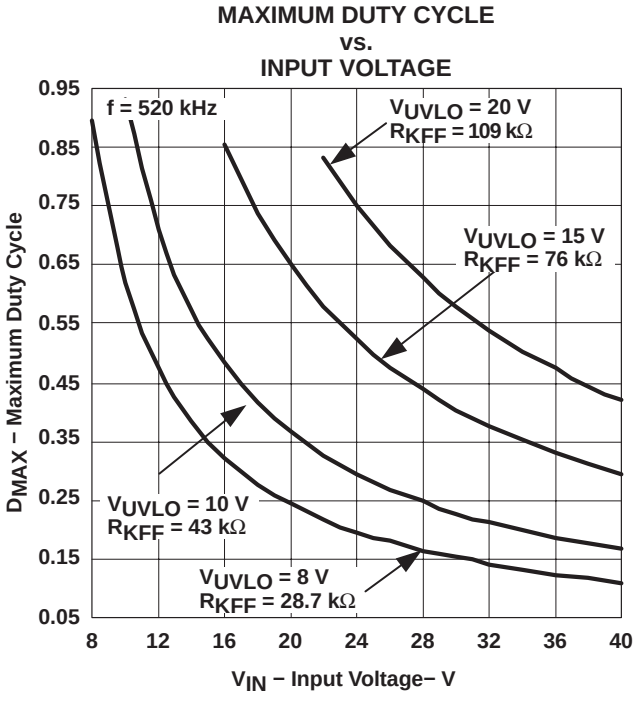

Figure 6.

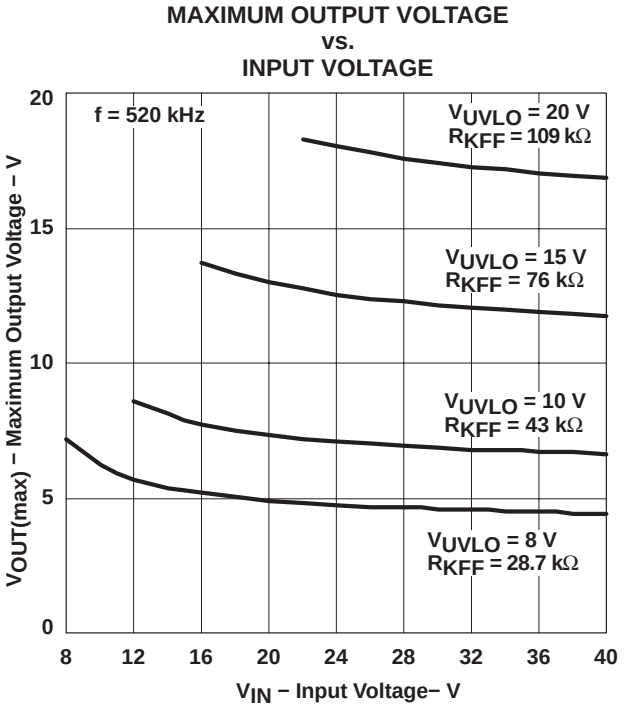

Figure 7.

4 Application Options

There may be applications where maintaining a large duty cycle over variations in the input voltage is more important than having the voltage feed-forward function or programmable UVLO. Two options are shown below. The first approach provides voltage feed-forward with an input voltage up to about 12 V. The second approach disables the feed-forward and UVLO function totally.

4.1 Limiting the Voltage Feed-Forward for the TPS40050/51/53/54/55/57 (R_{KFF} to BP10)

For a UVLO set point of about 8 V (for the TPS4005x family) or 10 V (for the TPS4006x family), voltage feed-forward and programmable UVLO can be implemented for an input up to about 12 V maximum. After the input is above approximately 12 V, there is no further increase in I_{KFF} with V_{IN}.

To implement this, calculate the R_{KFF} resistor to give the appropriate UVLO as determined by the datasheet equation for R_{KFF}, and determine the I_{KFF} current by:

$$I_{KFF} = \frac{V_{IN} - 3.5\ V}{R_{KFF}} \tag{5}$$

Use Figure 9 to determine the value of BP10 that corresponds to V_{IN}, used to calculate the UVLO point. Using the value of BP10 from Figure 9, calculate the value of resistor between BP10 and KFF that yields the same I_{KFF} current from equation (5).

$$R_{SUB} = \frac{V_{BP10} - 3.5\ V}{I_{KFF}} \tag{6}$$

where

- BP10 is the internal linear regulator output (see Figure 9)
- R_{SUB} is the substitute resistor for R_{KFF}

This provides voltage feed-forward up to an input voltage of about 12 V.

With R_{SUB} connected between BP10 and KFF, as shown in Figure 8, the RAMP capacitor has the appropriate current for the chosen switching frequency.

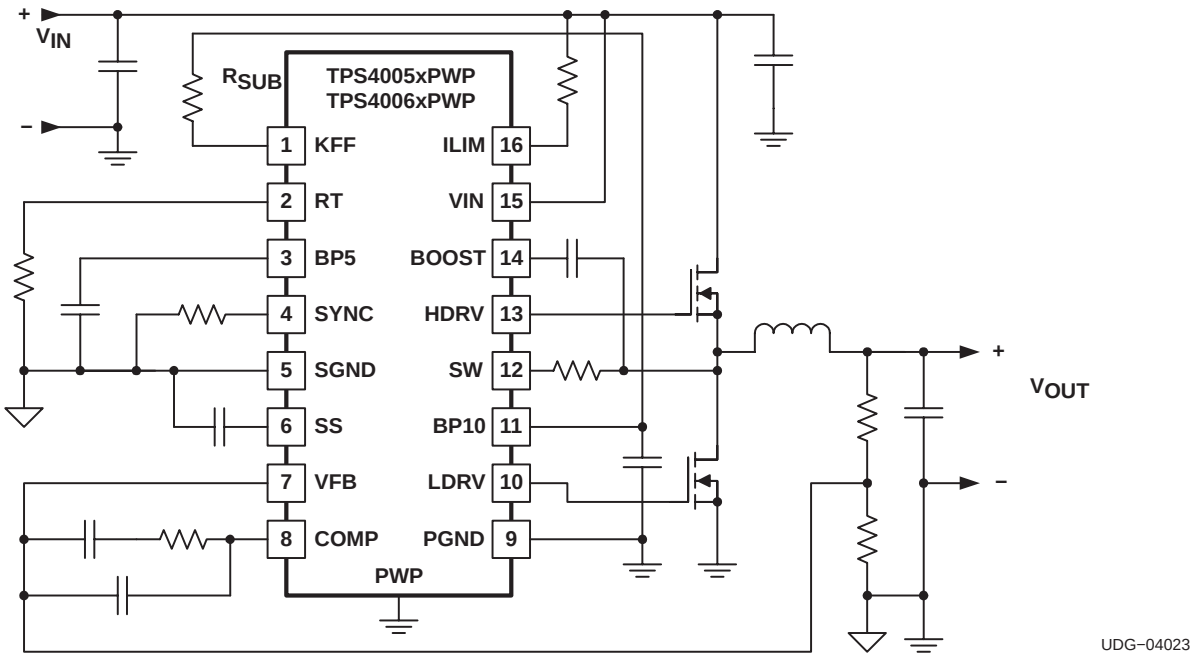

Figure 8. Limiting Range of V_{IN} to Provide Feed-Forward Function

Since BP10 does track the input voltage up to about 12 V, with a 2 V offset, there is a voltage feed-forward function as V_{IN} varies from 10 V to 12 V. Above an input voltage of 12 V, BP10 becomes a constant and there is no further feed-forward function.

Because the voltage feed-forward function has been purposely limited, care must be taken with the feedback loop to insure that at maximum V_{IN} (maximum modulator gain) and at the lowest V_{IN}, the loop is still stable.

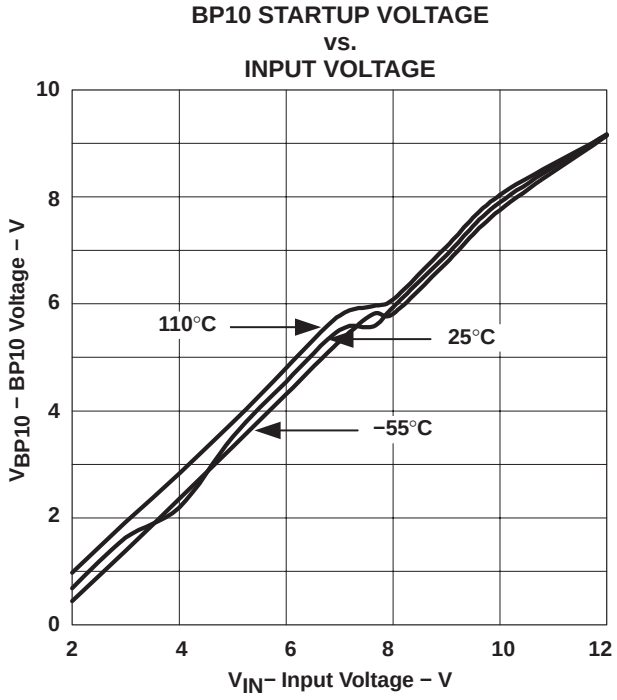

Figure 9.

4.2 Disabling the Voltage Feed-Forward (R_{KFF} to BP5)

A way to disable the feed-forward function and programmable UVLO would be to provide a constant I_{KFF} current regardless of the value of the input voltage. This is done by calculating the R_{KFF} resistor to give the appropriate I_{KFF} current for the operating frequency, using a V_{IN} minimum of 8 V for the (TPS4005x family) or 10 V (for the TPS4006x family).

To implement this, calculate the R_{KFF} resistor to give the appropriate UVLO at the switching frequency as determined by the datasheet equation for R_{KFF} and determine the I_{KFF} current by :

$$I_{KFF} = \frac{V_{IN} - 3.5\ V}{R_{KFF}} \tag{7}$$

With the value of I_{KFF} from equation (7), calculate the R_{SUB} value from equation (8).

$$R_{SUB} = \frac{5\ V - 3.5\ V}{I_{KFF}} \tag{8}$$

With R_{SUB} connected between BP5 and KFF, as shown in Figure 10, the RAMP capacitor has the appropriate current for the chosen switching frequency.

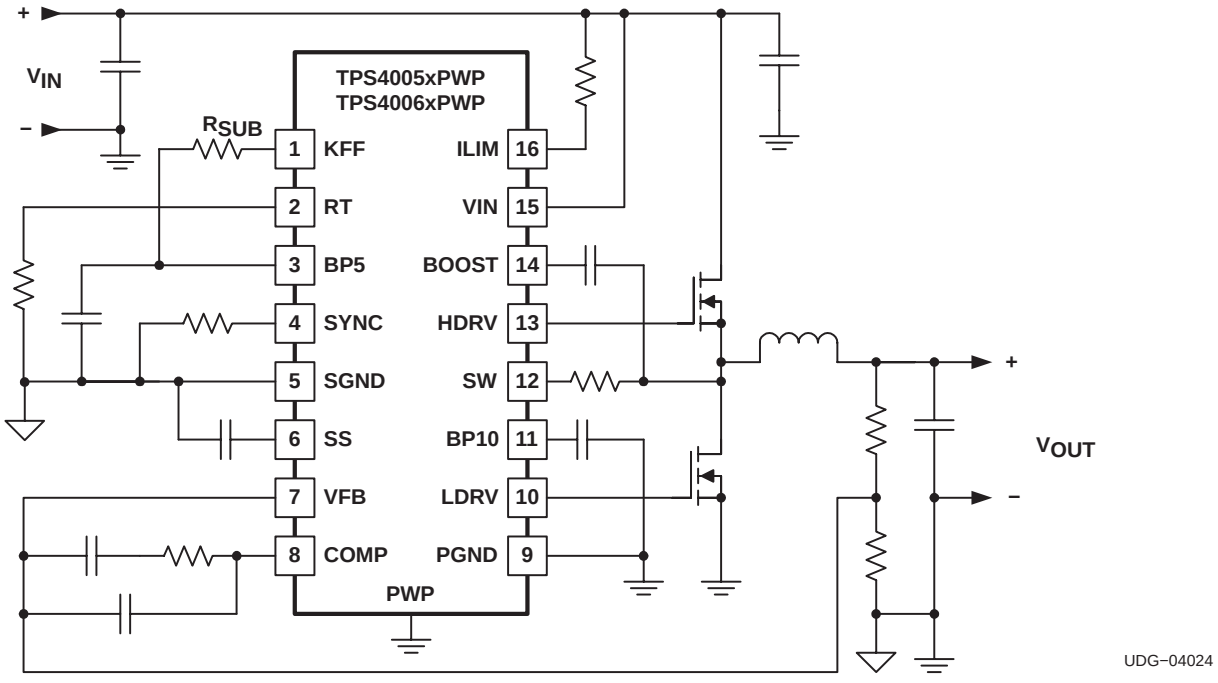

Figure 10. Disabling the Voltage Feed-Forward Function

This constant I_{KFF} current allows the converter to start up based on a fixed UVLO. The duty cycle is controlled by the output voltage feedback loop only, and not variations in the input voltage.

Because the voltage feed-forward function has been purposely defeated, care must be taken with the feedback loop to ensure that at maximum V_{IN} (maximum modulator gain) and at the lowest input voltage, the loop is still stable.

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