UCC21520: A Universal Isolated Gate Driver with Fast Dynamic Response

Application Report

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UCC21520: A Universal Isolated Gate Driver with Fast Dynamic Response

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ABSTRACT

Developed for high-voltage applications where isolation and reliability is required, the UCC21520 delivers reinforced isolation of 5.7 kV_{RMS} along with a common mode transient immunity (CMTI) greater than 100 V/ns, and it has the industry's best-in-class propagation delay of 19 ns and the best channel-to-channel delay matching of less than 5 ns which enables high switching frequency, high-power density and efficiency. In this application report, design considerations and benefits of the UCC21520's fast dynamic response are introduced with discussion of its wide application in a great variety of power electronics topologies.

1 Trademarks

2 Introduction

To fully enhance the performance of the latest high-voltage power semiconductors, such as super junction MOSFETs, trench/field stop IGBTs, wide band-gap SiC and GaN transistors, a universal gate driver becomes a critical interface which not only supports enough peak source/sink current, but also facilitates fast dynamic response with robustness and protection for higher switching frequency and higher efficiency applications.

The flexible, universal capability of the UCC21520 with up to 18-V VCCI and 25-V VDDA/VDDB allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver with MOSFETs, IGBTs or SiC MOSFETs. With its integrated components, advanced protection features (UVLO, deadtime and disable) and the optimized dynamic performances, the UCC21520 enables designers to build smaller, more robust designs for enterprise, telecom, automotive and industrial applications allowing for faster time to market.

The two output buffer stages of UCC21520 provides 4-A source and 6-A sink current, which provides satisfied rising and falling time (<30 ns) with load capacitance up to 10 nF. However, in some scenarios where the load is larger than 10 nF, external totem-pole buffer stage with discrete transistor should be applied for achieving required rising and falling switching time. Figure 1 shows the UCC21520 drives 30 nF with single channel (green), and the rising time is 110 ns from 5 V to 20 V on the output waveform, which is too long and does increase the switching loss. UCC21520 has two identical designed channels with both propagation delay matching and pulse width distortion less than 5 ns, which make it possible to parallel the output channel and double the gate drive strength. This application note will investigate the dynamic performance of the UCC21520, and also discusses feasibility of paralleling UCC21520 two output channels.

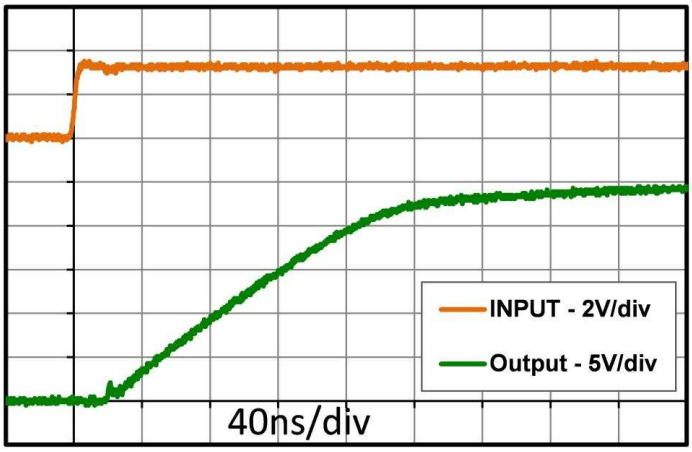

Figure 1. Single Channel Driving 30-nF Load Capacitance

3 Internal Shoot-Through with Mismatched Propagation Delay

The propagation delay mismatch will introduce internal shoot-through if the two output channels are paralleled. Figure 2 shows the simplified circuit diagram with UCC21520 two output channels in parallel driving a heavy load. In this example, it is assumed that the channel A turn-on happens earlier than channel B, or channel A turn-off later than channel B. The red dotted line shows the shoot-through path which shorts VDD to ground with very small impedance, which is typically 1.5 Ω combining pull-up and pull-down resistance. Therefore, there will be large current flow through the gate driver device, and will result in additional internal heat. The estimated loss per cycle can be calculated by:

$$P_{ST} = \left[V_{DD} \cdot I_{ST} \cdot t_{DM\_Rise} + V_{DD} \cdot I_{ST} \cdot t_{DM\_Fall} \right] \times f_{SW} \quad (1)$$

where

- P_{ST}: Shoot-through introduced extra loss;
- V_{DD}: Supply voltage on VDDA and VDDB;
- I_{ST}: Shoot-through current, decided by the pull-up and pull-down circuit design;
- t_{DM_Rise}: Propagation delay matching at rising edge;
- t_{DM_Fall}: Propagation delay matching at falling edge;
- f_{SW}: switching frequency;

To make sure UCC21520 two channels can be used in parallel, it is essential to quantify the delay matching data at different VDD voltage and temperature.

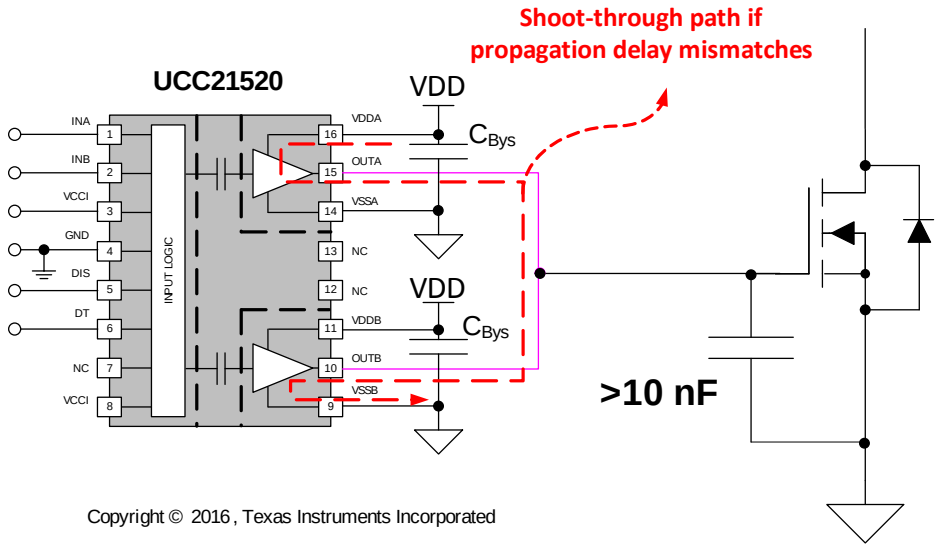

Figure 2. Internal Shoot-Through with Mismatched Propagation Delay Between Output Channels

4 UCC21520 Dynamic Characteristics

To evaluate the dynamic characteristics of the UCC21520, propagation delay, propagation delay matching and pulse width distortion performance are tested through different VDD voltage and temperature corners. For definition of these parameters, please refer to UCC21520 datasheet.

Figure 3 and Figure 4 show the propagation delay measurement data with temperature and VDD voltage corners. It can be seen that the propagation delay is independent of VDD voltage, and the typical propagation delay is less than 20 ns across wide temperature range, which helps to improve system response for high frequency applications, for example, timing control of zero voltage switching (ZVS), fast response for system protection, etc.

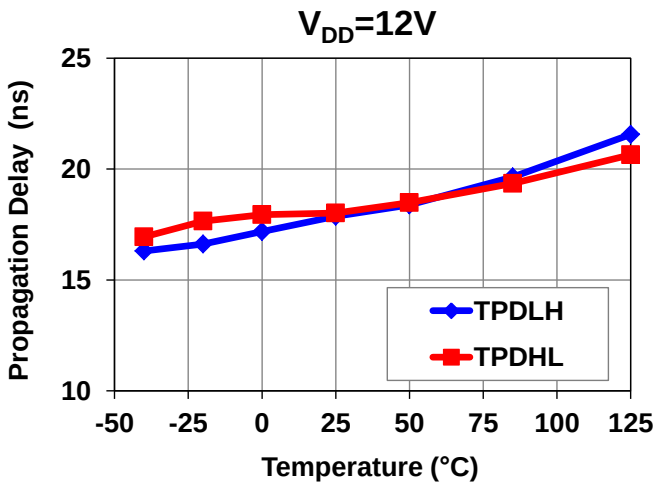

Figure 3. Propagation Delay vs. Temperature

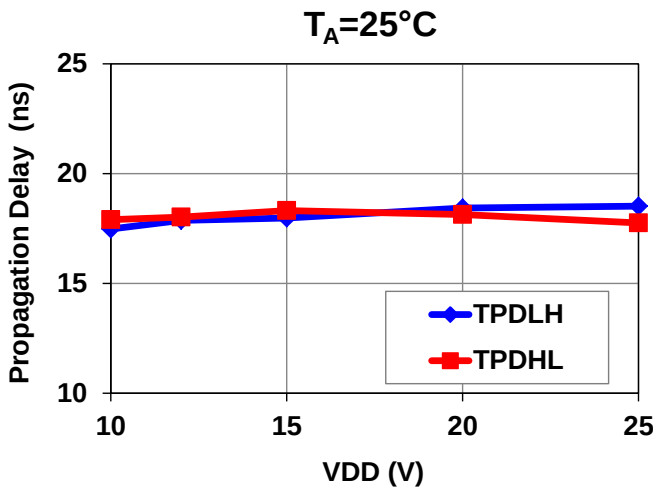

Figure 4. Propagation Delay vs. VDD

Figure 5 and Figure 6 show the propagation delay matching measurement data at temperature and VDD voltage corners. It can be seen that the delay matching at both the rising and falling edges is less than 2 ns within wide temperature and VDD ranges, which does help the channel parallel performance to drive large capacitance load.

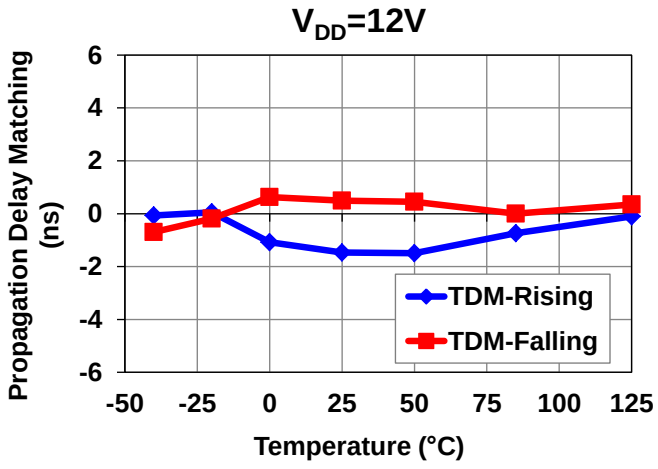

Figure 5. Propagation Delay Matching vs. Temperature

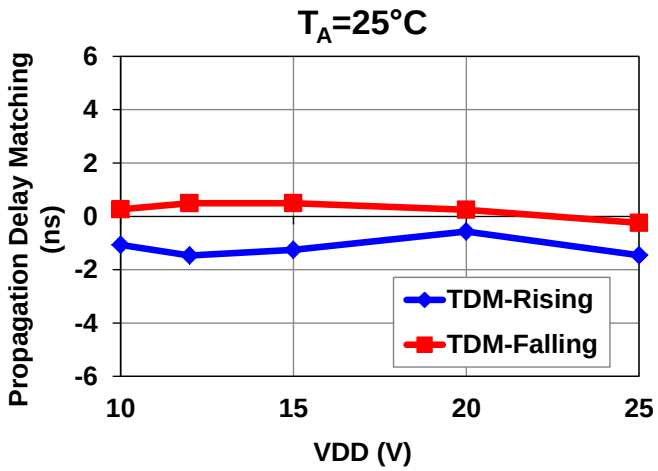

Figure 6. Propagation Delay Matching vs. VDD

Figure 7 and Figure 8 shows the pulse width distortion (PWD) measurement data, and it is less than 1 ns through all the temperature and VDD voltage corners. Low PWD does help deliver the correct and precise response with the given input signal, and maintain stable system operation.

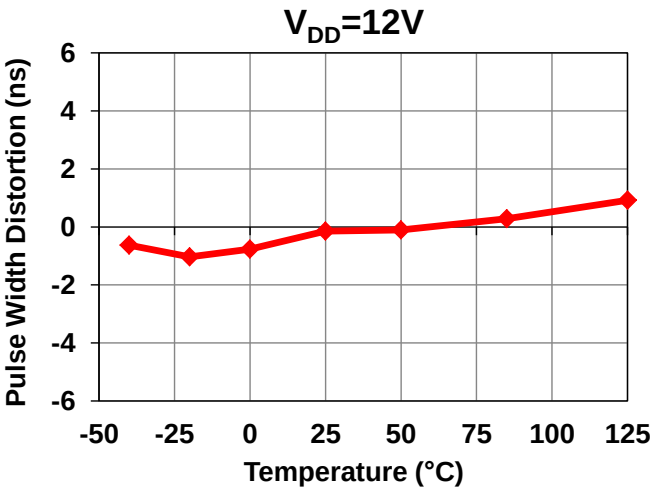

Figure 7. PWD vs. Temperature

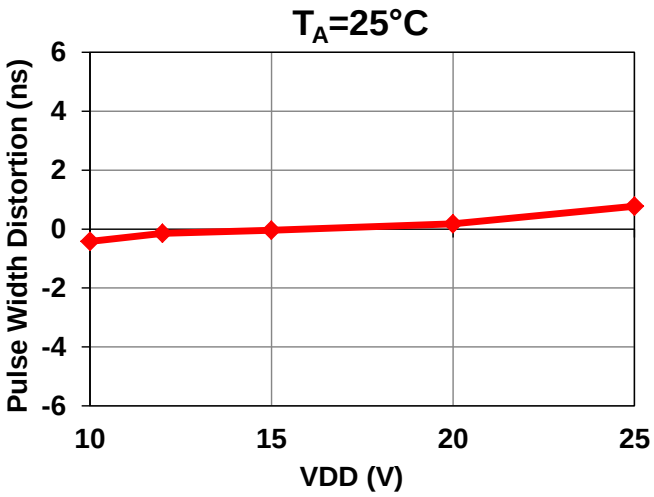

Figure 8. PWD vs. VDD

In summary, low propagation delay, low propagation delay matching and low pulse width distortion does position the UCC21520 as the best-in-class gate driver with the best-in-class dynamic response. It is important to note that less than 2-ns propagation delay matching help to parallel the two output channels, double the gate drive strength and increase the versatility of the UCC21520 for a variety of applications.

5 Parallel UCC21520 Output Channels

5.1 UCC21520 Efficiently Drives Heavy Capacitive Loads by Paralleling its Output Channels

To further evaluate the UCC21520 with two output channels in parallel, two test setups are prepared to investigate the performance difference. As discussed in Section 3, extra power loss introduced by propagation delay mismatch will add to the typical power consumption.

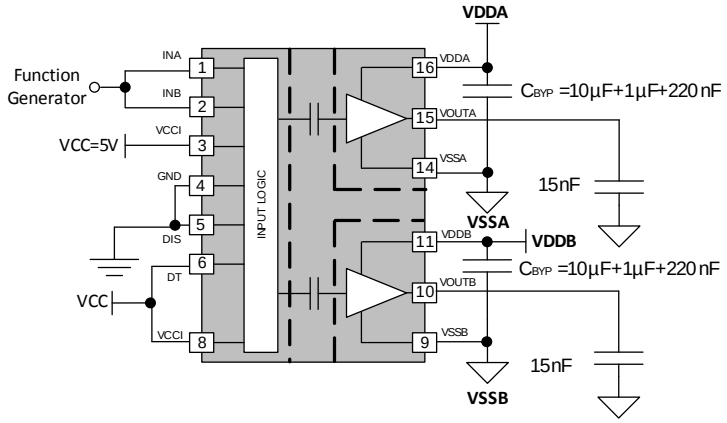

Figure 9. Setup A: UCC21520 Drives Two 15-nF Loads with Two Channels Separately

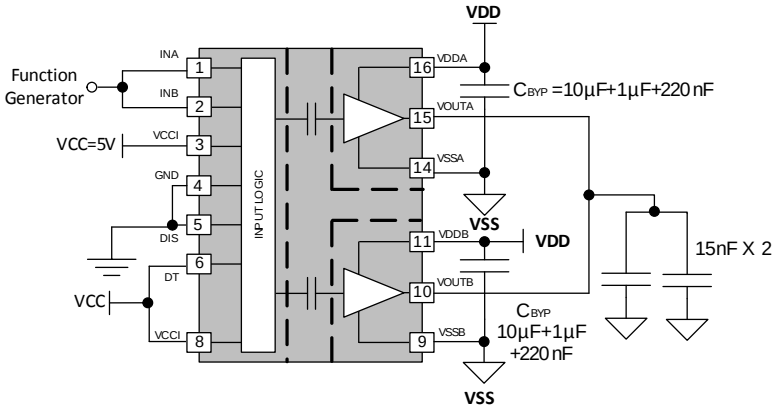

Figure 10. Setup B: UCC21520 Two Channel in Parallel Drives Two 15-nF Load

Figure 11 through Figure 13 show the total VDD (VDD = 12 V and 25 V) operating current consumption measurement with different switching frequencies at 25°C/-40°C/125°C ambient temperatures. And it can be seen that the current consumption differences between these two setups is negligible.

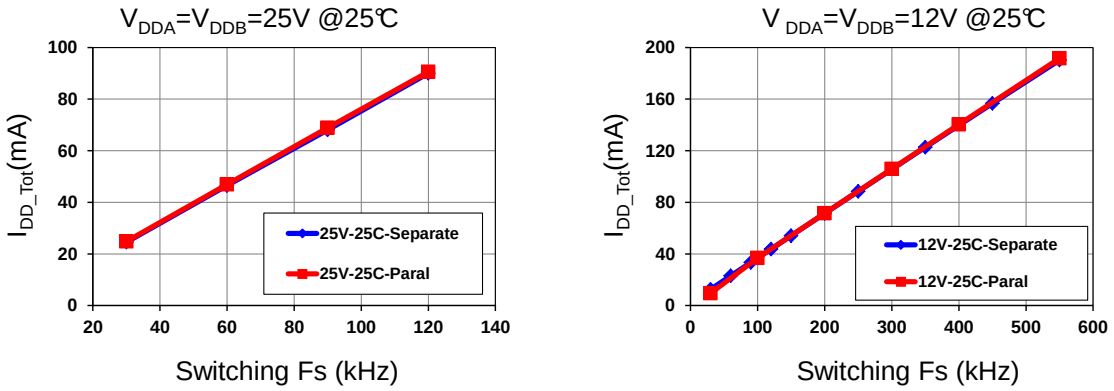

Figure 11. VDD Total Operating Current vs. F_S at 25°C

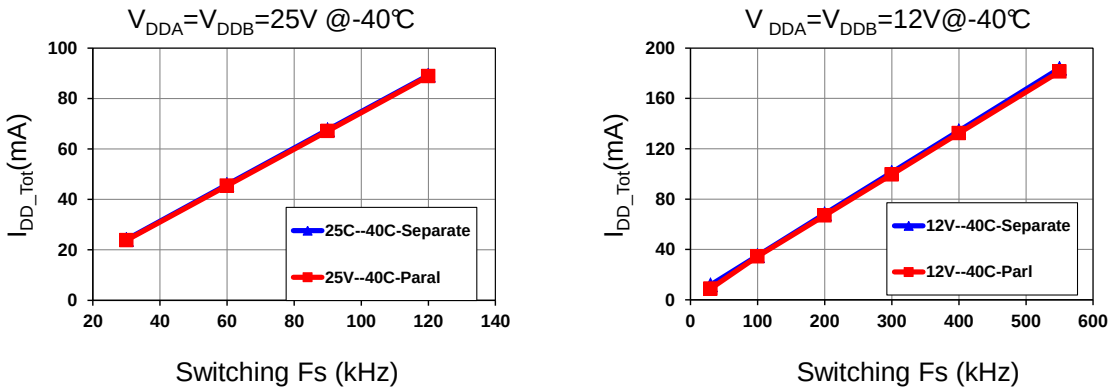

Figure 12. VDD Total Operating Current vs. F_S at –40°C

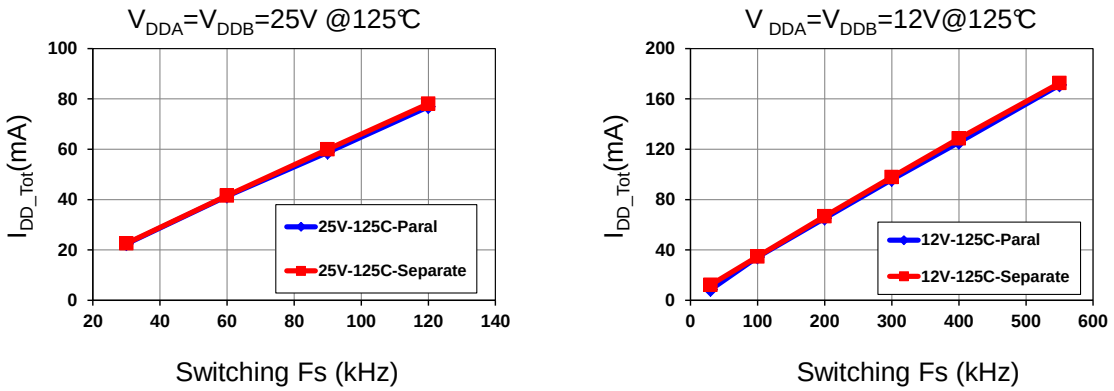

Figure 13. VDD Total Operating Current vs. F_S at 125°C

Figure 14 puts the current consumption data with tri-temperature performance in one graph with zoom-in on the vertical axis.

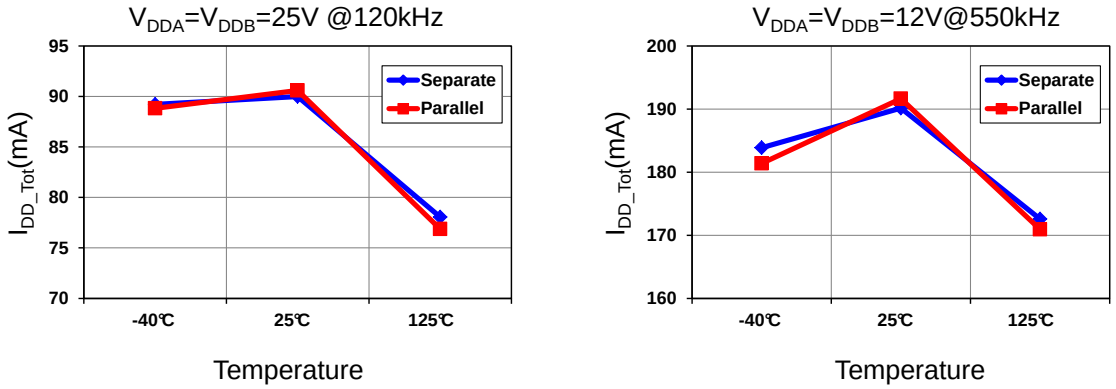

Figure 14. VDD Total Operating Current vs. Temperature at VDD = 12 V and 25 V

Importantly, the VDD total current consumption data is measured with the device under test (DUT) operating (switching) within only a short moment after the DUT, as well as junction temperature, soaks to the ambient temperature, and the UCC21520 is not running into thermal stable state at the given switching and load condition. The major purpose is to validate the driver device performance at given junction temperature, and the users should not try to run the test conditions for a long time, since it may damage the UCC21520 due to overheating. For UCC21520 safety-related performance, please refer to UCC21520 datasheet.

In summary, the UCC21520 shows very good performance with two output channels in parallel at all operating switching frequencies, VDD range and temperature corners. Due to the best-in-class propagation delay matching performance, the internal shoot-through caused extra loss is negligible. Figure 15 shows the UCC21520 driving 30 nF with parallel and separate output, and it can be seen that the output parallel can effectively increase the gate drive strength by 50%. The rising time is decreased to be 50 ns from 5 V to 20 V on the output, which is less than half when using only single channel.

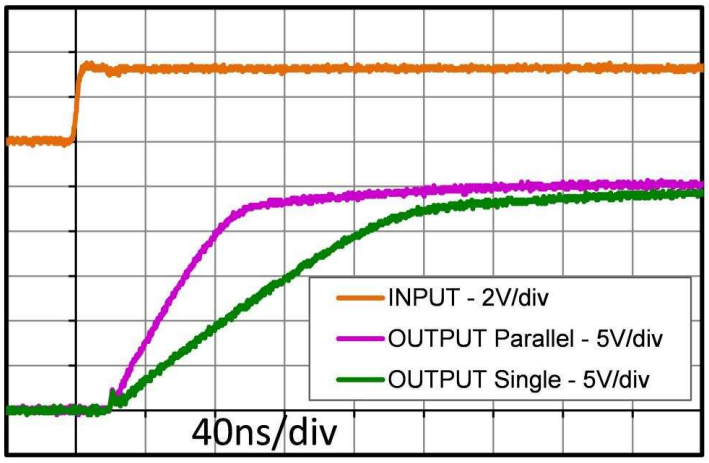

Figure 15. UCC21520 Single Channel Driving 30-nF Load Capacitance

5.2 Schematic and PCB Layout Recommendations when Paralleling Output Channels

To maintain the optimal performance of the UCC21520 with output channel in parallel, it is recommended to follow the following schematic and PCB layout design considerations,

1. Short the INA and INB as close to the device as possible to make sure there is little delay introduced between the two signal inputs.
2. Use the same bypassing capacitor for channel A and channel B respectively to minimize the timing imbalance introduced due to parasitic inductance.
3. Make sure the PCB layout are symmetrical between channel A output and channel B output, refer to Figure 16. More PCB layout information can be found in UCC21520 datasheet.

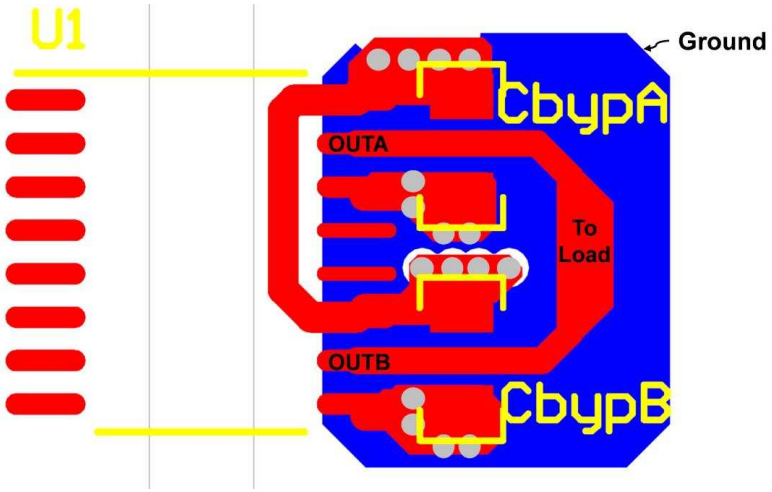

Figure 16. Layout Example for Paralleling UCC21520 Two Output Channels

4. If the external output resistor is used for system trade-offs, it is recommended to have two resistors with the same resistance value placed in output A and output B to further minimize the parasitic inductance introduced channel imbalance, refer to Figure 17.

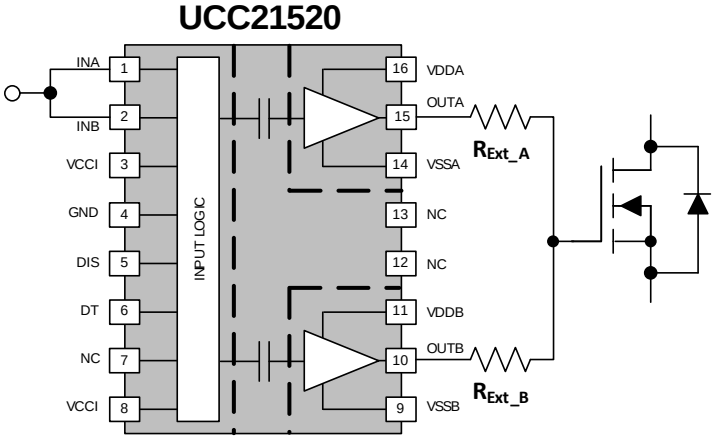

Figure 17. Paralleling UCC21520 Two Output Channels with External Resistor

6 UCC21520 Driving Different Power Topologies

The flexible, universal capability of the UCC21520 with up to 18-V VCCI and 25-V VDDA/VDDB allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver with MOSFETs, IGBTs or SiC MOSFETs. Here are some topology examples where the UCC21520 can fit very well. Synchronous buck or boost is shown in Figure 18 and Figure 19; full bridge isolated converter is shown in Figure 20; Motor drives application is shown in Figure 21.

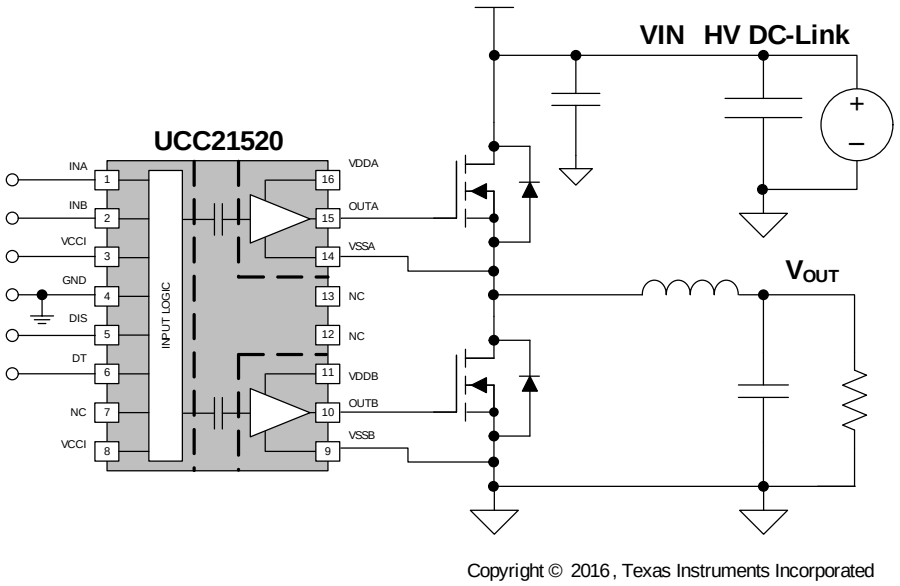

Figure 18. UCC21520 Used in Synchronous Buck

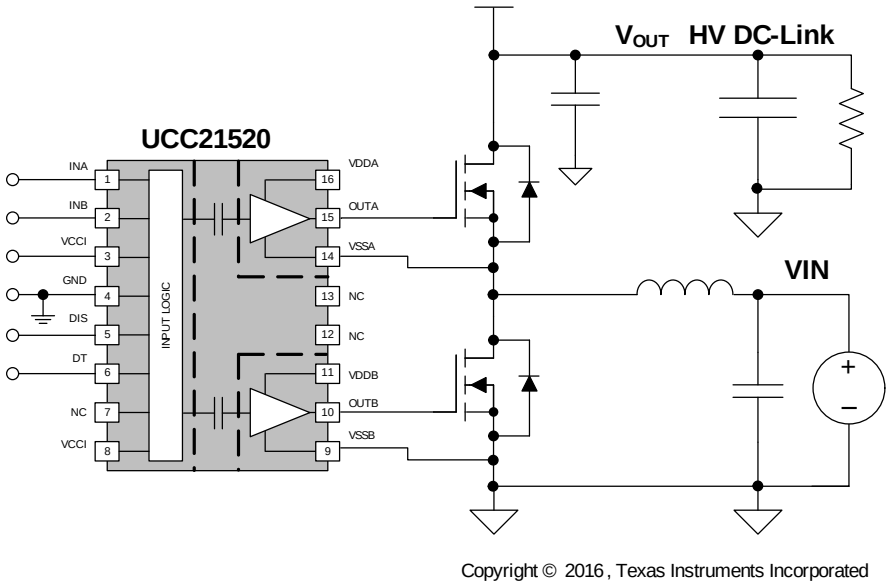

Figure 19. UCC21520 Used in Synchronous Boost

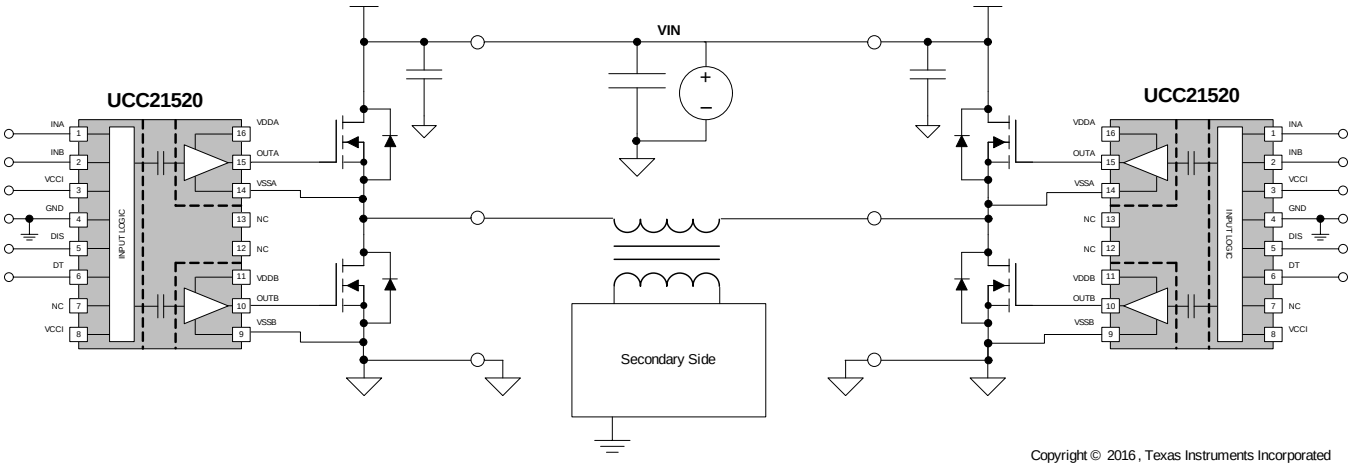

Figure 20. UCC21520 Used in Full-Bridge Isolated Converter

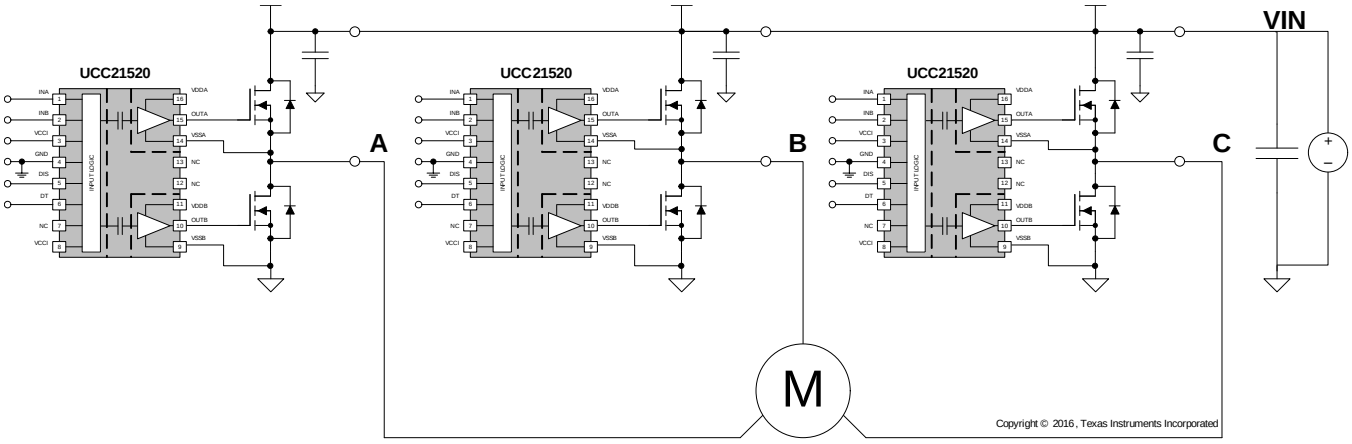

Figure 21. UCC21520 Used in Motor Drives

7 Summary

The UCC21520 is a dual-channel gate driver with reinforced isolation of 5.7 kV_{RMS} along with a common-mode transient immunity (CMTI) greater than 100 V/ns. This application report discussed the UCC21520's best-in-class propagation delay of 19 ns and the best channel-to-channel delay matching of less than 5 ns which enables high-switching frequency, high-power density and efficiency. Importantly, design considerations and benefits with the UCC21520's fast dynamic response and two output channels in parallel are addressed in detail with its wide application in a great variety of power electronics topologies.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2016) to A Revision	Page
• Changed text from "The rising time is increased..." to "The rising time is decreased..."	9

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