Application Note

How to Receive a Lower Output Voltage Than Reference Voltage

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ABSTRACT

In typical Buck circuit, the output voltage is higher than reference voltage. Currently, the reference voltage is about 0.6 V or 0.8 V. SoC has a trend which requires a lower and lower supply voltage, sometimes even lower than 0.6 V. This article introduces a step to receive an output voltage lower than reference voltage. The circuit uses adaptive voltage scaling (AVS) to receive a lower output voltage and dynamic adjust output voltage to meet SoC requirement. This article also introduces theory analysis and simulation of this AVS. An example of TPS563252 is given to demonstrate achieving this new method.

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1 Introduction

These days, processors have higher and higher requirements such as high-accuracy supply voltage and dynamic adjustable voltage for DC/DC power converter to maintain system operating in high performance. Therefore, how to design an excellent power supply with price advantage to meet the improvement of system performance will be the topic in the future.

When designing the power supply, the target output voltage is usually higher than the reference voltage. Normally the reference voltage is 0.6 V to 0.8 V for most of buck ICs. Sometimes the SoC needs a voltage lower than 0.6 V. How to receive a lower output voltage than reference voltage with current IC is a challenge.

Adaptive voltage scaling (AVS) is a closed-loop dynamic power minimization technique that adjusts the voltage supplied for main chip or device to meet the required power during operation. From power-saving benefits, reducing the self-heating of the main-chip while operating in high temperature environments creates a need for optimizing power supply solutions such as Figure 1-1. The application note *Adaptive (Dynamic) Voltage (Frequency) Scaling—Motivation and Implementation* detail introduces AVS process.

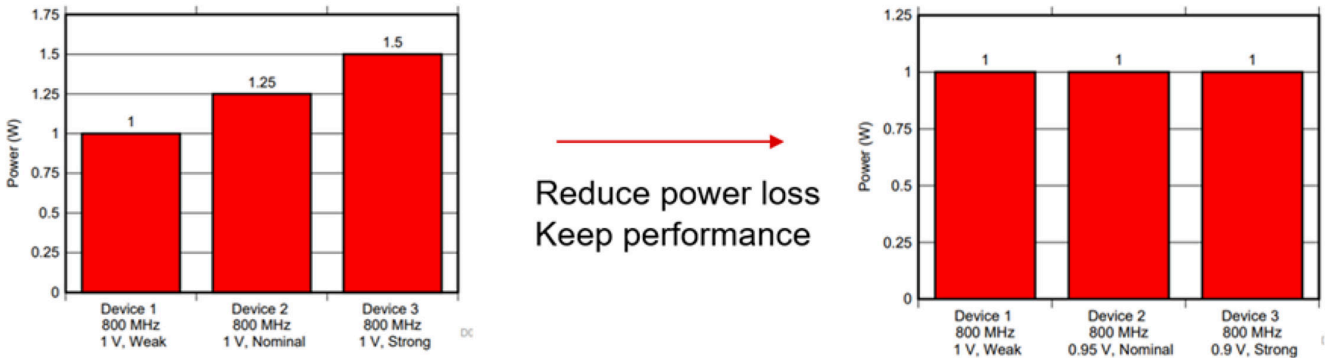

Figure 1-1. Example of AVS Normalization Effect Across Process Variation

AVS can be used to fix voltage dropping problem. A main chip claims a certain voltage for the supply, the voltage dropping issue is very common because of conduction loss on PCB. AVS process is also used to keep a certain voltage level for Main chip supply.

This article uses the AVS process to receive a lower output voltage than reference voltage. By adjusting the voltage of AVS, output voltage can be lower than reference voltage.

2 Lower Output Voltage Than Reference by AVS Control

There are external component and voltage sources at the feedback circuit of buck converter to realize AVS. In normal operating, the output voltage is programed by divider resister Rtop and Rbot. By AVS, the output voltage is also effected by the external resister and voltage source. The control circuit and output voltage calculation are shown in Figure 2-1 and Equation 1, Equation 2, and Equation 3.

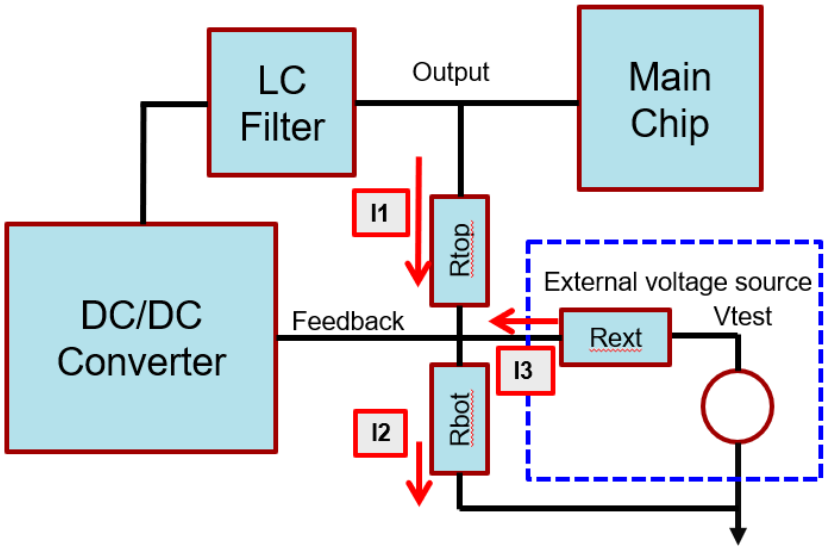

Figure 2-1. Adjustable Output Voltage With AVS

$$I2 = I3 + I1 \tag{1}$$

$$\frac{VFB}{R_{bot}} = \frac{Vtest - VFB}{R_{ext}} + \frac{Vout - VFB}{R_{top}} \tag{2}$$

$$Vout = R_{top} \times \left(\frac{VFB}{R_{bot}} - \frac{Vtest - VFB}{R_{ext}}\right) + VFB \tag{3}$$

Based on the previous equations, Equation 4, Equation 5, and Equation 6 show the relationship between Vout and Vtest.

$$Vout = R_{top} \times \frac{VFB}{R_{bot}} + VFB \ \left(if\ Vtest = VFB\right) \tag{4}$$

$$Vout = R_{top} \times \left(\frac{VFB}{R_{bot}} - \frac{Vtest - VFB}{R_{ext}}\right) + VFB \ < R_{top} \times \frac{VFB}{R_{bot}} + VFB \ \left(if\ Vtest > VFB\right) \tag{5}$$

$$Vout = R_{top} \times \left(\frac{VFB}{R_{bot}} - \frac{Vtest - VFB}{R_{ext}}\right) + VFB \ > R_{top} \times \frac{VFB}{R_{bot}} + VFB \ \left(if\ Vtest < VFB\right) \tag{6}$$

If a lower output voltage is required, Vtest voltage needs to be larger than reference voltage from Equation 4, Equation 5, and Equation 6. If Vtest is continuously rising until current I3 is over I2, the current I1 change direction through Rtop. The output voltage is lower than reference voltage. Figure 2-2 shows the current direction.

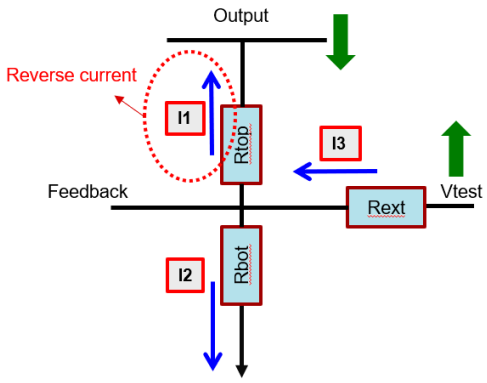

Figure 2-2. Lower Output Voltage With AVS

AVS process changes the FB circuit, and has no impact on power stage and internal loop parameters. The AVS process changes the function of Vfb to Vout. For lower output voltage, normally CFF (feed forward cap) is not suggested to add. The typical FB circuit is shown in Figure 2-3. The function of FB circuit is Equation 7.

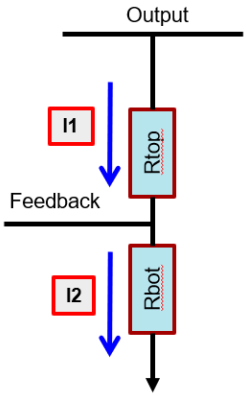

Figure 2-3. Typical FB Circuit

$$\frac{VFB}{Vout} = \frac{R_{bot}}{R_{bot} + R_{top}} \tag{7}$$

The FB circuit with AVS process is shown in Figure 2-4. Vtest is supposed to be 0 when doing AC analysis. The function of FB circuit with AVS process is shown in Equation 8 based on Equation 2.

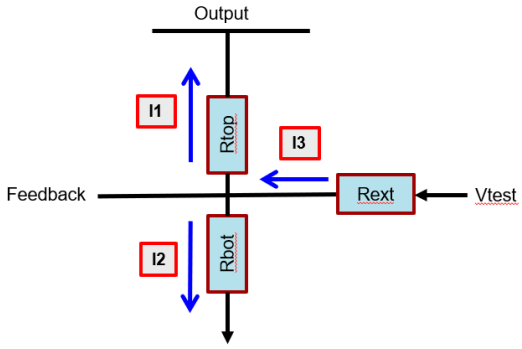

Figure 2-4. FB Circuit With AVS

$$\frac{VFB}{Vout} = \frac{R_{top}//R_{bot}//R_{ext}}{R_{top}} \quad (8)$$

Compare the FB transform function, the process of AVS has an impact on DC gain based on [*D-CAP2TM Frequency Response Model Based on Frequency Domain Analysis of Fixed On-Time with Bottom Detection Having Ripple Injection*]. The gain changing is shown in Equation 9 if using DC gain of typical FB circuit divide DC gain of FB circuit with AVS. If DC gain changes too much, there is an impact on bandwidth and phase margin. For Equation 9 to be equal to 1, AVS resister R_{ext} is set to be much larger than divider resister based on Equation 10.

$$\frac{\frac{VFB}{Vout}(typ)}{\frac{VFB}{Vout}(AVS)} = \frac{\frac{R_{bot}}{R_{bot}+R_{top}}}{\frac{R_{top}//R_{bot}//R_{ext}}{R_{top}}} = \frac{R_{top}//R_{bot}}{R_{top}//R_{bot}//R_{ext}} \quad (9)$$

$$\frac{\frac{VFB}{Vout}(typ)}{\frac{VFB}{Vout}(AVS)} = \frac{R_{top}//R_{bot}}{R_{top}//R_{bot}//R_{ext}} \approx \frac{R_{top}//R_{bot}}{R_{top}//R_{bot}} = 1 \quad (10)$$

3 Simulation Result with TPS563252

A circuit with TPS563252 Simplis model is built to do DC and AC analysis. TPS563252 is a part with high frequency to 1.2 MHz and high accuracy reference voltage. The reference voltage of TPS563252 is 0.6 V. If the SoC needs supply voltage to be 0.5 V to 0.7 V and typical supply voltage is 0.6 V. If Vtest voltage is 0, the output voltage is maximum value. Set bottom divider resister to be 10 kΩ, top divider resister 2 kΩ. Based on previous analysis, set AVS resister to be 47 kΩ which has small effect on loop at different output voltage. The voltage of AVS range is 1.07 V to 5.77 V based on Equation 3. Figure 3-1 shows TPS563252 schematic in Simplis.

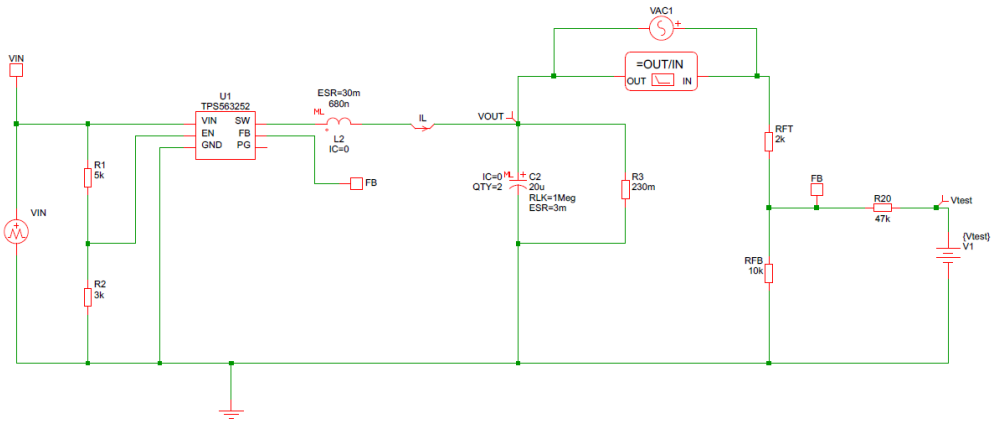

Figure 3-1. TPS563252 Schematic of Simplis

Figure 3-2 shows output voltage at Vtest voltage of 1.07 V, 3.1 V and 5.77 V. From steady state analysis, output voltage is stable and smooth. By this method, a desired output voltage, that is lower than reference voltage, is received.

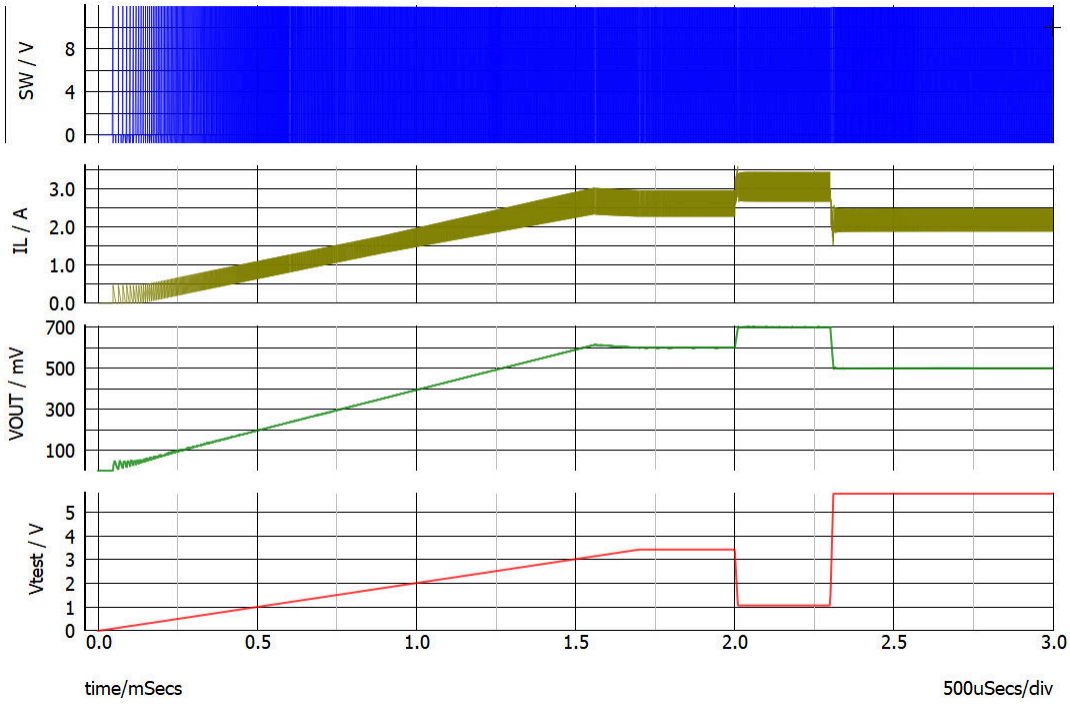

Figure 3-2. Output Voltage Waveform at Different Vtest Voltage

The bode plot as Figure 3-3 is received by running the AC simulation. The gain and phase curve are nearly the same. From phase margin, the bode plot is stable.

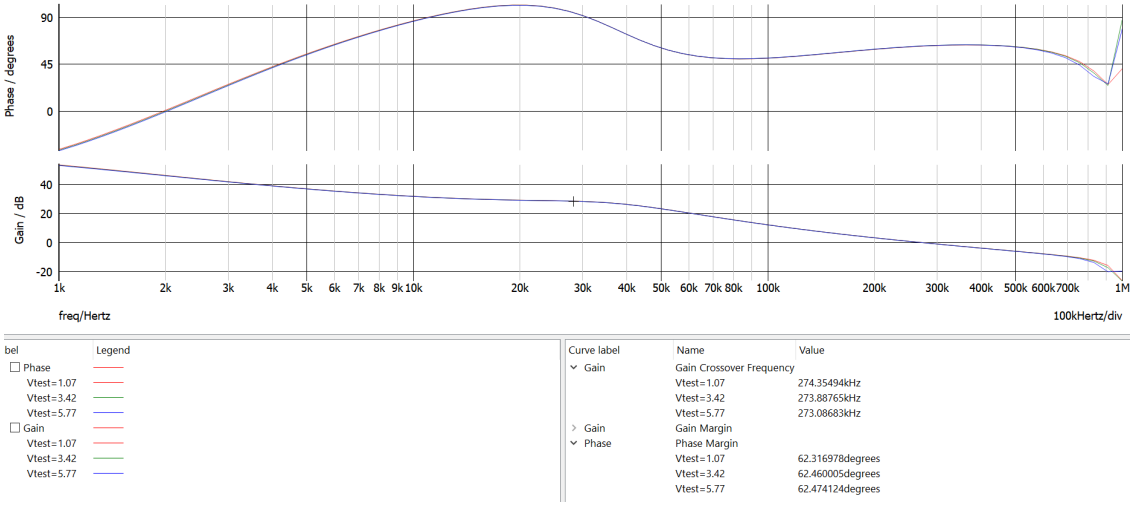

Figure 3-3. Bode Plot

4 Test Results with TPS563252

This AVS process is also tested on TPS563252EVM board. Please refer to the detailed EVM information in *PS563252 and TPS563257 Step-Down Converter Evaluation Module User's Guide*. Update the BOM to match the Simplis schematic.

Figure 4-1 to Figure 4-3 show the steady state status. From steady state waveform, output voltage and switching waveform are stable. Figure Figure 4-4 shows the dynamic change about output voltage with external test voltage. Channel 1 is Vtest voltage with dynamic change from 1.07 V to 5.77 V. Output voltage change by following Vtest voltage. From the waveform, output voltage smoothly change with external output voltage. Figure 4-5 to Figure 4-7 show the bode plot at difficult output voltage. Phase margin and gain margin show the stable. Figure 4-8 combine the three bode plot together to check if there is difference. From the waveform, the external test voltage have no effect on bode plot.

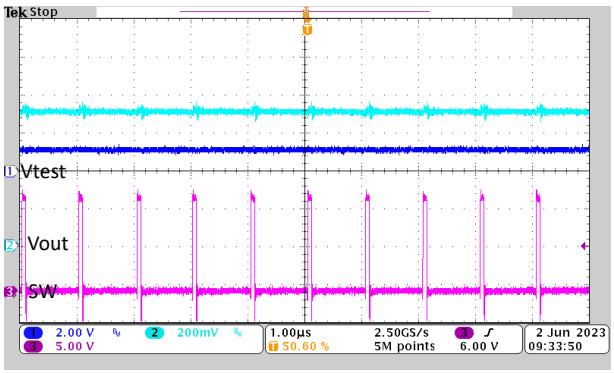

Figure 4-1. Steady State at 0.7 V Output Voltage and 1 V External Test Voltage

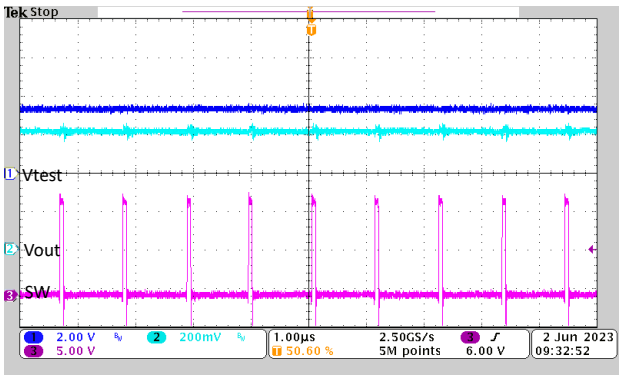

Figure 4-2. Steady State at 0.6 V Output Voltage and 3 V External Test Voltage

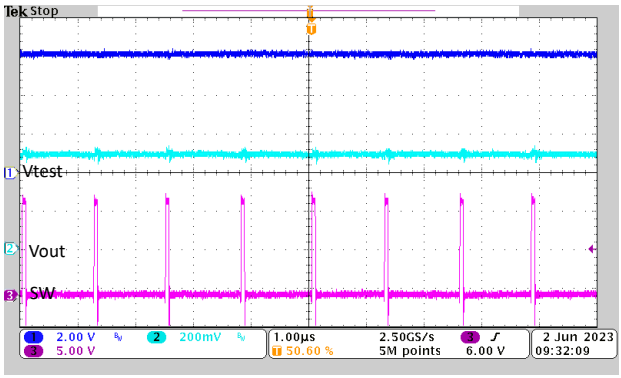

Figure 4-3. Steady State at 0.5 V Output Voltage and 6 V External Test Voltage

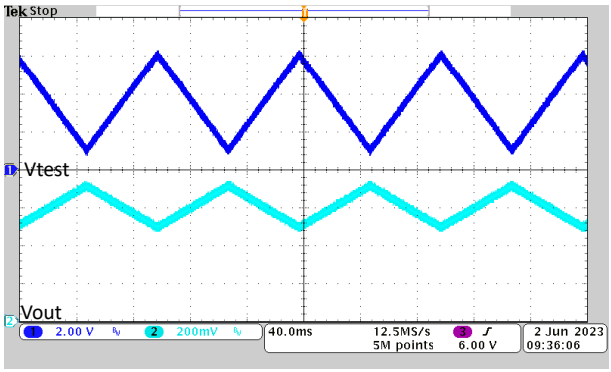

Figure 4-4. Dynamic Change for Output Voltage with External Test Voltage

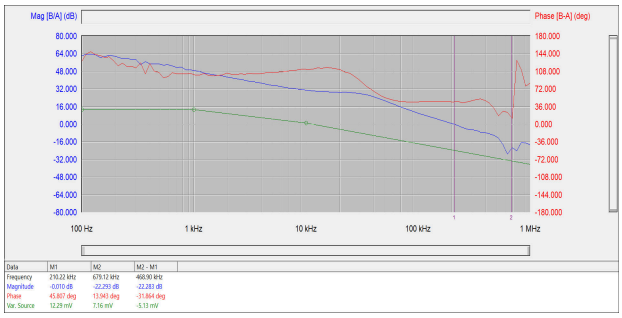

Figure 4-5. Bode Plot at 0.5 V Output Voltage

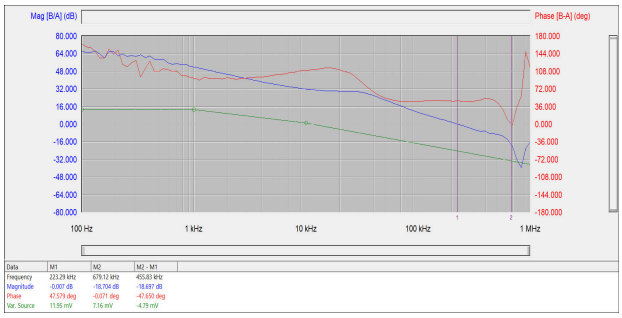

Figure 4-6. Bode Plot at 0.6 V Output Voltage

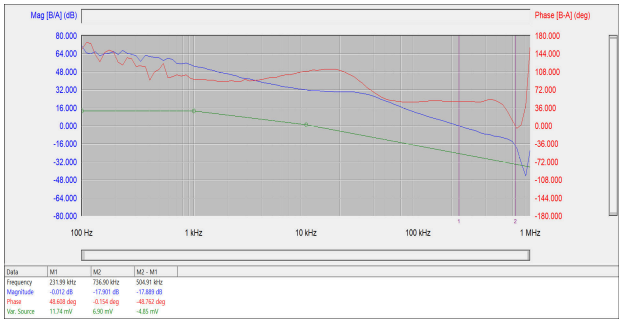

Figure 4-7. Bode Plot at 0.7 V Output Voltage

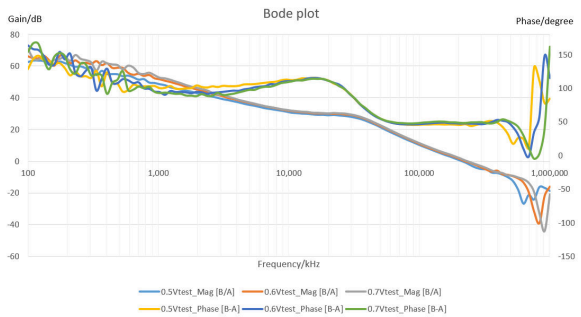

Figure 4-8. Bode Plot

5 Summary

In normal power design, frequent checks are done to see how low FB is when designing an extreme low output. This design is a limitation for power engineer. This article introduces how to receive a lower output voltage even than reference by AVS process. This article also introduces how to set the AVS resister and external forced voltage and analyze the stability. Finally, TPS563252 is used to build a schematic with AVS circuit to the flexibility by simulation and testing.

6 References

- Texas Instruments, *Adaptive (Dynamic) Voltage (Frequency) Scaling—Motivation and Implementation*, application note.
- Texas Instruments, *D-CAP2TM Frequency Response Model Based on Frequency Domain Analysis of Fixed On-Time with Bottom Detection Having Ripple Injection*, application note.
- Texas Instruments, *PS563252 and TPS563257 Step-Down Converter Evaluation Module User's Guide*

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