Application Brief

Increasing Further Data Rates Using High-Current Power Converters in Optical Modules

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Introduction

With the boom of AI servers spurring demand for higher data rates, OSFP (octal small-form-factor pluggable) modules rated up to 15 watts, and QSFP-DD (quad small-form-factor, pluggable, double-density) modules rated up to 12 watts, are widely manufactured. OSFP modules offers taller height requirements, up to 1.5mm on the bottom side of the PCB, compared to the 1.2mm height restriction previously offered with QSFP-DD. Systems designers are looking for step-down regulators that can accommodate both OSFP and QSFP-DD modules form factors. Small design size, thin height, and great efficiency are key design requirements.

Pushing the Limits of Thermal Designs

Data rates are continuously increasing, now going up to 1.6Tbps. Though the form factor of pluggable optical modules are defined to be inter-operable and compatible to different vendors (such as, QSFP-DD displayed in Figure 1). Being able to manage thermal dissipation in such a restricted environment enables systems designers to operate at higher speeds. In this server environment, airflow is very restricted. Therefore, heatsinks are built on top to help cool the pluggable modules. Figure 2 shows a QSFP-DD stacked cage with a heatsink built on top.

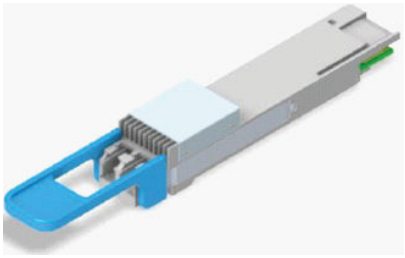

Figure 1. Single QSFP-DD Module

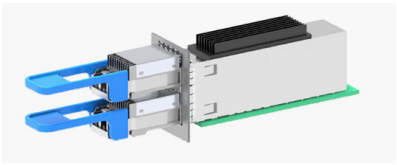

Figure 2. Two QSFP-DD Modules Shown in a Stacked Sage

The pluggable modules must still operate within the same power budget, defined by the form factor. To be able to fit a power design into different pluggable module form factors, and leverage reuse of designs to go quicker to market, systems designers tend to look at the performance of a buck converter with the thinnest height requirement and then adapt the inductor height depending on which thickness is allowed in the different form factors. Very few inductors exist that achieve small overall dimensions, have a low DCR, and high-saturation current.

The DSP core rail is the main driver for power consumption in a pluggable module. For example, current generation of DSPs usually requires a supply voltage between 0.65V down to 0.4V and consume up to 25A load current.

To power the core rail, choose a high-current power supply with an I^2C interface and small design size. The 25A TPS6287B25 enables designers to dynamically change the output voltage, with 1.25mV steps, using an I^2C interface, and comes in a small 3.05mm x 4.05mm QFN package to achieve high-power density.

Additionally, to ease the inductor selection process in meeting the height requirement and improving heat distribution in such a small 3D area, multiple TPS6287B25s can be paralleled. Paralleling buck converters helps reduce the temperature increase by splitting the hot spots.

For the design case throughout this document a 1.2mm height restriction is discussed. The XGL3512 is a very small inductor with 1.2mm height and is used as example.

Figure 3 shows a thermal picture of the TPS6287B25 at a 20A load. At this high load, the IC only has a moderate 30°C temperature rise, and the inductor has a smaller 20°C temperature rise.

Figure 3. Single TPS6287B25 Supplying 0.45V Rail at 20A DC With 3.3V V_{IN} at Room Temperature

In comparison, Figure 4 shows a thermal picture of two TPS6287B25s in a stack configuration at a 20A load. At this high load, the two ICs have only a moderate 15°C temperature rise and the inductor has a smaller 11°C temperature rise.

Figure 4. Two TPS6287B25s in Parallel Supplying 0.45V Rail at 20A DC With 3.3V V_{IN} at Room Temperature

Efficiency Optimization at High Loads

Moreover, splitting the current evenly enables the optimization of the defined power budget.

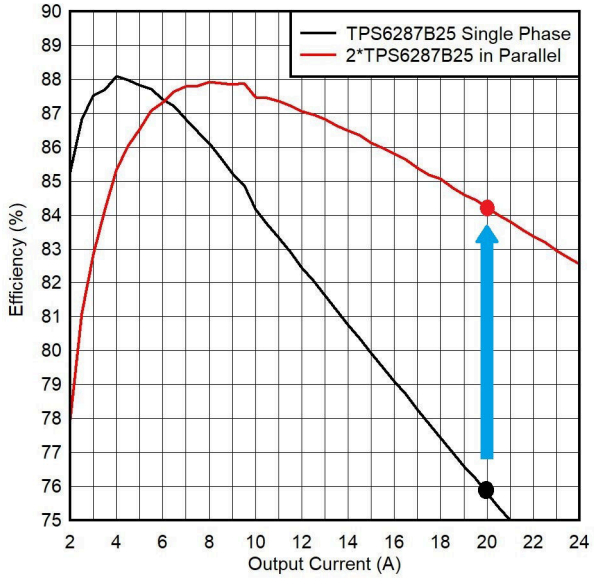

Figure 5. Efficiency Comparison Between Single TPS6287B25 and Two TPS6287B25 in Parallel

For instance, if a single TPS6287B25 converter is used at 20A DC for a 0.45V output, as shown in Figure 5, efficiency is 76% (2.84W Power Dissipation) for a single stacked TPS6287B25 configuration. For two TPS6287B25 placed in parallel, the efficiency goes up to 84% (1.69W Power Dissipation). In this case, stacking two TPS6287B25 results in a significant 1.15W savings. Stacking two TPS6287B25 also helps lower output ripple, since the ripple frequency is double from the out-of-phase operation.

Table 1. Summary Table with Selected Inductor

V_{IN}= 3.3V, V_{OUT}= 0.45V Room Temperature	Efficiency at 20A	Power Dissipation	Max Temperature
Single TPS6287B25	76%	2.84W	54.4°C
Dual TPS6287B25	84.2%	1.69W	39.8°C

Conclusion

In optical communications, power-budget optimization is a time consuming activity which requires to carefully pick power components. The TPS6287B25 family offers high-power density and great efficiency to run at high speed, even at high temperatures. To supply a high-power DSP, choose the right features, such as small R_{DSON} MOSFETS, stackability, and external synchronization capability, which are very important to simplify power and thermal constrained design.

References

1. Texas Instruments, *Operating TPS6287X-Q1 Devices in a Stacked Configuration*, application note.
2. Texas Instruments, *Understanding SOA Curves to Operate at High Output Currents and Temperature* application note.
3. Texas Instruments, *Enabling Higher Data Rates for Optical Modules With Small and Efficient Power and Data-Converter Solutions*, technical white paper.
4. *Semantic Scholar* optical module images (Figure 1 and Figure 2), *Optimizing QSFP-DD Systems to Achieve at Least 25 Watt Thermal Port Performance*, Cisco®, January 2021.

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