User's Guide
SLUU472–March 2011

Using the TPS59610EVM-675, A 5-V Vin 2010 Atom™ E6xx Tunnel Creek Power System

The TPS59610EVM-675 evaluation module (EVM) is a complete solution for the 2010 Atom™ E6xx Tunnel Creek Power System from a 5-V input bus. The EVM uses the TPS59610 for an Atom™ CPU and GPU core, TPS54620 for a 3.3-V system, TPS54326 for Topcliff IOH, TPS59116 for DDRII 1.8VDDQ and 0.9VTT, TPS54620 for CPU VTT 1.05 V, TPS74801 for CPU 1.5-V PLL and CPU C6 RAM 1.05 V. TPS59610EVM-675 also uses the 3-mm × 3-mm TI power block MOSFET (CSD86330Q3D) for high-power density and superior thermal performance.

Contents

1 Description 4
1.1 Typical Applications 4
1.2 Features 4
2 Atom™ Tunnel Creek Power System Block Diagram 5
3 Electrical Performance Specifications 6
4 Schematics 8
5 Test Setup 13
5.1 Test Equipment 13
5.2 Recommended Test Setup 13
6 Configuration 15
6.1 CPU and GPU Configuration 15
6.2 3.3-V System Configuration 17
6.3 1.05-V CPU VTT Configuration 17
6.4 1.8-VDDQ, 0.9-V VTT, and 0.9-V VTTREF Configuration 18
6.5 1.5-V CPU PLL Configuration 18
6.6 1.05-V CPU C6 RAM Configuration 18
6.7 1.2-V IOH Configuration 18
7 Test Procedure 19
7.1 Line/Load Regulation and Efficiency Measurement Procedure 19
7.2 Onboard Transient Response Measurement 19
7.3 Loop Gain/Phase Measurement 19
7.4 Equipment Shutdown 19
8 Performance Data and Typical Characteristic Curves 20
8.1 CPU 20
8.2 GPU 23
8.3 3.3-V System 27
8.4 1.05V CPU VTT 29
8.5 1.8VDDQ 32
8.6 1.2-V IOH 34
9 EVM Assembly Drawings and PCB layout 36
10 Bill of Materials 39

List of Figures

1 5-V Vin 2010 Atom™ Tunnel Creek Power System Block Diagram 5
2 TPS59610EVM-675 Schematic, Sheet 1 of 5 8

3 TPS59610EVM-675 Schematic, Sheet 2 of 5 9
4 TPS59610EVM-675 Schematic, Sheet 3 of 5 10
5 TPS59610EVM-675 Schematic, Sheet 4 of 5 11
6 TPS59610EVM-675 Schematic, Sheet 5 of 5 12
7 TPS59610EVM-675 Recommended Test Setup 13
8 CPU Efficiency 20
9 CPU Load Regulation 20
10 CPU Enable Turnon 20
11 CPU Enable Turnoff 20
12 CPU Switching Node 21
13 CPU Vcore Ripple 21
14 CPU Output Load Release Without Overshoot Reduction 21
15 CPU Output Load Release With Maximum Overshoot Reduction 21
16 CPU Transient From DCM to CCM 22
17 CPU Transient From CCM to DCM 22
18 CPU Bode Plot at 5 Vin, 1 V/3.5 A 22
19 CPU Top Board 23
20 CPU Bottom Board 23
21 GPU Efficiency 23
22 GPU Load Regulation 23
23 GPU Enable Turnon 24
24 GPU Enable Turnoff 24
25 GPU Switching Node 24
26 GPU Vcore Ripple 24
27 GPU Output Load Release Without Overshoot Reduction 25
28 GPU Output Load Release With Maximum Overshoot Reduction 25
29 GPU Transient From DCM to CCM 25
30 GPU Transient From CCM to DCM 25
31 GPU Bode Plot at 5 Vin, 1 V/3.5 A 26
32 GPU Top Board 26
33 GPU Bottom Board 26
34 3.3-V Efficiency 27
35 3.3-V Load Regulation 27
36 3.3-V Enable Turnon 27
37 3.3-V Enable Turnoff 27
38 3.3-V Switching Node 28
39 3.3-V Vo Ripple 28
40 3.3-V Bode Plot at 5-Vin, 3.3 V/5 A 28
41 3.3-V Top at 5 Vin, 3.3 V/5 A, No Airflow 29
42 1.05-V Efficiency 29
43 1.05-V Load Regulation 29
44 1.05-V Enable Turnon 30
45 1.05-V Enable Turnoff 30
46 1.05-V Switching Node 30
47 1.05-V Vo Ripple 30
48 1.05-V Bode Plot at 5 Vin, 1.05 V/5 A 31
49 1.05-V Top Board at 5 Vin, 1.05 V/5 A, No Airflow 31
50 1.8-V Efficiency 32
51 1.8-V Load Regulation 32

52 1.8-V Enable Turnon 32
53 1.8-V Enable Turnoff 32
54 1.8-V Switching Node 33
55 1.8-V Vo Ripple 33
56 1.8-V Top Board 33
57 1.8-V Bottom Board 33
58 1.2-V Efficiency 34
59 1.2-V load regulation 34
60 1.2-V Enable Turnon 34
61 1.2-V Enable Turnoff 34
62 1.2-V Switching Node 35
63 1.2-V Vo Ripple 35
64 1.2-V Top Board 35
65 TPS59610EVM-675 Top Layer Assembly Drawing, Top View 36
66 TPS59610EVM-675 Bottom Assembly Drawing, Bottom View 36
67 TPS59610EVM-675 Top Copper, Top View 37
68 TPS59610EVM-675 Internal Layer 2, Top View 37
69 TPS59610EVM-675 Internal Layer 3, Top View 37
70 TPS59610EVM-675 Bottom Layer, Bottom View 38

List of Tables

1 TPS59610EVM-675 Electrical Performance Specifications 6
2 Current-Limit Trip Selection 15
3 Frequency Selection 15
4 Overshoot Reduction Selection 15
5 CPU VID Bits Selection 16
6 GPU VID Bits Selection (See datasheet for detail) 16
7 C4 Exit Rate Selection 16
8 Overvoltage Protection Selection 16
9 Onboard Dynamic Load Selection 17
10 Enable Selection 17
11 3.3-V Enable Selection 17
12 1.05-V Enable Selection 17
13 J303(S3), J305(S5) Enable selection 18
14 1.5-V Enable Selection 18
15 1.05-V CPU C6 RAM Enable Selection 18
16 1.2-V Enable Selection 18
17 Bill of Materials 39

1 Description

The TPS59610EVM-675 is designed to use a regulated 5-V (4.5-V to 5.5-V) bus to produce nine regulated outputs for an Atom™ E6xx Tunnel Creek Power System. The TPS59610EVM-675 is specially designed to demonstrate the TPS59610 Atom™ E6xx CPU and GPU Vcore regulators, while providing a number of test points to evaluate their static and dynamic performance.

1.1 Typical Applications

1. 5-V Vin Atom™ E6xx Tunnel Creek Power System for Embedded Computing Platforms

1.2 Features

The TPS59610EVM-675 features:

- Complete solution for 5-V Vin Atom™ Tunnel Creek Power System
- Selectable 200/300/400/500-kHz switching frequency for CPU and GPU power
- Selectable current limit for CPU and GPU power
- Selectable output overshoot reduction (OSR™) for CPU and GPU power
- Switches or jumpers for each output enable
- Onboard dynamic load for CPU, GPU Vcore output
- High efficiency and high density by using TI power block MOSFET
- Convenient test points for probing critical waveforms
- Four-layer PCB with 2-oz copper on the outside layers

2 Atom™ Tunnel Creek Power System Block Diagram

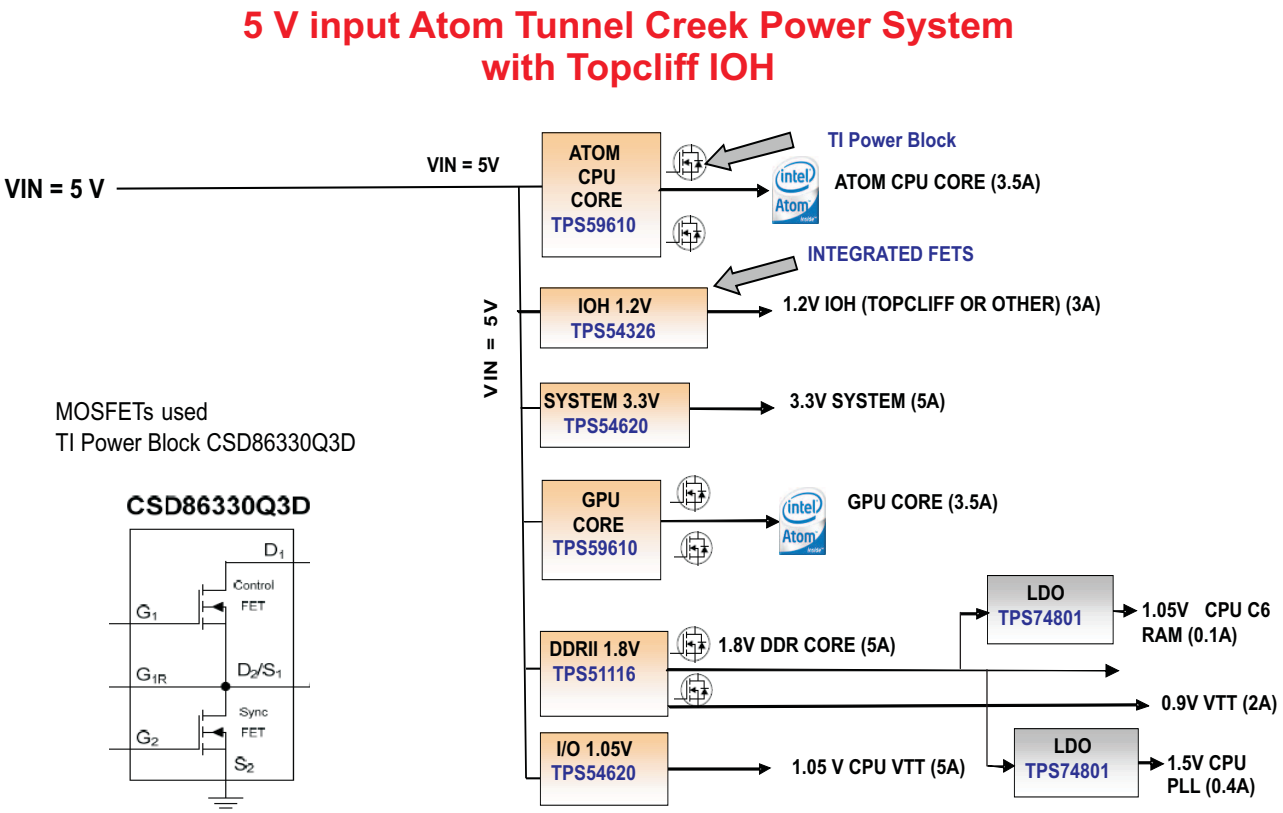


Figure 1. 5-V Vin 2010 Atom™ Tunnel Creek Power System Block Diagram

3 Electrical Performance Specifications

Table 1. TPS59610EVM-675 Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
VIN input voltage range*	VIN	4.5	5	5.5	V
Maximum input current	VIN = 5 V, all full load		10		A
No load input current	VIN = 5 V, all no load		45		mA
OUTPUT CHARACTERISTICS					
CPU (TPS59610)					
Output voltage Vcore	VID0 = VID1 = VID2 = VID4 = VID6 = 0, VID3 = VID5 = 1		1		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation(droop) load line		–5.7		M
Output voltage ripple	VIN = 5 V, 1 V/3.5 A at 300 KHz		30		mVpp
Output load current		0		3.5	A
Output over current			6.8		A
Switching frequency	Selectable	200	300	500	kHz
Full load efficiency	VIN = 5 V, 1 V/3.5 A at 300 kHz		87.47%		
GPU (TPS59610)					
Output voltage Vcore	VID0 = VID2 = VID4 = VID5 = 0, VID1 = VID3 = 1, VID6 = 5 V		1.00		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation(droop) load line		–5.7		M
Output voltage ripple	VIN = 5 V, 1 V/3.5 A at 300 KHz		30		mVpp
Output load current		0		3.5	A
Output over current			6.8		A
Switching frequency	Selectable	200	300	500	kHz
Full load efficiency	VIN = 5 V, 1 V/3.5 A at 300 kHz		87.78%		
3.3-V SYSTEM (TPS54620)					
Output voltage			3.3		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		0.1%		
Output voltage ripple	VIN = 5 V, 3.3 V/5 A		34		mVpp
Output load current		0		5	A
Output over current			10		A
Switching frequency	Selectable		480		kHz
Full load efficiency	VIN = 5 V, 3.3 V/5 A		92.08%		
DDR 1.8VDDQ (TPS59116)					
Output voltage			1.8		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		0.3%		
Output voltage ripple	VIN = 5 V, 1.8 V/5 A		30		mVpp
Output load current		0		5	A
Output over current			10		A
Switching frequency	Selectable		400		kHz
Full load efficiency	VIN = 5 V, 1.8 V/5 A		91.63%		
1.2V IOH(TPS54326)					
Output voltage			1.2		V

Table 1. TPS59610EVM-675 Electrical Performance Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1.5%		
Output voltage ripple	VIN = 5 V, 1.2 V/3 A		20		mVpp
Output load current		0		3	A
Output over current			4.1		A
Switching frequency			700		kHz
Full load efficiency	5 Vin, 1.2 V/3 A		74.75%		
1.5-V CPU PLL(TPS74801)					
Output voltage			1.5		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1%		
Output voltage ripple	VIN = 1.8 V,1.5 V/0.4 A		10		mVpp
Output load current		0		0.4	A
Output over current			2		A
Switching frequency			N/A		kHz
Full-load efficiency			N/A%		
0.9-V VTT(TPS59116)					
Output voltage			0.9		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		±40		mV
Output voltage ripple	VIN = 1.8 V, 0.9 VTT, Io = 2 A		10		mVpp
Output load current		0		2	A
Output over current			3		A
Switching frequency			N/A		kHz
Full-load efficiency			N/A%		
1.05-V CPU C6 RAM (TPS74801)					
Output voltage			1.05		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1%		
Output voltage ripple	VIN = 1.8 V, 1.05 V/0.1 A		10		mVpp
Output load current		0		0.1	A
Output over current			2		A
Switching frequency			N/A		kHz
Full-load efficiency			N/A%		
Operating temperature			25		°C

Note: Jumpers set to default locations, see section 6 of this user's guide

4 Schematics

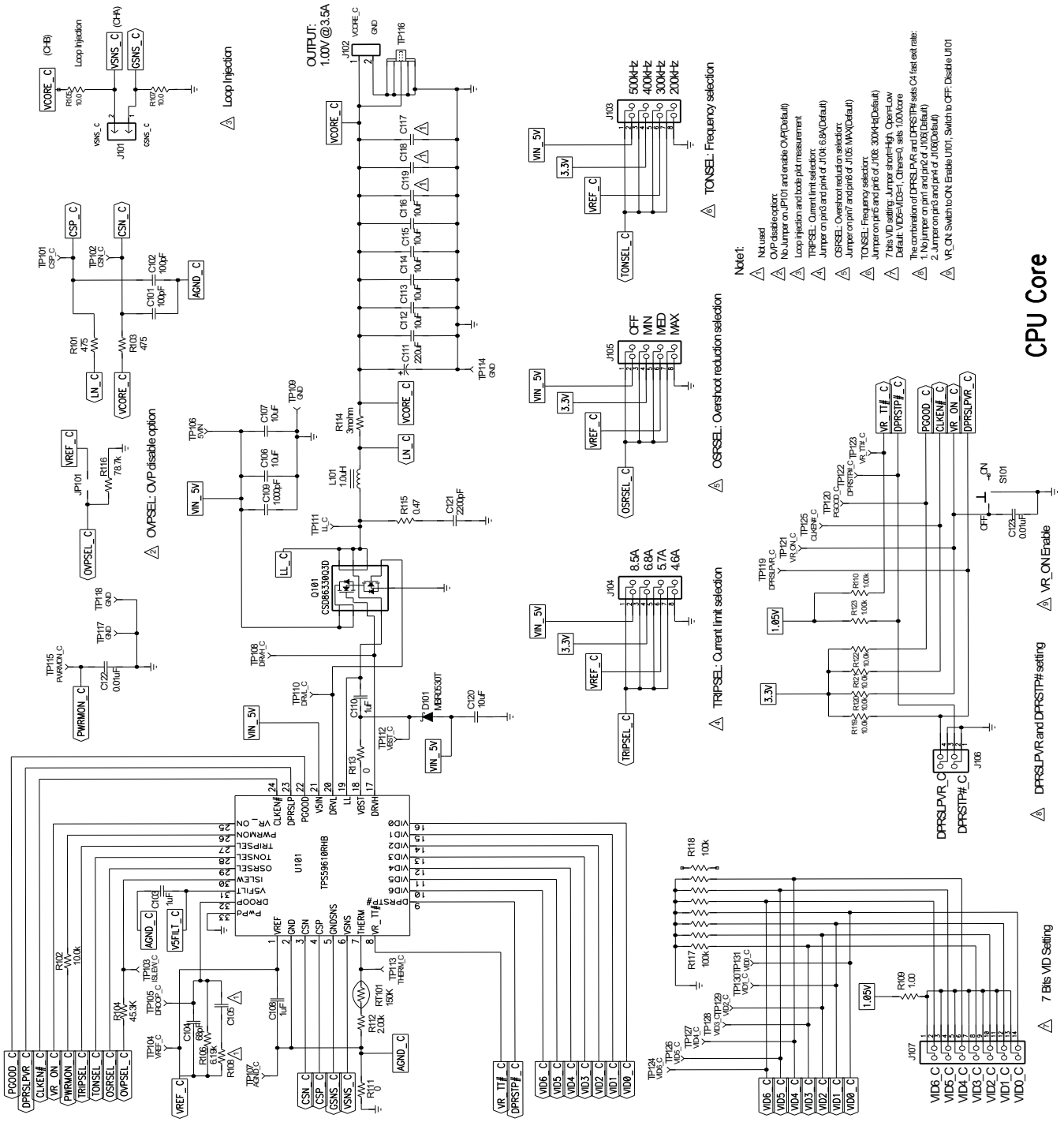


Figure 2. TPS59610EVM-675 Schematic, Sheet 1 of 5

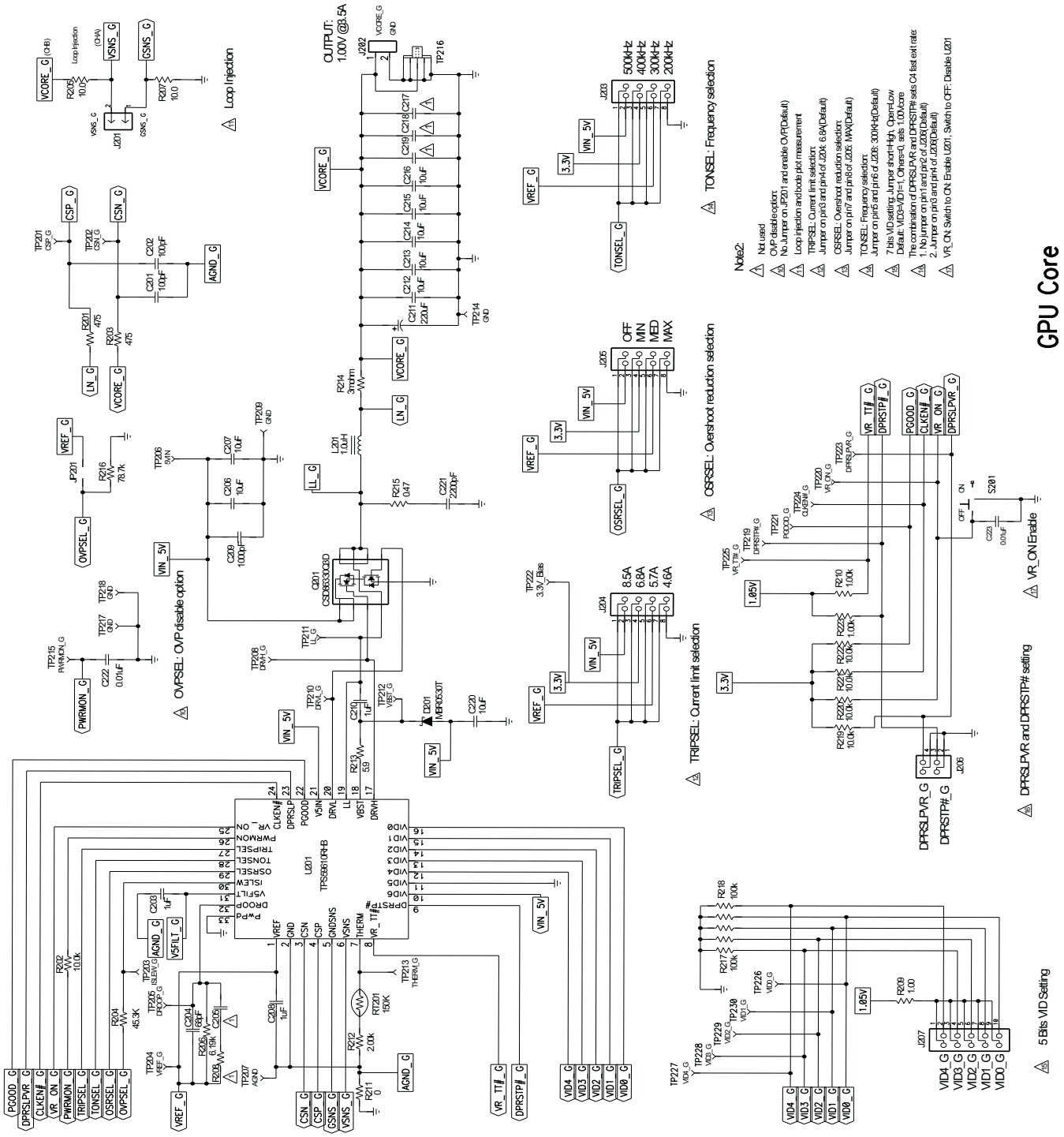


Figure 3. TPS59610EVM-675 Schematic, Sheet 2 of 5

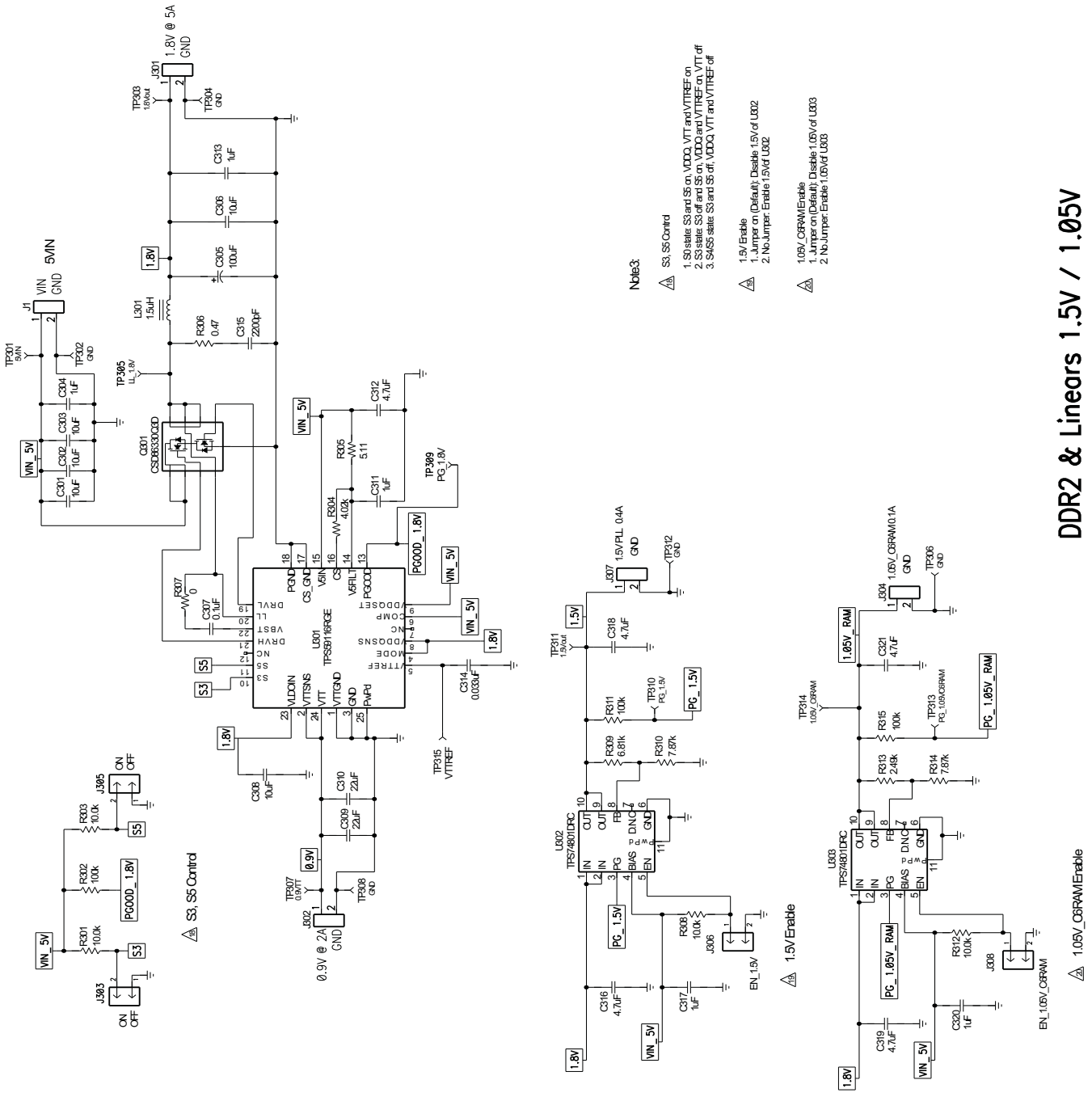


Figure 4. TPS59610EVM-675 Schematic, Sheet 3 of 5

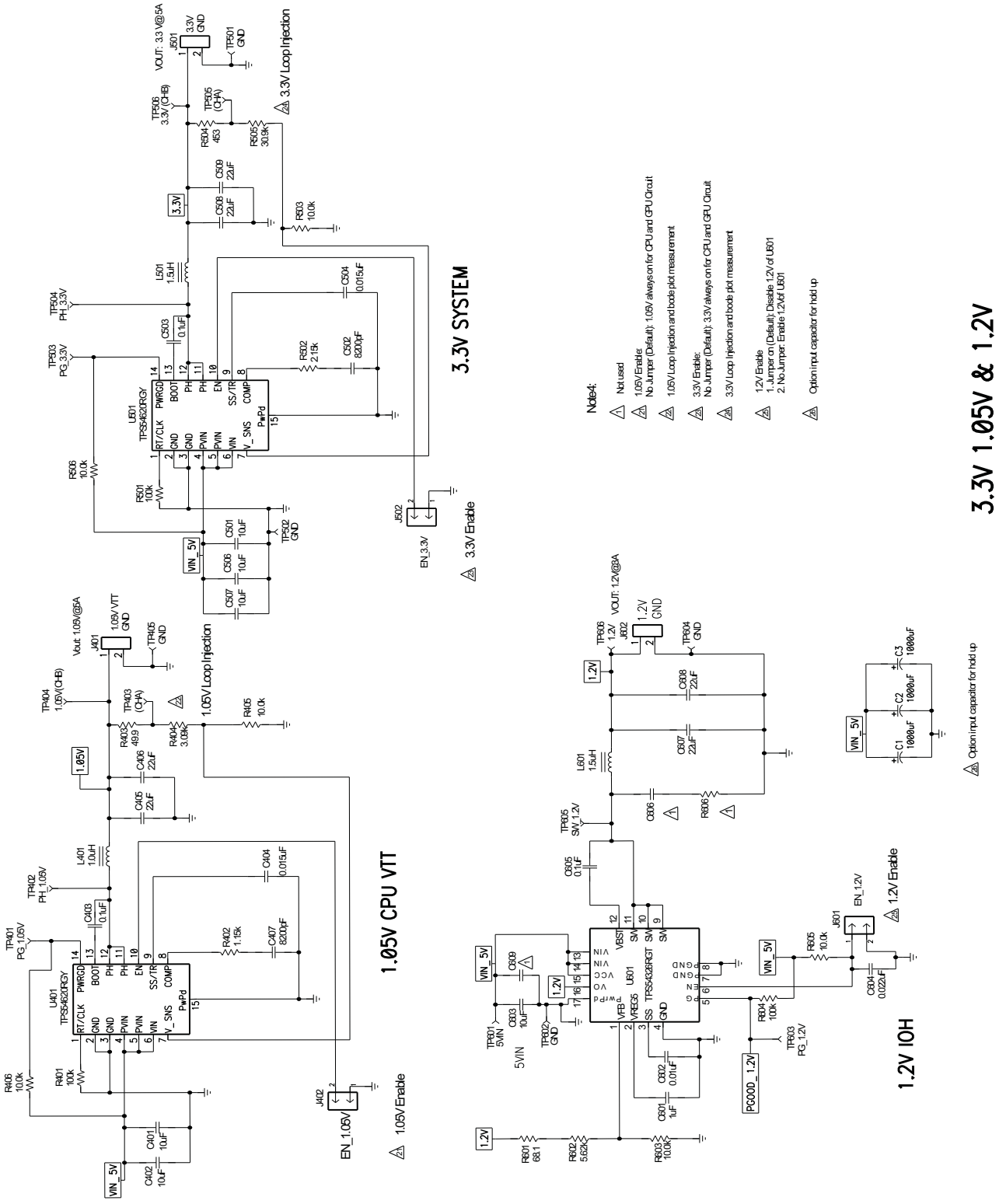


Figure 5. TPS59610EVM-675 Schematic, Sheet 4 of 5

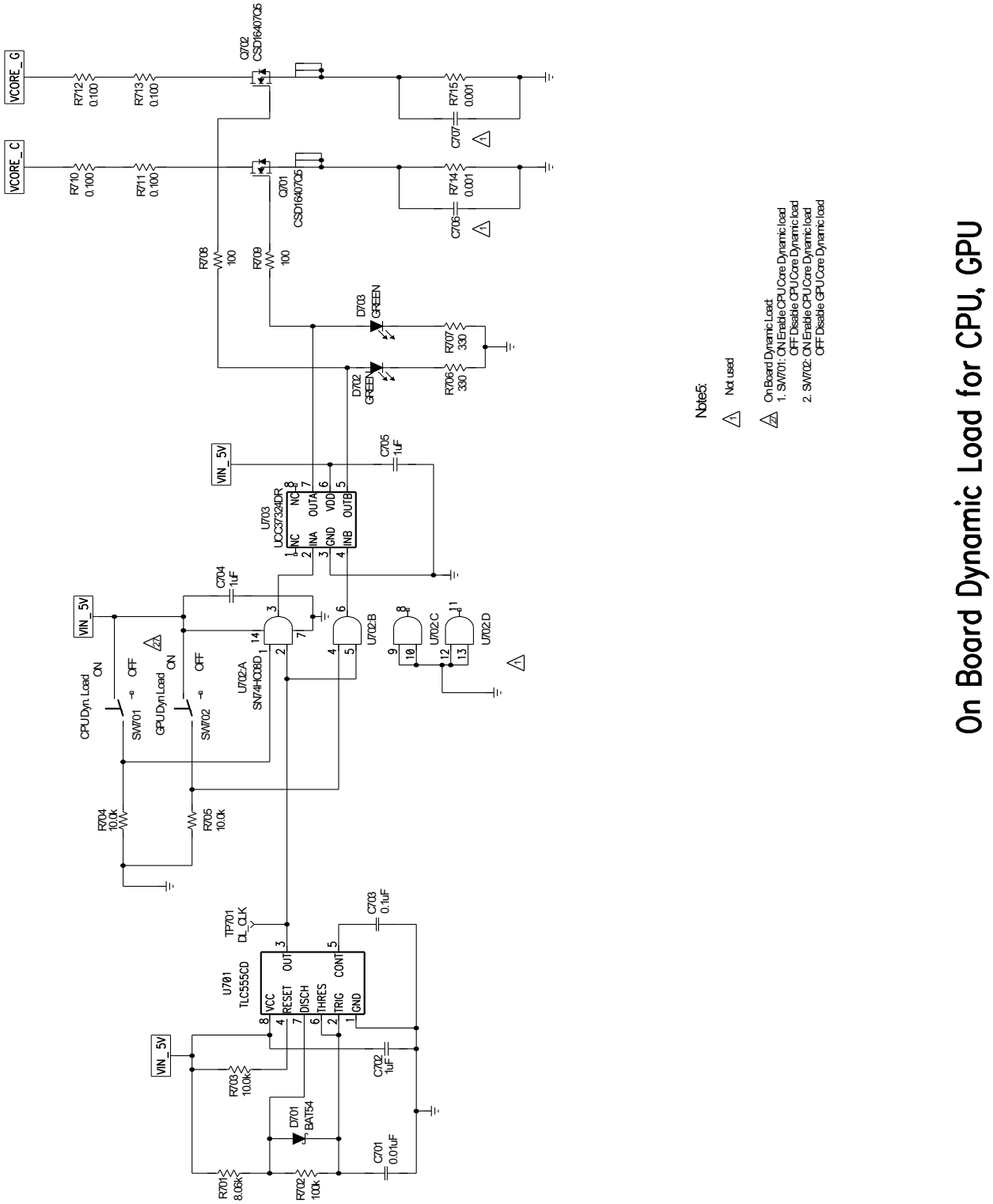


Figure 6. TPS59610EVM-675 Schematic, Sheet 5 of 5

5 Test Setup

5.1 Test Equipment

Voltage Source VIN: The input voltage source VIN must be a 0-V to 5.5-V variable dc source capable of supplying 10 Adc. Connect VIN to J1 as shown in Figure 7.

Multimeters:
V1: Vin at TP301 (5VIN) and TP302 (GND)
V2: Vout at each output test point. For example: CPU at J101
A1: Vin input current

Output Load: The output load must be an electronic constant resistance mode load capable of 0 Adc to 10 Adc.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope must be set for 1-M impedance, 20-MHz bandwidth, ac coupling, 2-µs/division horizontal resolution, 50-mV/division vertical resolution. Test points on each output can be used to measure the output ripple voltage. Do not use a leaded ground connection as this may induce additional noise due to the large ground loop.

Recommended Wire Gauge:

1. VIN to J1 (5-V input):
   The recommended wire size is AWG 14 per input connection, with the total length of wire less than 4 feet (2-foot input, 2-foot return).
2. Each outputs to LOAD.
   The minimum recommended wire size is AWG 16, with the total length of wire less than 4 feet (2-foot output, 2-foot return)

5.2 Recommended Test Setup

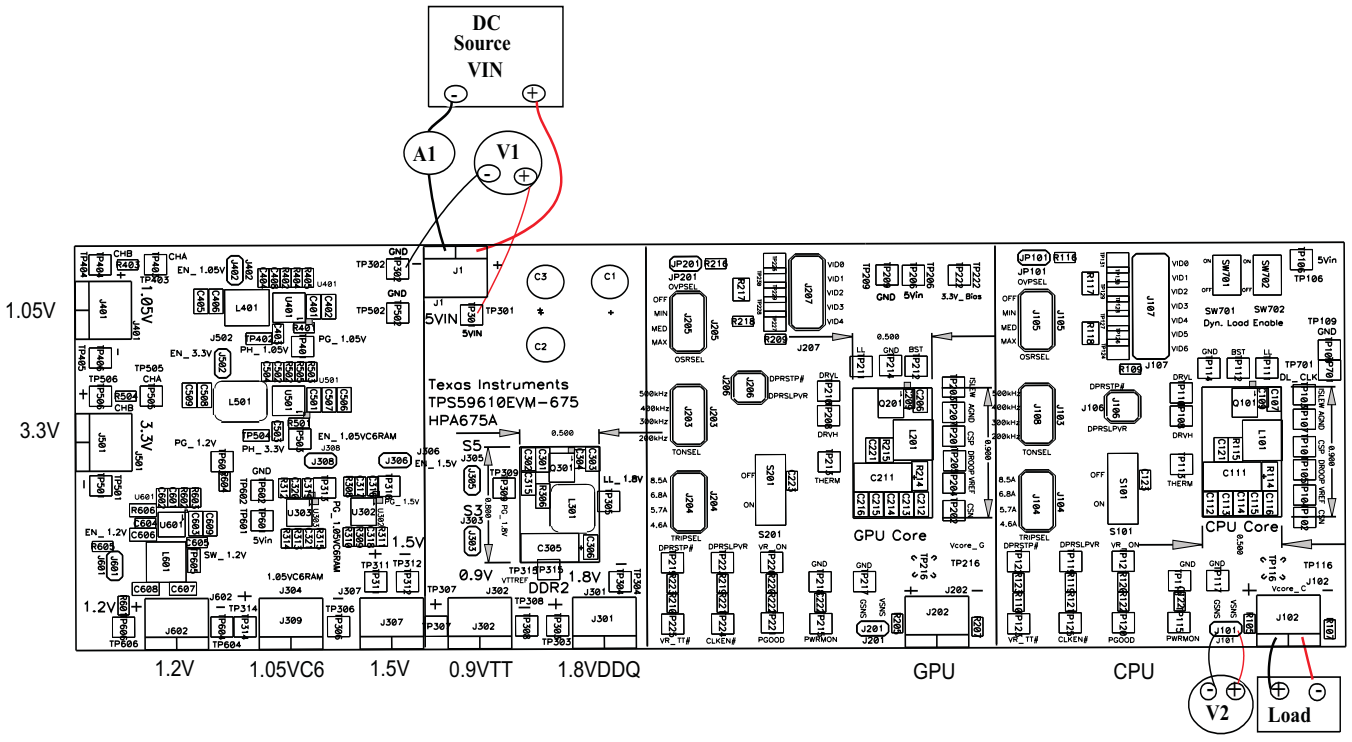


Figure 7. TPS59610EVM-675 Recommended Test Setup

Figure 7 is the recommended test setup to evaluate the TPS59610EVM-675. Working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before handling the EVM.

Input Connections:

1. Prior to connecting the dc input source VIN, it is advisable to limit the source current from VIN to 10 A maximum. Ensure that VIN is initially set to 0 V and connected as shown in Figure 7.
2. Connect a voltmeter V1 at TP301(5VIN) and TP302(GND) to measure VIN input voltage.
3. Connect a current meter A1 between VIN dc source and J1.

Output Connections (For example, CPU testing)

1. Connect the load to J102, and set the load to constant resistance mode to sink 0 Adc before VIN is applied.
2. Connect a voltmeter V2 at J101 to measure CPU 1-Vcore voltage as shown in Figure 7.

6 Configuration

All jumper selections must be made prior to applying power to the EVM. Users can configure this EVM per the following configurations.

6.1 CPU and GPU Configuration

6.1.1 Current-Limit Trip Selection (J104 for CPU and J204 for GPU)

The current limit trip can be set by J104 and J204 TRIPSEL.

Default setting: 6.8 A.

Table 2. Current-Limit Trip Selection

Jumper set to	TRIPSEL	OCP Limit Typ. (A)
Top (1-2 pin shorted)	5VFILT	8.5
Second **(3-4 pin shorted)**	**3.3VBIAS**	**6.8**
Third (5-6 pin shorted)	VREF	5.7
Bottom (7-8 pin shorted)	GND	4.6

6.1.2 Frequency Selection (J103 for CPU and J203 for GPU)

The operating frequency can be set by J103 and J203 TONSEL.

Default setting: 300 kHz.

Table 3. Frequency Selection

Jumper set to	TONSEL	Frequency (kHz)
Top (1-2 pin shorted)	5VFILT	500
Second (3-4 pin shorted)	3.3VBIAS	400
Third (5-6 pin shorted)	**VREF**	**300**
Bottom (7-8 pin shorted)	GND	200

6.1.3 Overshoot Reduction Selection (J105 for CPU and J205 for GPU)

The overshoot reduction can be set by J105 and J205 OSRSEL.

Default setting: Max.

Table 4. Overshoot Reduction Selection

Jumper set to	OSR	Overshoot Voltage Reduction
Top (1-2 pin shorted)	5VFILT	OFF
Second (3-4 pin shorted)	3.3VBIAS	Minimum
Third (5-6 pin shorted)	VREF	Medium
Bottom (7-8 pin shorted)	**GND**	**Maximum**

6.1.4 VID Bits Selection

The CPU Vcore voltage can be set by J107 (7-bit CPU VID).

Default setting: 0101000 for 1.000V
Jumper = 1
No Jumper = 0

Table 5. CPU VID Bits Selection

7-Bit VID Table (1 = 1.05 V, 0 = GND)							
VID6	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**Vcore (V)**
0	0	0	0	0	0	0	1.500
0	0	1	1	0	0	0	1.200
0	**1**	**0**	**1**	**0**	**0**	**0**	**1.000**
0	1	1	1	0	0	0	0.800
1	0	0	1	0	0	0	0.600
1	0	1	1	0	0	0	0.400
1	1	0	0	0	0	0	0.300

See data sheet for details.

The GPU Vcore voltage can be set by J207 (5- Bit GPU VID).

Default setting: 01010 for 1.000V

Table 6. GPU VID Bits Selection (See datasheet for detail)

5-Bit VID Table(1=1.05V, 0=GND)					
VID4	**VID3**	**VID2**	**VID1**	**VID0**	**Vcore(V)**
0	0	0	0	0	1.250
0	0	1	1	0	1.100
0	**1**	**0**	**1**	**0**	**1.000**
1	0	0	1	0	0.800
1	1	0	1	0	0.600
1	1	1	1	1	0.400

6.1.5 Deep Sleep Mode Selection (DPRSLPVR)

The combination of DPRSTP# and DPRSLPVR sets C4 exit rate. These can be set by J106 for CPU and J206 for GPU.

Default setting: Jumper on DPRSLPVR and no Jumper on DPRSTP# of J106 and J206

Table 7. C4 Exit Rate Selection

Jumper set to	C4 exit rate
Jumper on DPRSLPVR No jumper on DPRSTP#	**C4 exit fast**
No jumper on DPRSLPVR No jumper on DPRSTP#	C4 exit slow

6.1.6 Overvoltage Protection Selection (JP101 for CPU and JP201 for GPU)

The overvoltage protection selection can be set by JP101 and JP201, OVPSEL.

Default setting: No jumper shorts on JP101 and JP201 to enable OVP

Table 8. Overvoltage Protection Selection

Jumper set to	Selection
No jumper	**OVP enabled**
Jumper shorted	OVP disabled

6.1.7 Onboard Dynamic Load Selection (SW701 for CPU and SW702 for GPU)

The onboard dynamic load can be set by SW701 and SW702.

Default setting: Push SW701 and SW702 to OFF position to disable the onboard dynamic load.

Table 9. Onboard Dynamic Load Selection

Switch set to	Dynamic Load Selection
Push SW701 to ON position	Enable 5A onboard dynamic load at CPU
Push SW701 to OFF position	**Disable 5A onboard dynamic load at CPU**
Push SW702 to ON position	Enable 5A onboard dynamic load at GPU
Push SW702 to OFF position	**Disable 5A onboard dynamic load at GPU**

6.1.8 Enable Selection (S101 for CPU and S201 for GPU)

The Vcore of CPU and GPU can be enabled and disabled by S101 and S201.

Default setting: Push S101 and S201 to OFF position to disable both CPU and GPU.

Table 10. Enable Selection

Switch set to	Dynamic Load Selection
Push S101 to ON position	Enable CPU Vcore
Push S101 to OFF position	**Disable CPU Vcore**
Push S201 to ON position	Enable GPU Vcore
Push S201 to OFF position	**Disable GPU Vcore**

6.2 3.3-V System Configuration

6.2.1 3.3-V Enable Selection J502

3.3-V Enable can be set by J502.

Default setting: No Jumper shorts on J502 to enable 3.3 V

Note: 3.3 V needs to be always enabled for CPU and GPU circuit.

Table 11. 3.3-V Enable Selection

Jumper set to	Selection
Jumper on J502	3.3 V Disabled
No jumper on J502	**3.3 V Enabled**

6.3 1.05-V CPU VTT Configuration

6.3.1 1.05-V Enable Selection J402

1.05-V Enable can be set by J402.

Default setting: No jumper shorts on J402 to enable 1.05 V

Note: 1.05 V needs to be always enabled for CPU and GPU circuit.

Table 12. 1.05-V Enable Selection

Jumper set to	Selection
Jumper on J402	1.05 V Disabled
No jumper on J402	**1.05 V Enabled**

6.4 1.8-VDDQ, 0.9-V VTT, and 0.9-V VTTREF Configuration

6.4.1 1.8-VDDQ, 0.9-VTT, and 0.9-VTTREF Enable Selection (J303 for S3, J305 for S5)

Default setting: Jumpers short on J303 and J305 to disable 1.8 VDDQ, 0.9 VTT and 0.9 VTTREF.

Table 13. J303(S3), J305(S5) Enable selection

State	J303	J305	VDDQ, VTT, VTTREF
S0	No jumper	No jumper	All ON
S3	Jumper on	No jumper	VDDQ, VTTREF ON and VTT OFF
S4/S5	**Jumper**	**Jumper**	**All OFF**

6.5 1.5-V CPU PLL Configuration

6.5.1 1.5-V Enable Selection (J306)

1.5-V Enable can be set by J306, EN_1.5V.

Default setting: Jumper shorts on J306 to disable 1.5 V.

Table 14. 1.5-V Enable Selection

Jumper set to	Selection
No jumper	1.5 V Enabled
Jumper on	**1.5 V Disabled**

6.6 1.05-V CPU C6 RAM Configuration

6.6.1 1.05-V CPU C6 RAM Enable Selection (J308)

1.05 V Enable can be set by J308, EN_1.05VC6RAM

Default setting: Jumper shorts on J308 to disable 1.05-V CPU C6 RAM

Table 15. 1.05-V CPU C6 RAM Enable Selection

Jumper set to	Selection
No jumper	1.05-V CPU R6 RAM Enabled
Jumper on	**1.05-V CPU C6 RAM Disabled**

6.7 1.2-V IOH Configuration

6.7.1 1.2-V Enable Selection (J601)

1.2 V Enable can be set by J601, EN_1.2V

Default setting: Jumper shorts on J601 to disable 1.2 V

Table 16. 1.2-V Enable Selection

Jumper set to	Selection
No jumper	1.2 V Enabled
Jumper on	**1.2 V Disabled**

7 Test Procedure

7.1 Line/Load Regulation and Efficiency Measurement Procedure

The CPU measurement is performed as follows.

1. Set up EVM as described in and Section 5.1 and Figure 7.
2. Ensure that the load is set to constant resistance mode and sink 0 A.
3. Ensure that all jumper configuration settings are per Section 6
4. Ensure that S101 VR_ON enable switch is set to OFF position before VIN is applied.
5. Increase VIN from 0 V to 5 V. Use V1 to measure VIN voltage.
6. Set switch S101 to ON position to enable the controller.
7. Use V2 to measure Vcore_c voltage.
8. Vary the load from 0 Adc to 3.5 Adc; Vcore_c must remain in load regulation.
9. Vary VIN from 4.5 V to 5.5 V, Vcore_c must remain in line regulation.
10. Set switch S101 to OFF to disable the controller.
11. Decrease load to 0A
12. Decrease VIN to 0V.
    Other output testing is same.

7.2 Onboard Transient Response Measurement

CPU and GPU Only

1. Set up EVM as described in Section 5.1 and Figure 7.
2. Ensure that all the jumper configuration settings are per Section 6.
3. Remove the load from J102 for CPU or J202 for GPU.
4. Ensure that VR_ON (S101 for CPU and S201 for GPU) are on OFF position before VIN is applied.
5. Increase VIN from 0 V to 5 V. Use V1 to measure VIN voltage.
6. Use TP701(DL_CLK) and TP109(GND) to measure transient timing signal.
7. Push switch SW701(CPU) or SW702(GPU) to ON position.
8. Measure the Vcore_c or Vcore_G transient response by using TP116(CPU) or TP216(GPU).

7.3 Loop Gain/Phase Measurement

CPU, GPU, 3.3-V and 1.05-V CPU VTT Only

1. Set up EVM as described in Section 5.1 and Figure 7.
2. CPU: Connect the isolation transformer to VSNS of J101 (CPU) and Vcore_C (+)(CPU) of J102
   GPU: Connect the isolation transformer to VSNS of J201(GPU) and Vcore_G (+)(GPU) of J202
3. CPU: Connect input signal CHA to VSNS pin of J101, and connect output signal CHB to Vcore_C(+) of J102.
   GPU: Connect input signal CHA to VSNS pin of J201, and connect output signal CHB to Vcore_G(+) of J202
4. Connect the GND lead of CHA and CHB to GND of TP116 (CPU) and TP216 (GPU).
5. Inject approximately 40 mV or less signal through the isolate transformer.
6. Sweep the frequency from 100 Hz to 1MHz with 10 Hz or lower post filter. The control loop gain and phase margin can be measured.
7. Disconnect the isolate transformer from the bode plot setup before making other measurements. Signal injection into feedback may interfere with accuracy of other measurement. The measurement for 3.3-V and 1.05-V CPU VTT is the same.

7.4 Equipment Shutdown

1. Shut down load.
2. Shut down VIN.

8 Performance Data and Typical Characteristic Curves

Figure 8 through Figure 64 present typical performance curves for TPS59610EVM-675.

Jumpers are set to default locations; see Section 6 of this user's guide

8.1 CPU

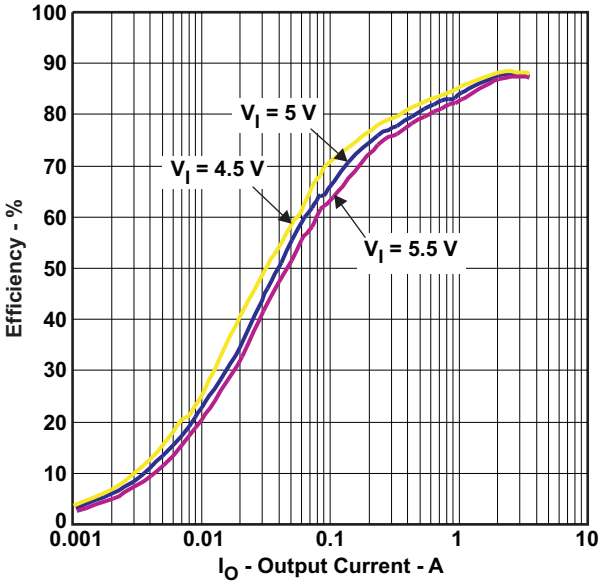


Figure 8. CPU Efficiency

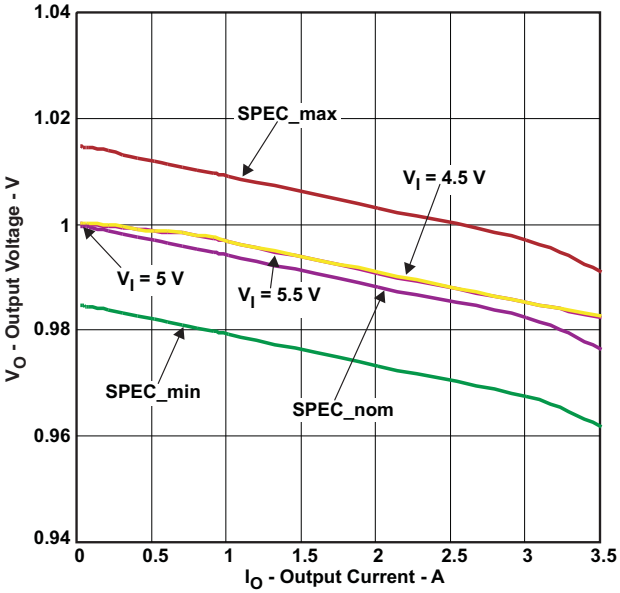


Figure 9. CPU Load Regulation

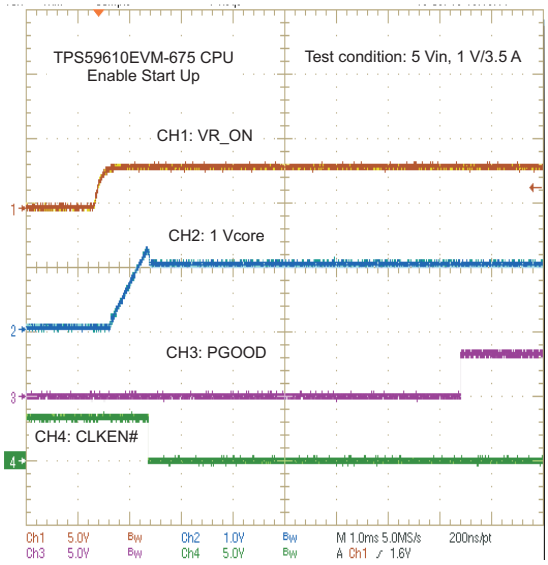


Figure 10. CPU Enable Turnon

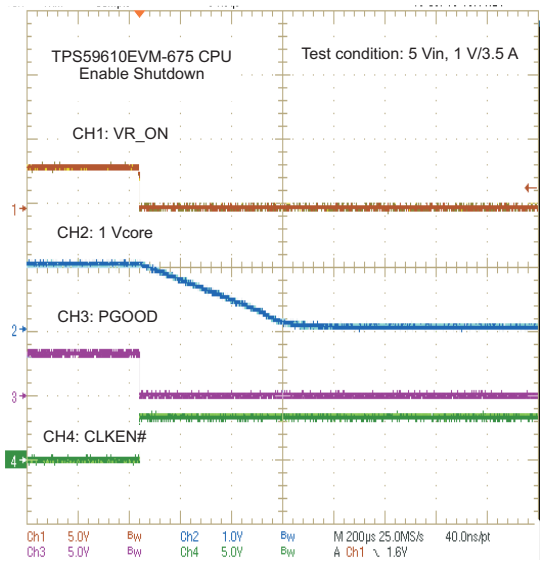


Figure 11. CPU Enable Turnoff

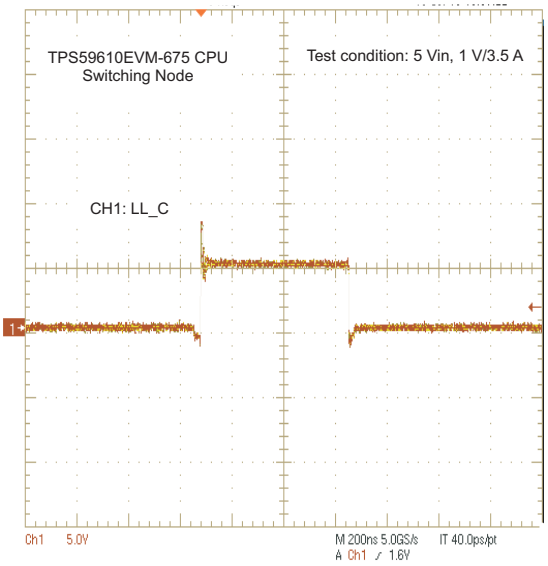


Figure 12. CPU Switching Node

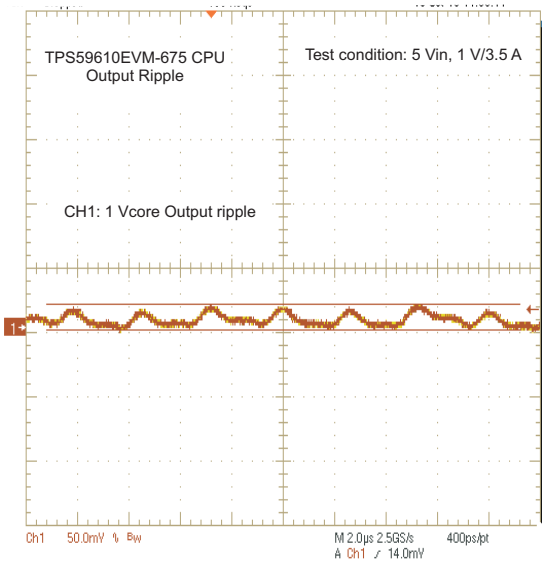


Figure 13. CPU Vcore Ripple

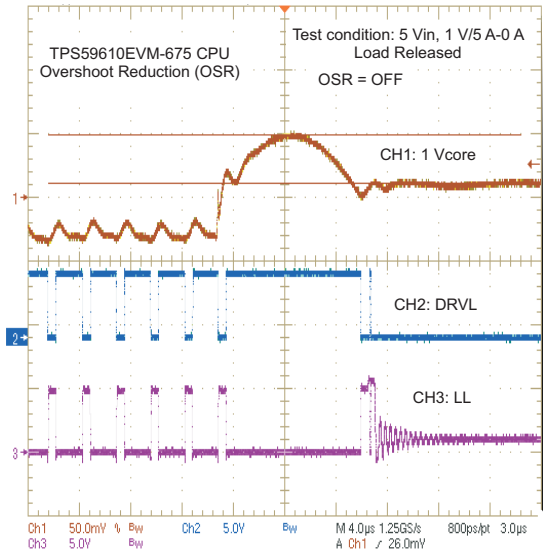


Figure 14. CPU Output Load Release Without Overshoot Reduction

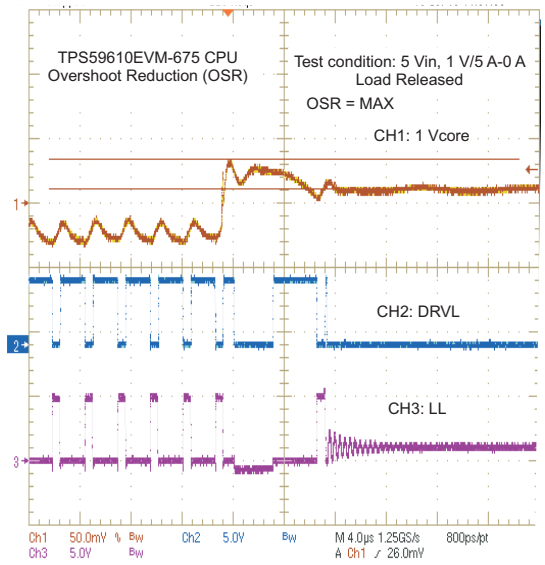


Figure 15. CPU Output Load Release With Maximum Overshoot Reduction

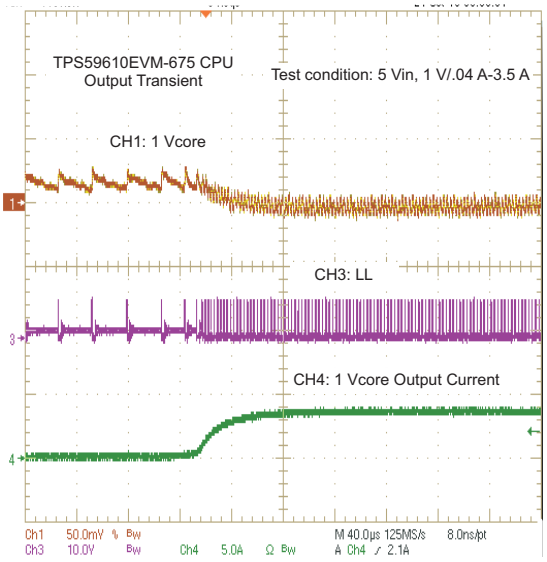


Figure 16. CPU Transient From DCM to CCM

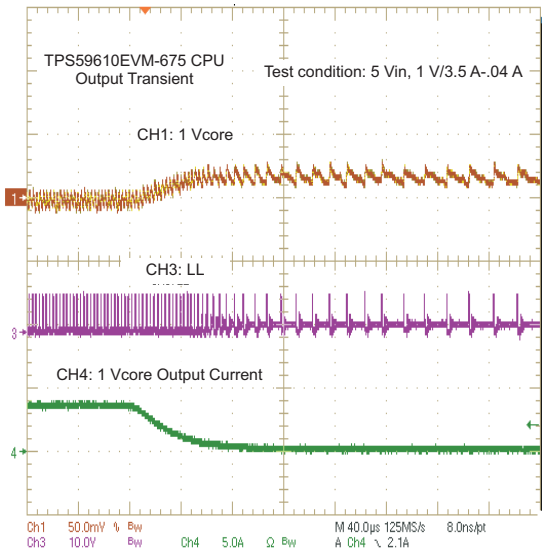


Figure 17. CPU Transient From CCM to DCM

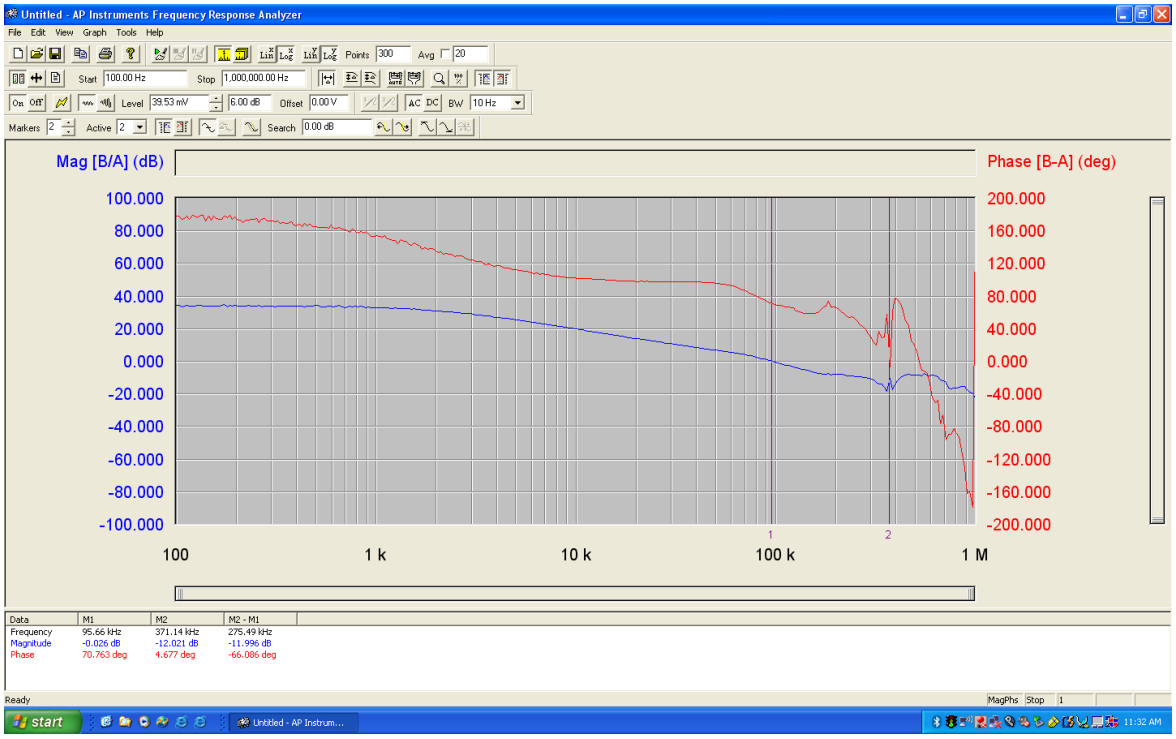


Figure 18. CPU Bode Plot at 5 Vin, 1 V/3.5 A

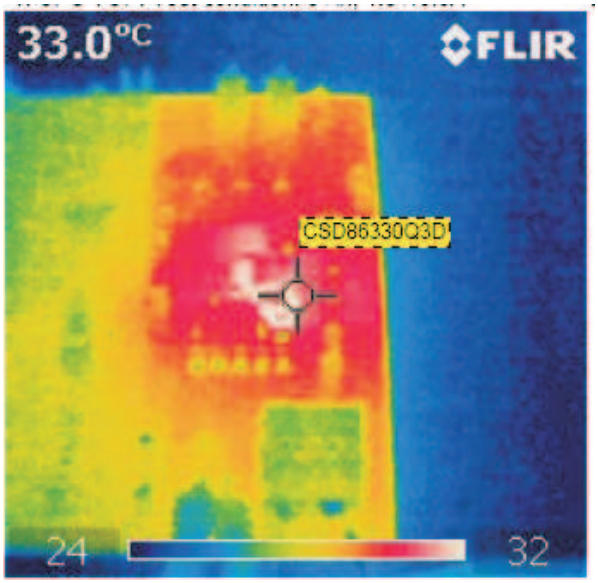


Figure 19. CPU Top Board

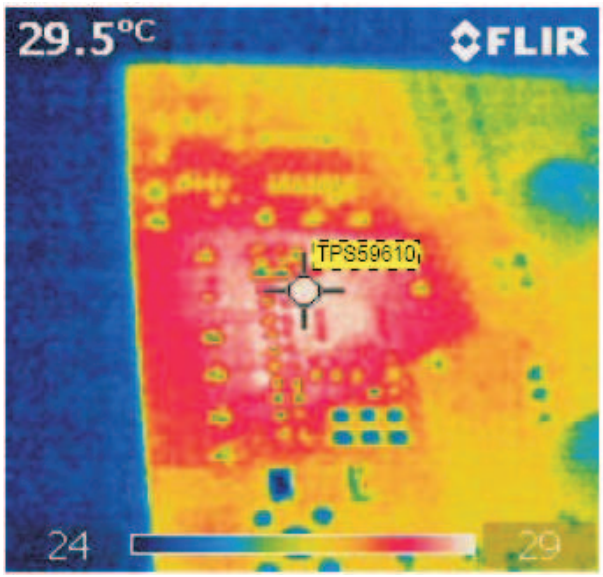


Figure 20. CPU Bottom Board

Test condition: 5Vin, 1.00V/3.5A no airflow

8.2 GPU

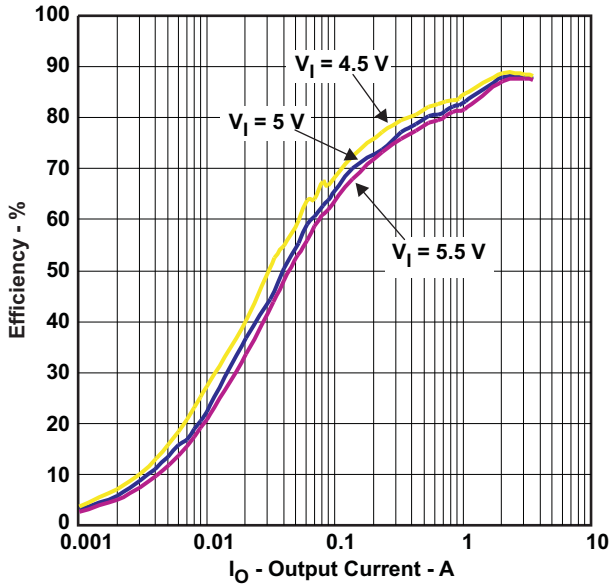
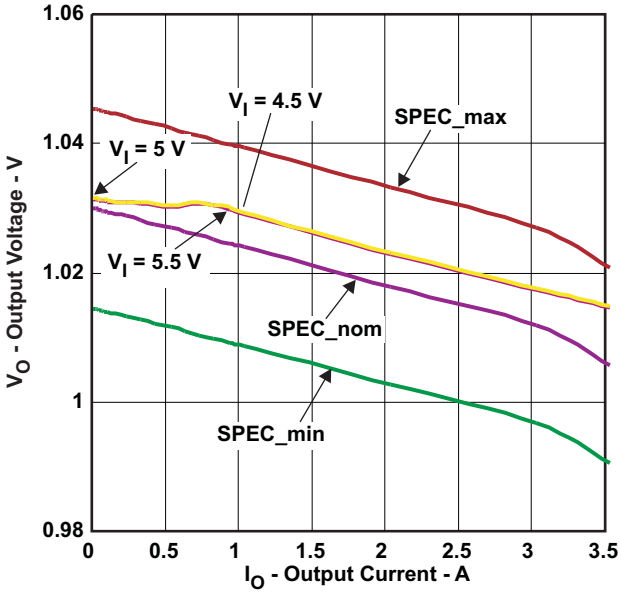


Figure 21. GPU Efficiency



NOTE: Intel spec calls for 3% offset at the VID setting

Figure 22. GPU Load Regulation

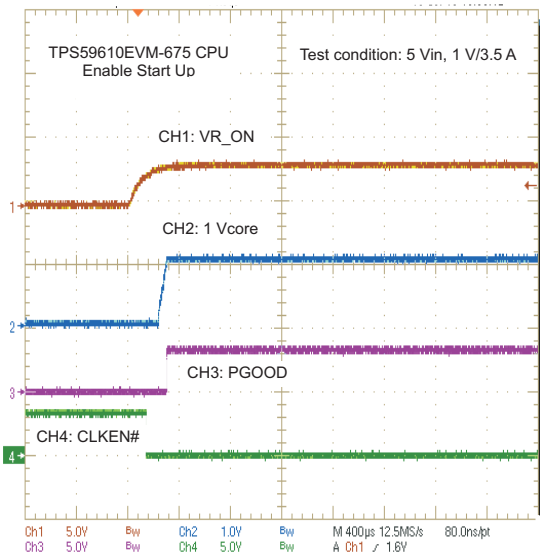


Figure 23. GPU Enable Turnon

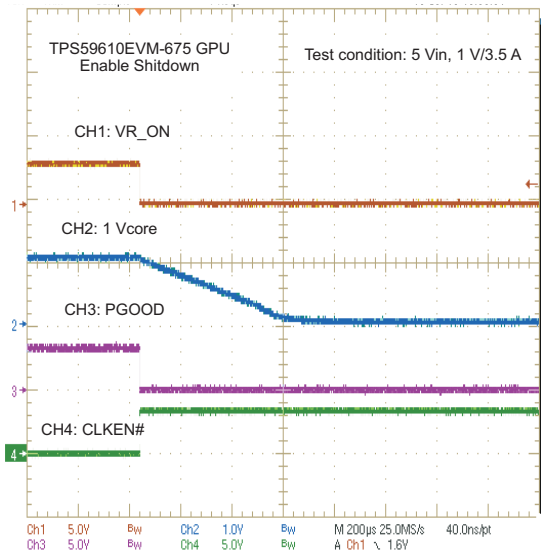


Figure 24. GPU Enable Turnoff

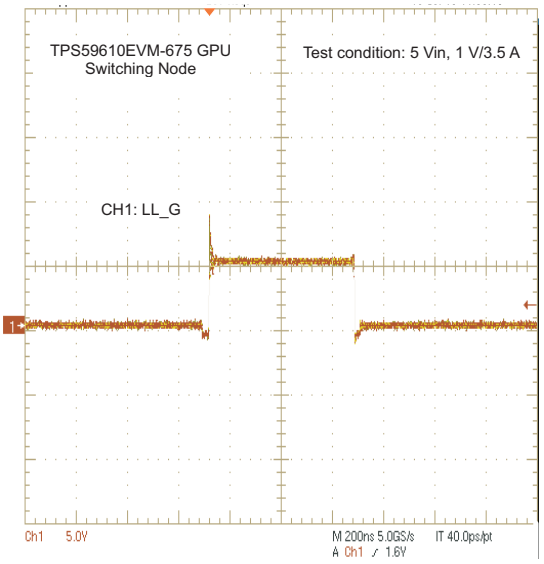


Figure 25. GPU Switching Node

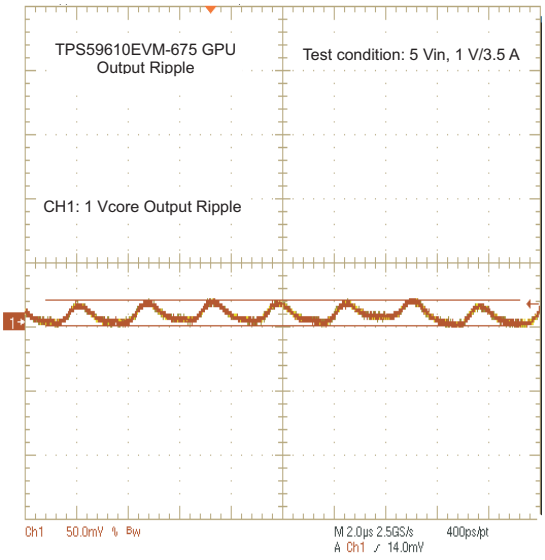


Figure 26. GPU Vcore Ripple

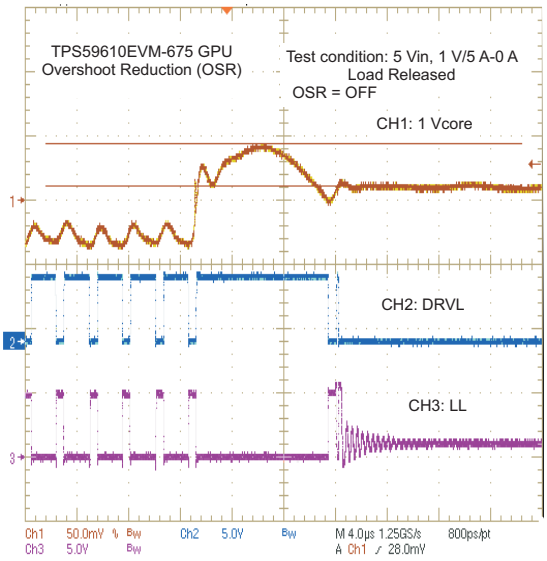


Figure 27. GPU Output Load Release Without Overshoot Reduction

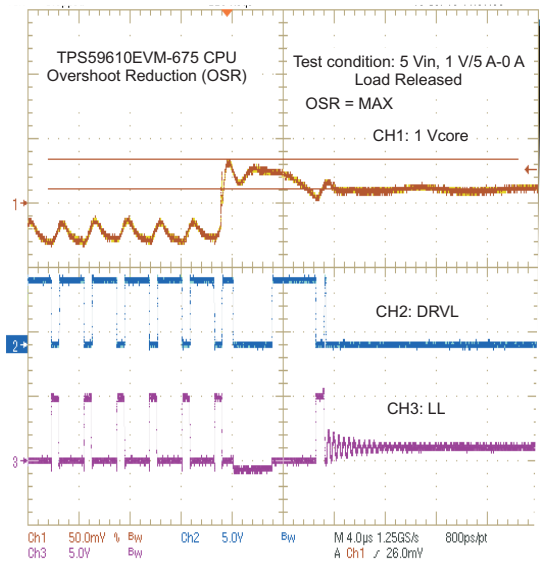


Figure 28. GPU Output Load Release With Maximum Overshoot Reduction

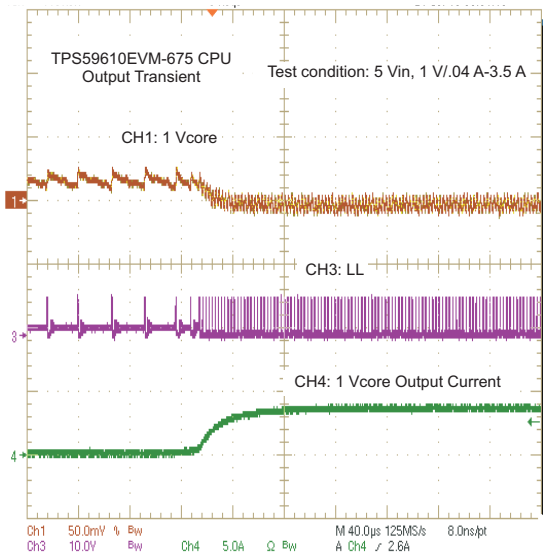


Figure 29. GPU Transient From DCM to CCM

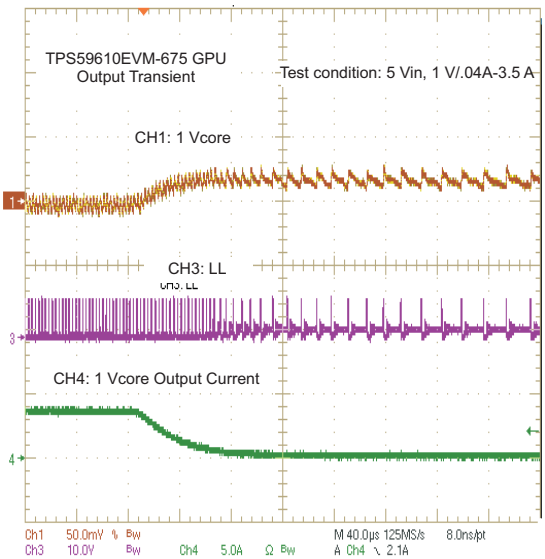


Figure 30. GPU Transient From CCM to DCM

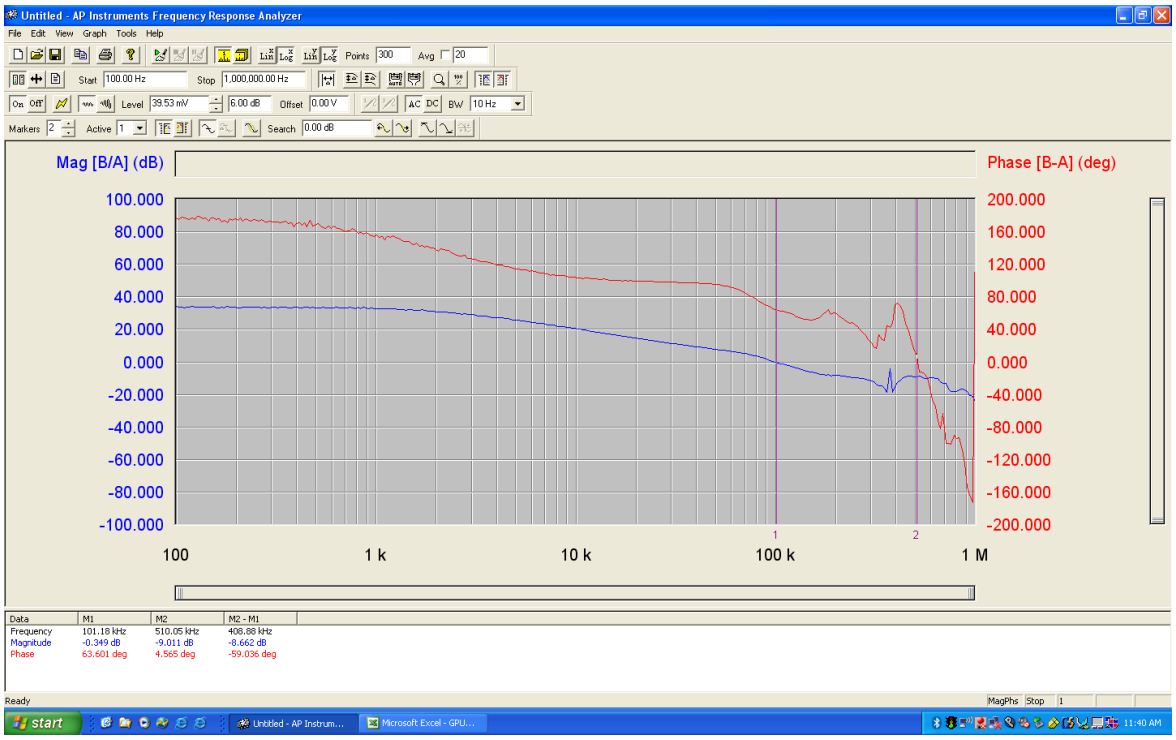


Figure 31. GPU Bode Plot at 5 Vin, 1 V/3.5 A

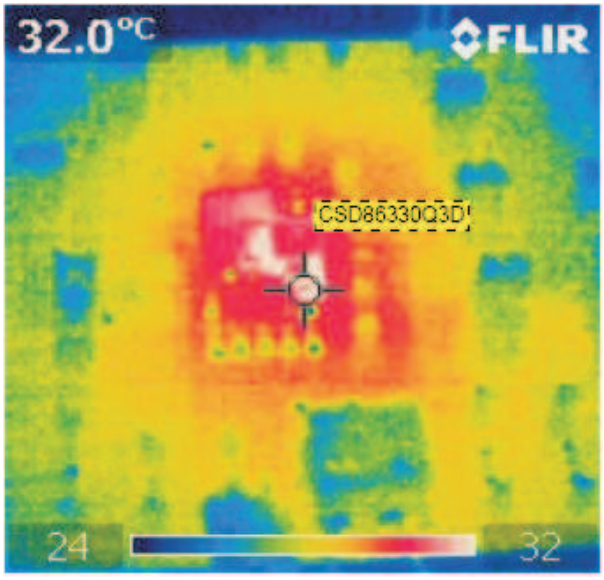


Figure 32. GPU Top Board

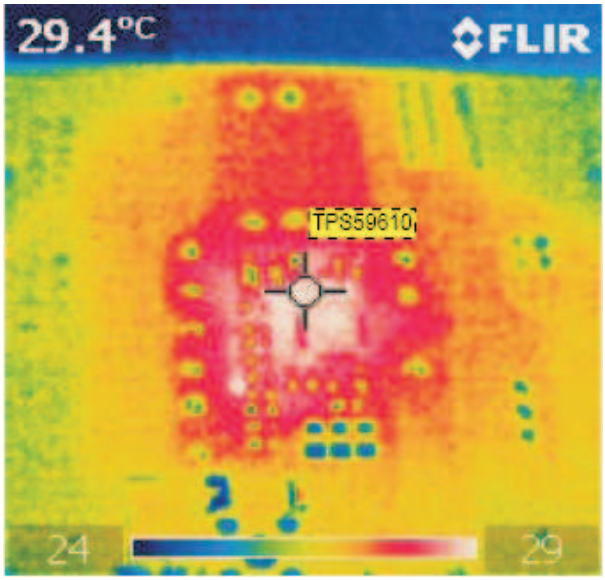


Figure 33. GPU Bottom Board

Test condition: 5 Vin, 1 V/3.5 A, no airflow

8.3 3.3-V System

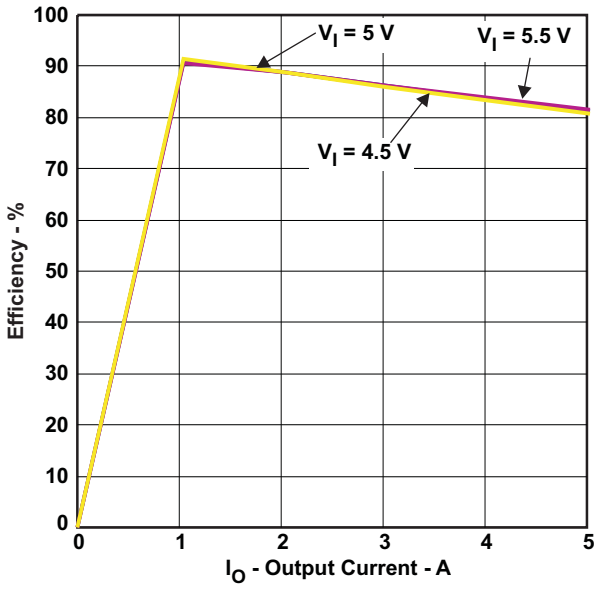


Figure 34. 3.3-V Efficiency

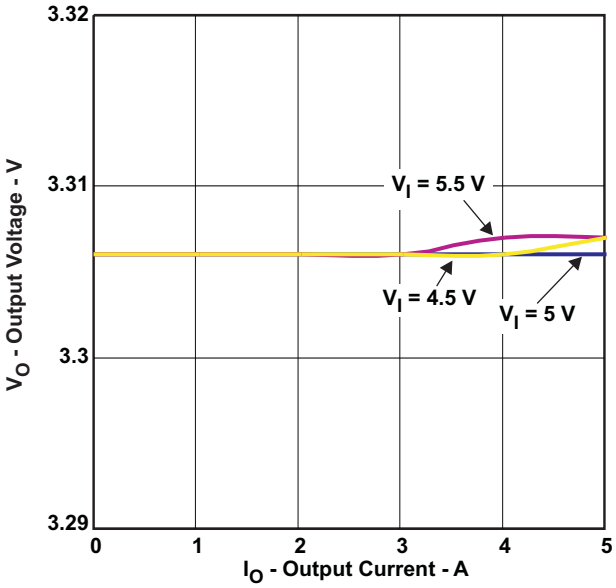


Figure 35. 3.3-V Load Regulation

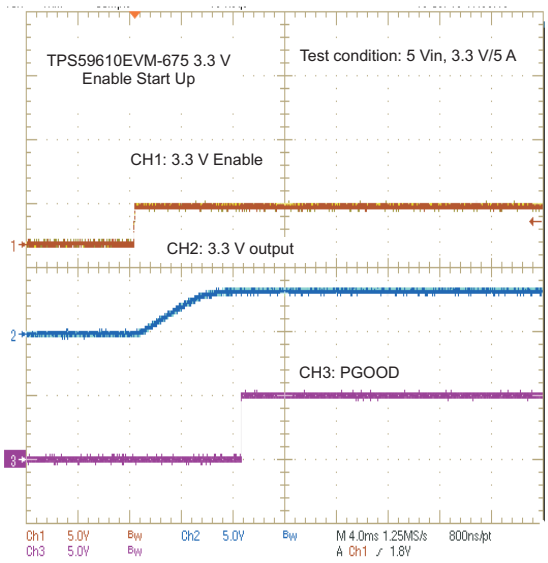


Figure 36. 3.3-V Enable Turnon

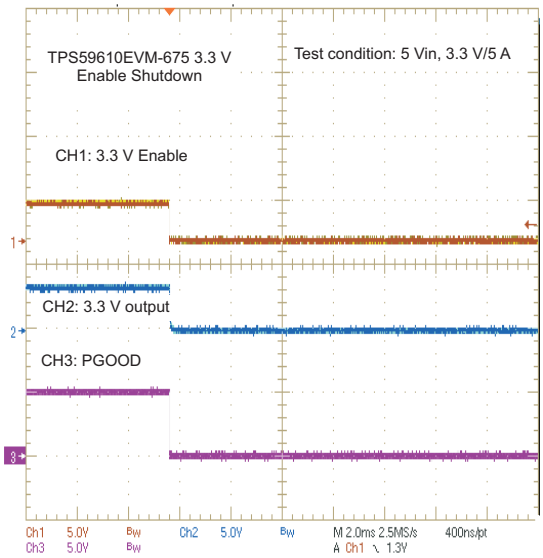


Figure 37. 3.3-V Enable Turnoff

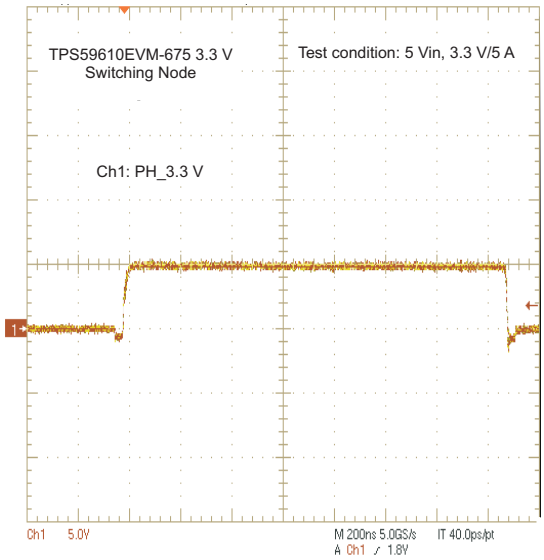


Figure 38. 3.3-V Switching Node

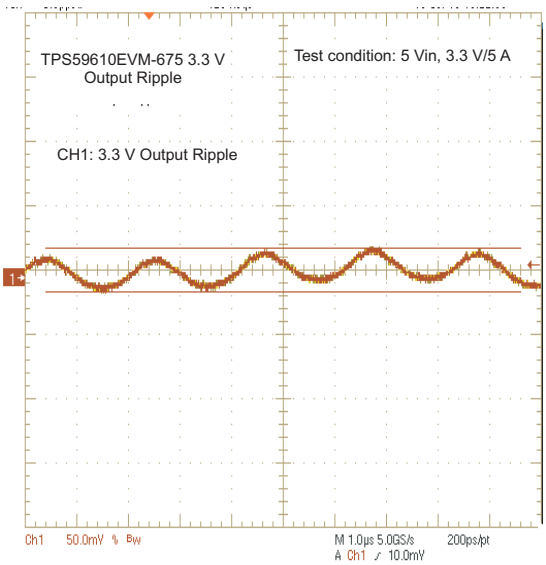


Figure 39. 3.3-V Vo Ripple

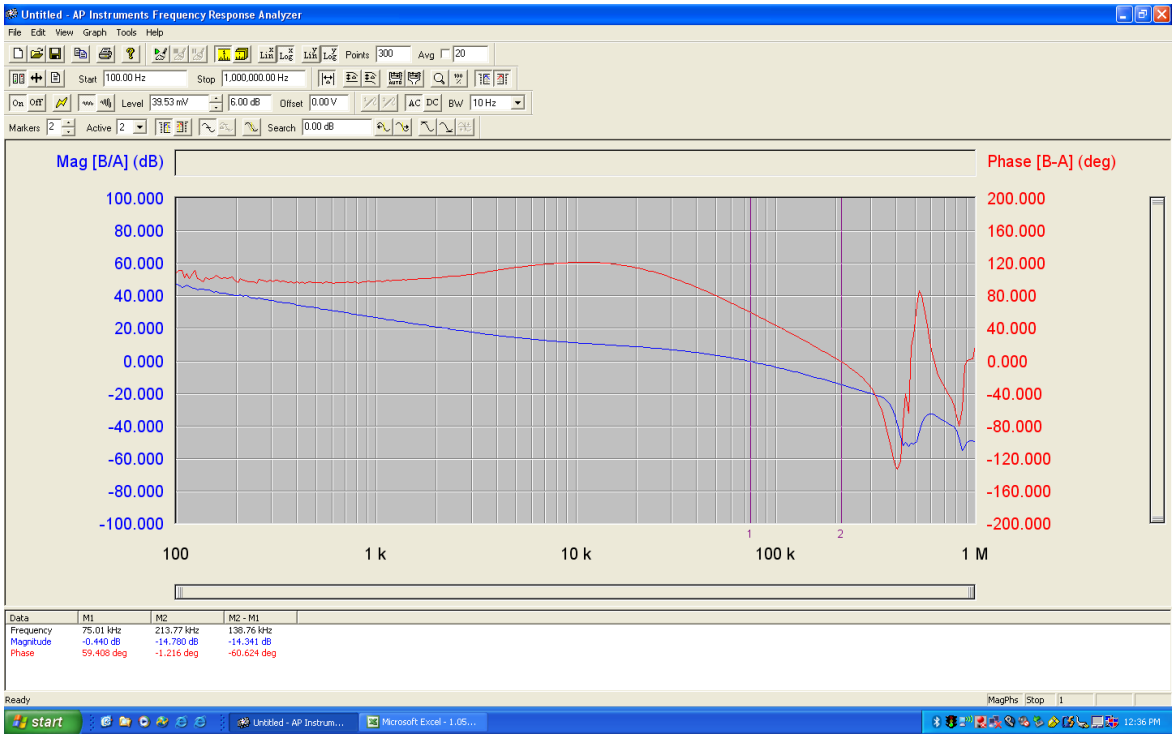


Figure 40. 3.3-V Bode Plot at 5-Vin, 3.3 V/5 A

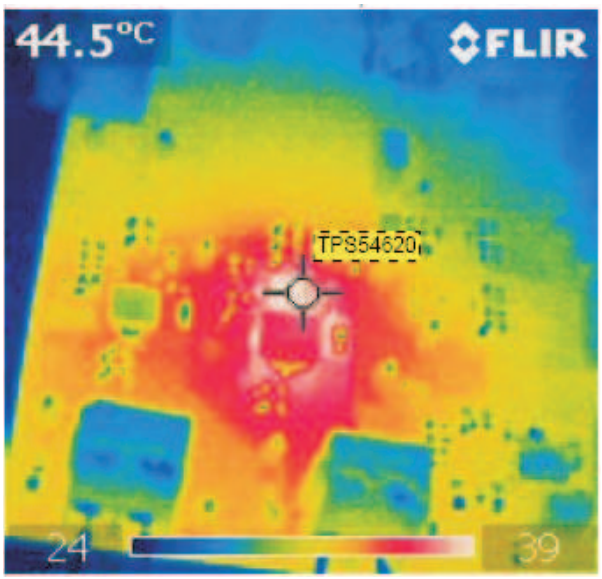


Figure 41. 3.3-V Top at 5 Vin, 3.3 V/5 A, No Airflow

8.4 1.05V CPU VTT

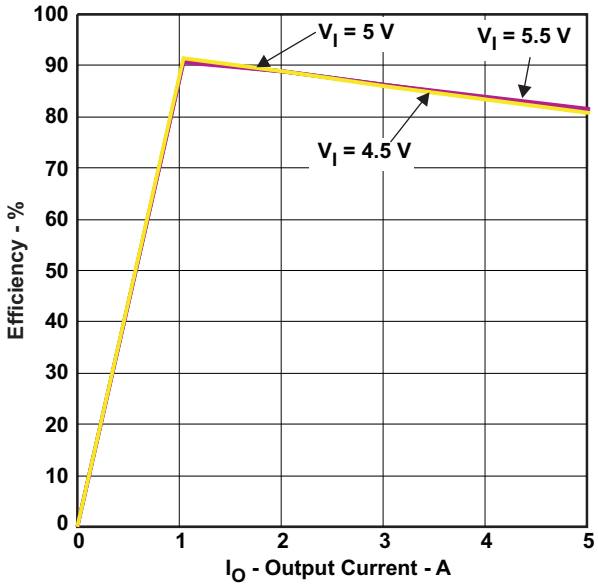


Figure 42. 1.05-V Efficiency

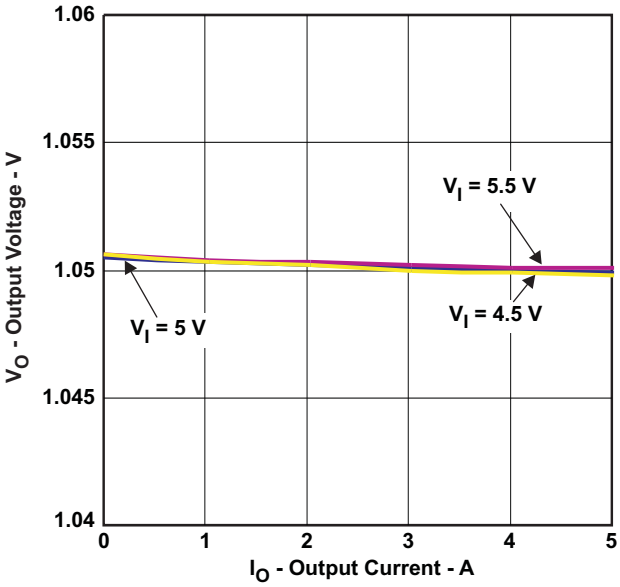


Figure 43. 1.05-V Load Regulation

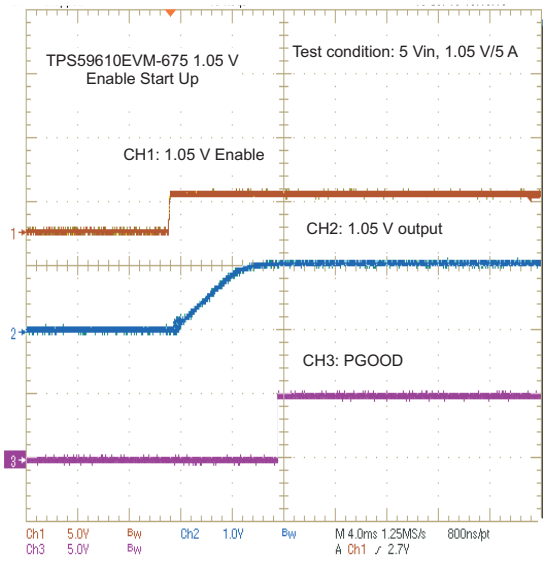


Figure 44. 1.05-V Enable Turnon

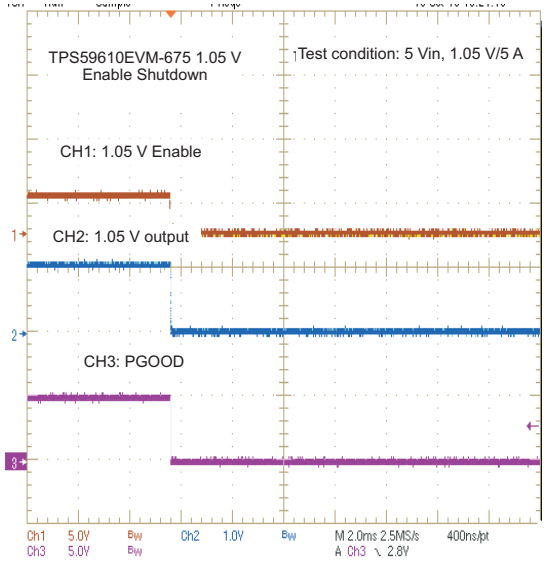


Figure 45. 1.05-V Enable Turnoff

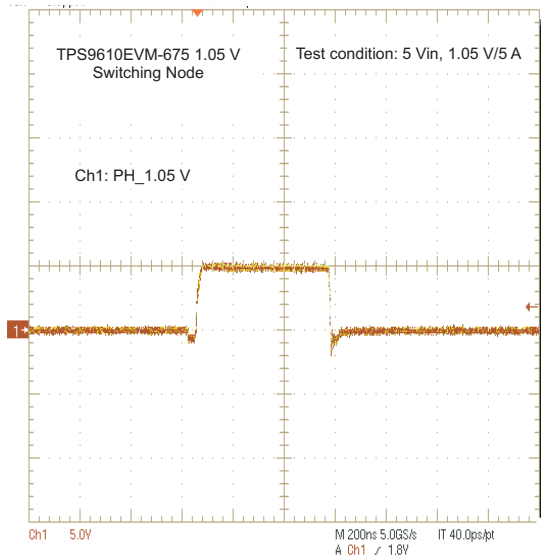


Figure 46. 1.05-V Switching Node

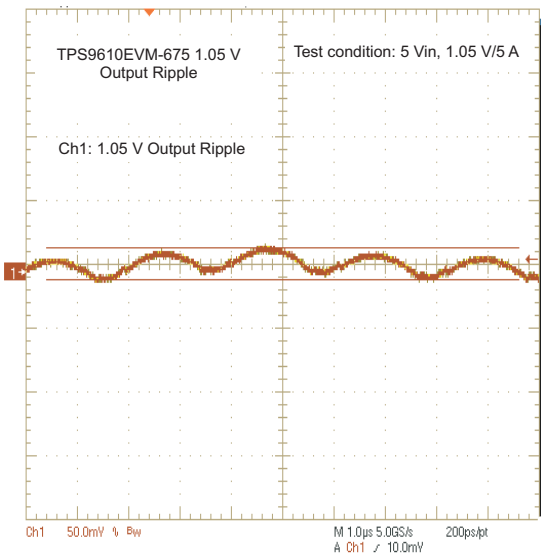


Figure 47. 1.05-V Vo Ripple

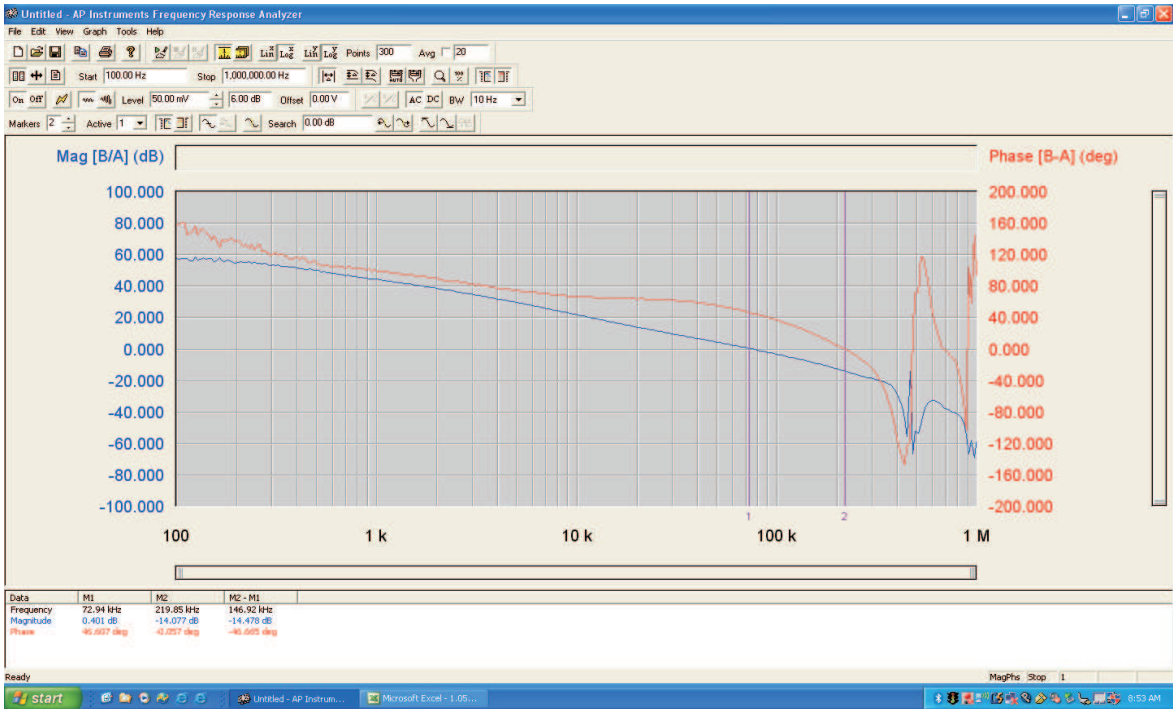


Figure 48. 1.05-V Bode Plot at 5 Vin, 1.05 V/5 A

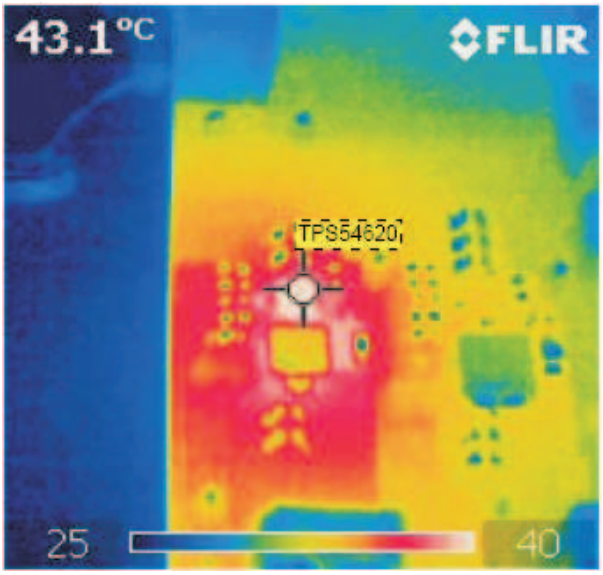


Figure 49. 1.05-V Top Board at 5 Vin, 1.05 V/5 A, No Airflow

8.5 1.8VDDQ

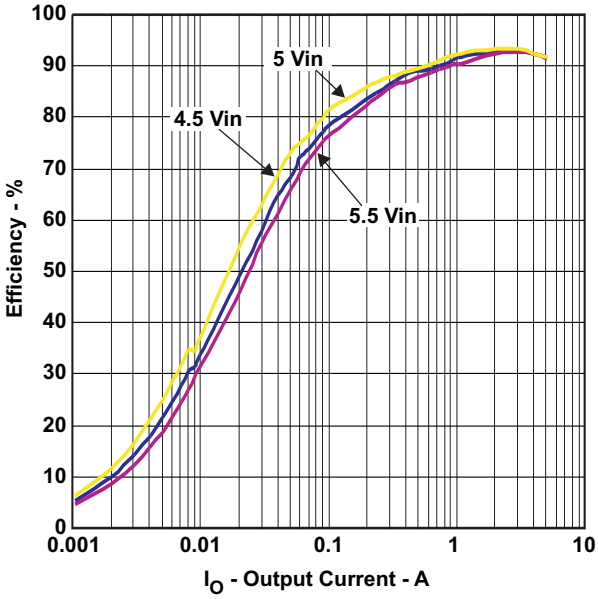


Figure 50. 1.8-V Efficiency

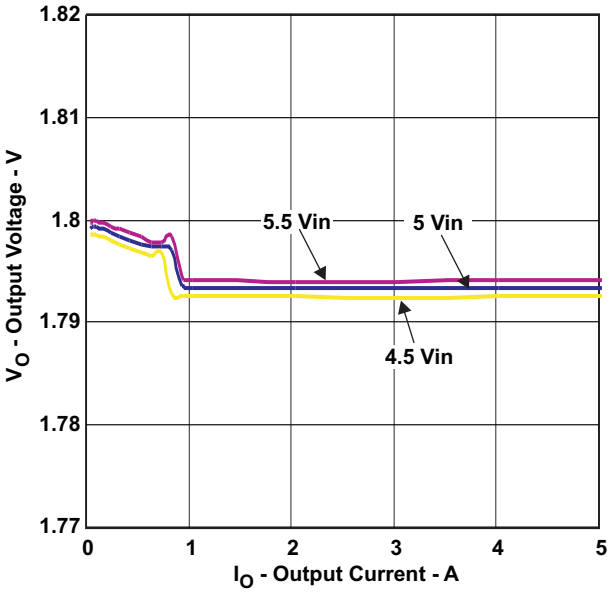


Figure 51. 1.8-V Load Regulation

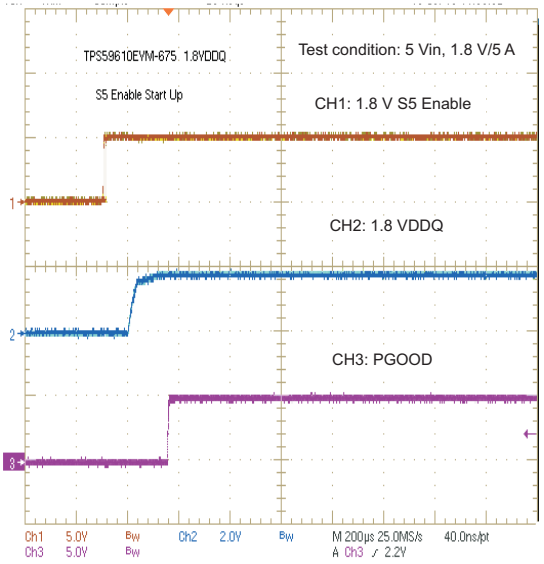


Figure 52. 1.8-V Enable Turnon

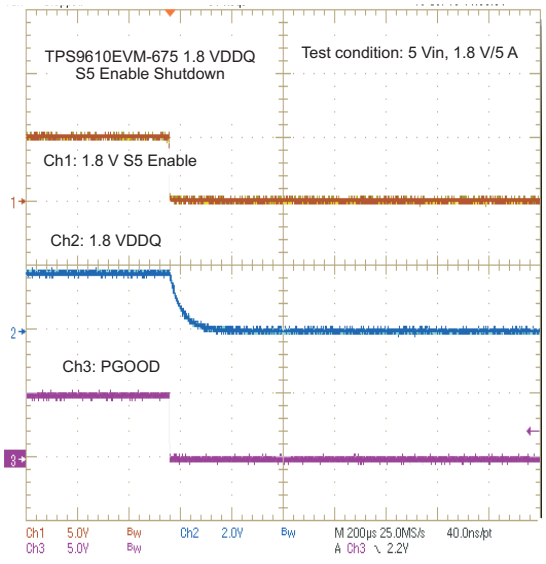


Figure 53. 1.8-V Enable Turnoff

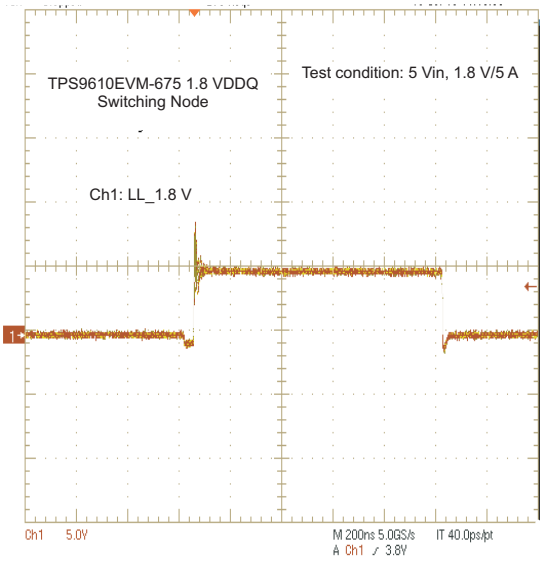


Figure 54. 1.8-V Switching Node

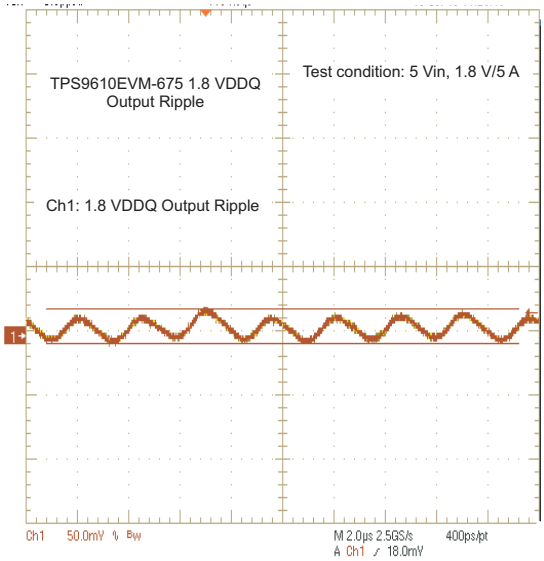


Figure 55. 1.8-V Vo Ripple

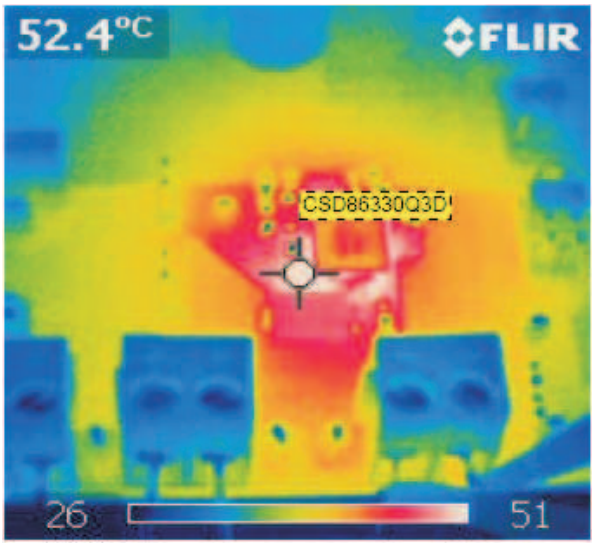


Figure 56. 1.8-V Top Board

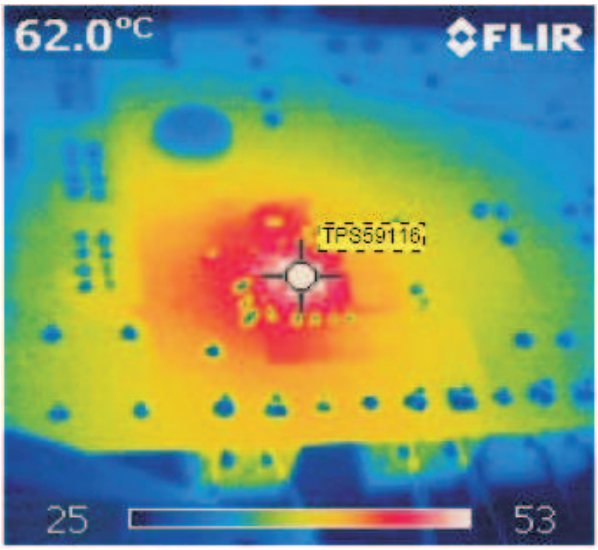


Figure 57. 1.8-V Bottom Board

Test condition: 5 Vin, 1.8 VDDQ/5 A and 0.9 VTT/1.7 A no airflow

8.6 1.2-V IOH

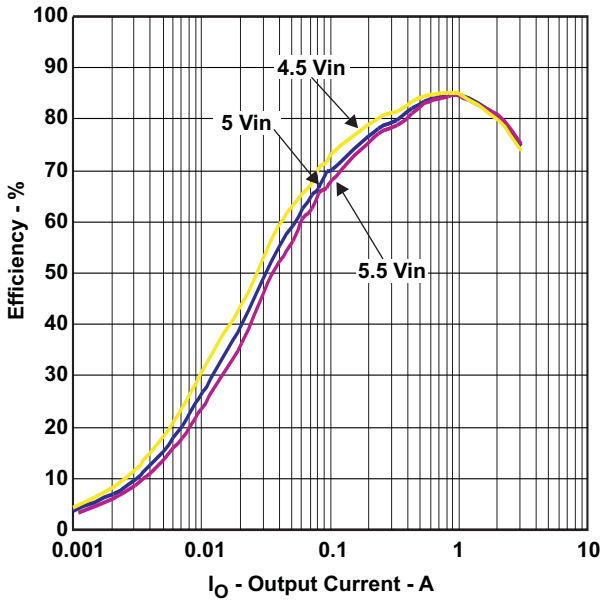


Figure 58. 1.2-V Efficiency

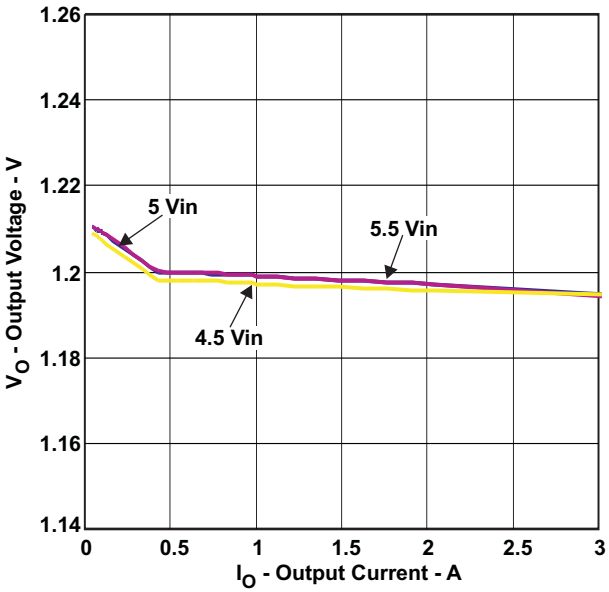


Figure 59. 1.2-V load regulation

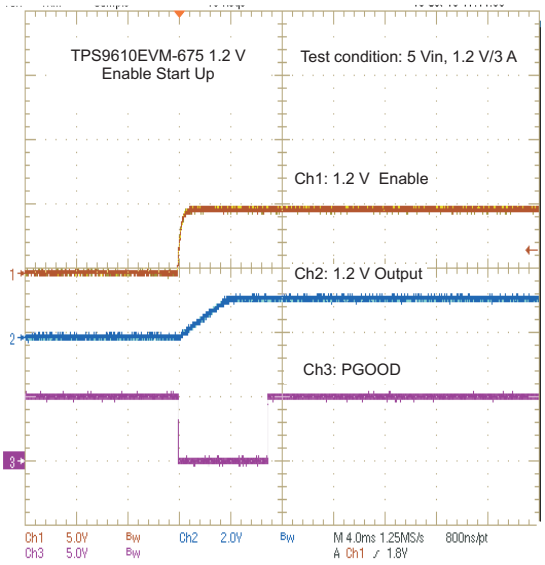


Figure 60. 1.2-V Enable Turnon

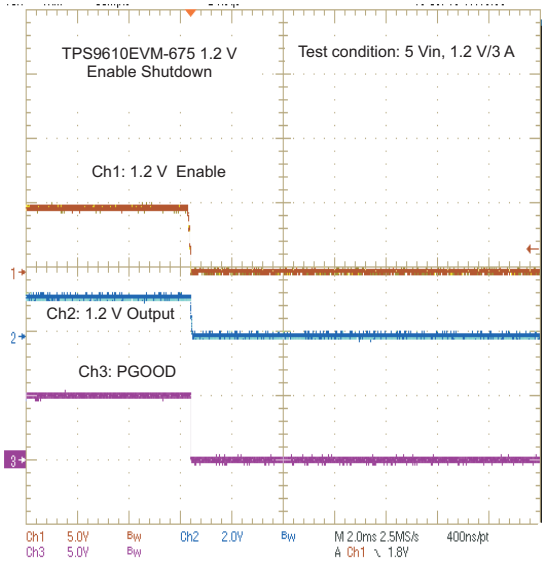


Figure 61. 1.2-V Enable Turnoff

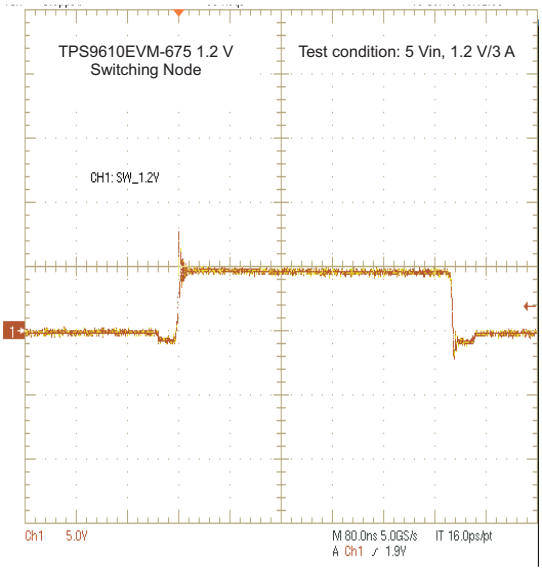


Figure 62. 1.2-V Switching Node

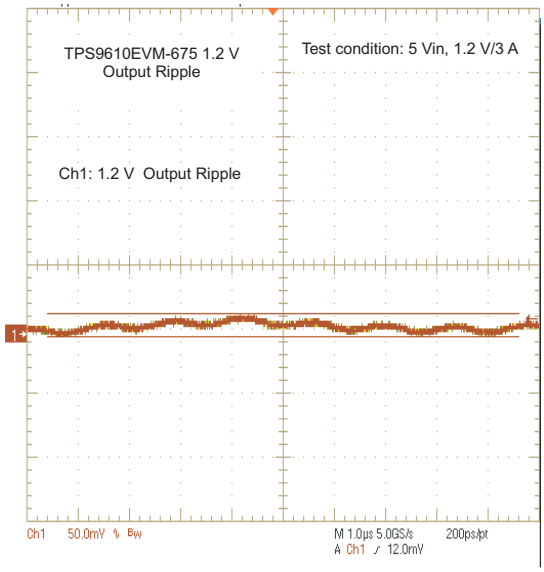
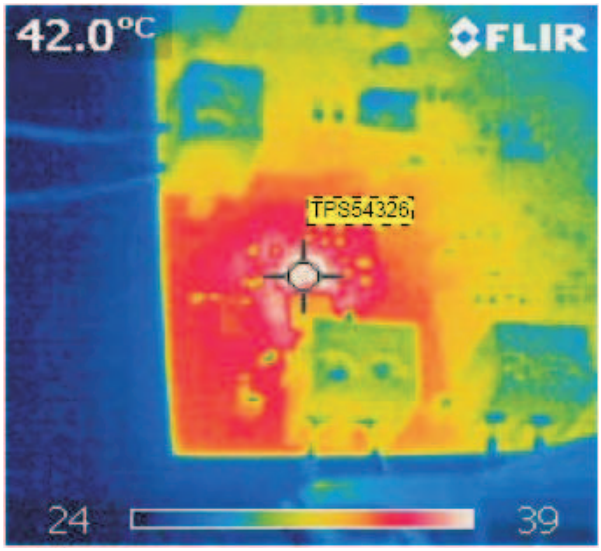


Figure 63. 1.2-V Vo Ripple



Test condition: 5 Vin, 1.2V/3A no airflow

Figure 64. 1.2-V Top Board

9 EVM Assembly Drawings and PCB layout

Figure 65 through Figure 70 show the design of the TPS59610EVM-675 printed circuit board. The EVM has been designed using 4 Layers circuit board with 2oz copper on outside layers.

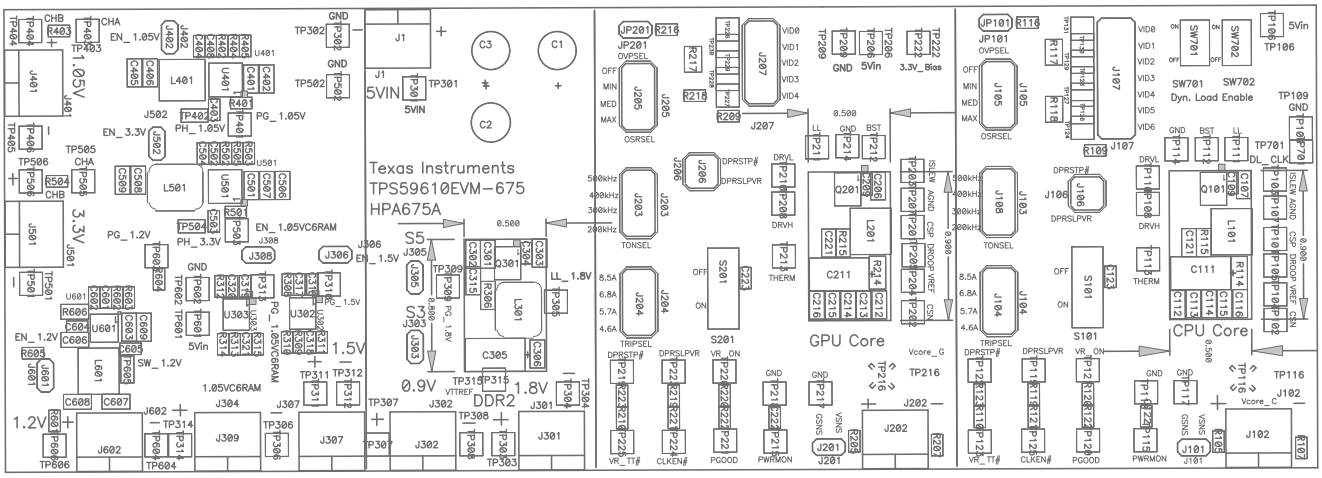


Figure 65. TPS59610EVM-675 Top Layer Assembly Drawing, Top View

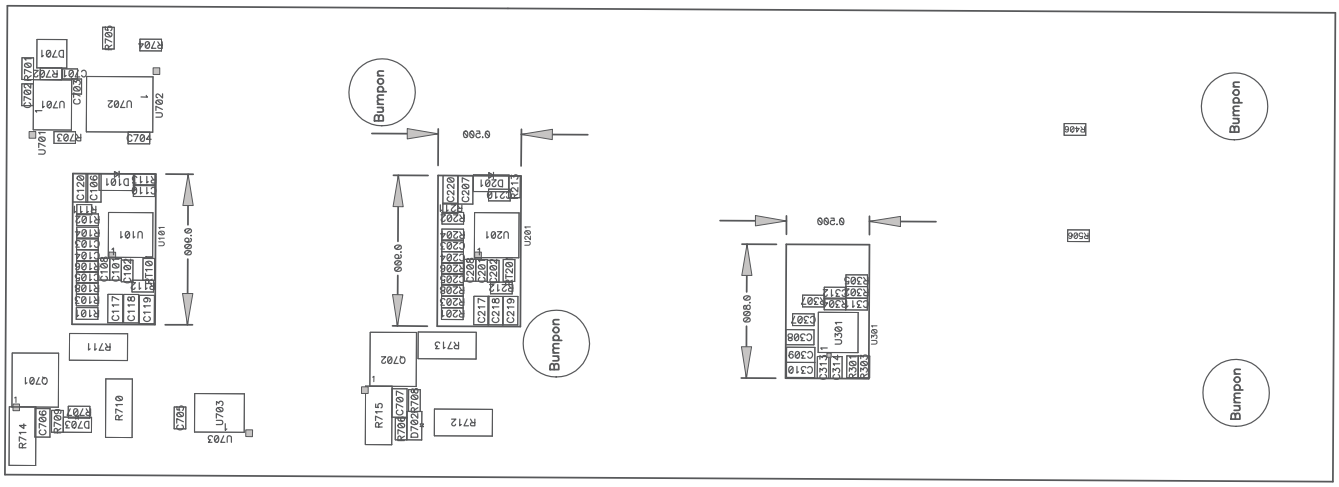


Figure 66. TPS59610EVM-675 Bottom Assembly Drawing, Bottom View

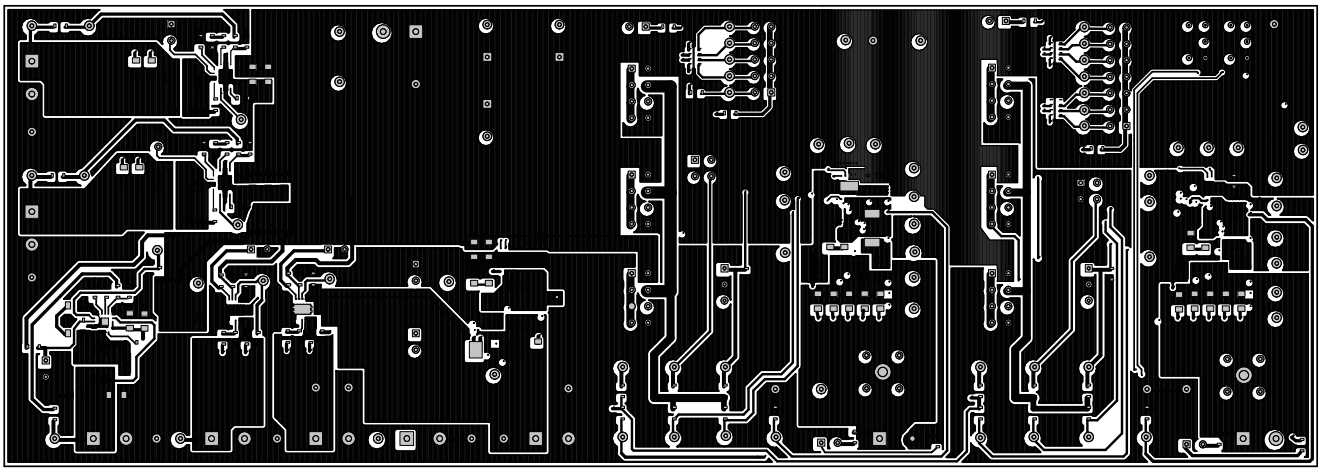


Figure 67. TPS59610EVM-675 Top Copper, Top View

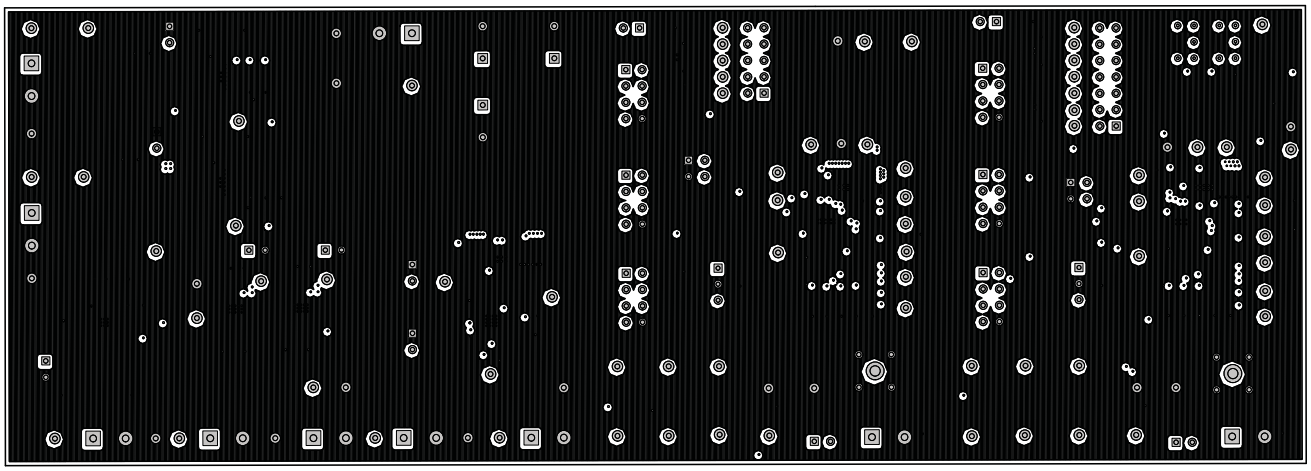


Figure 68. TPS59610EVM-675 Internal Layer 2, Top View

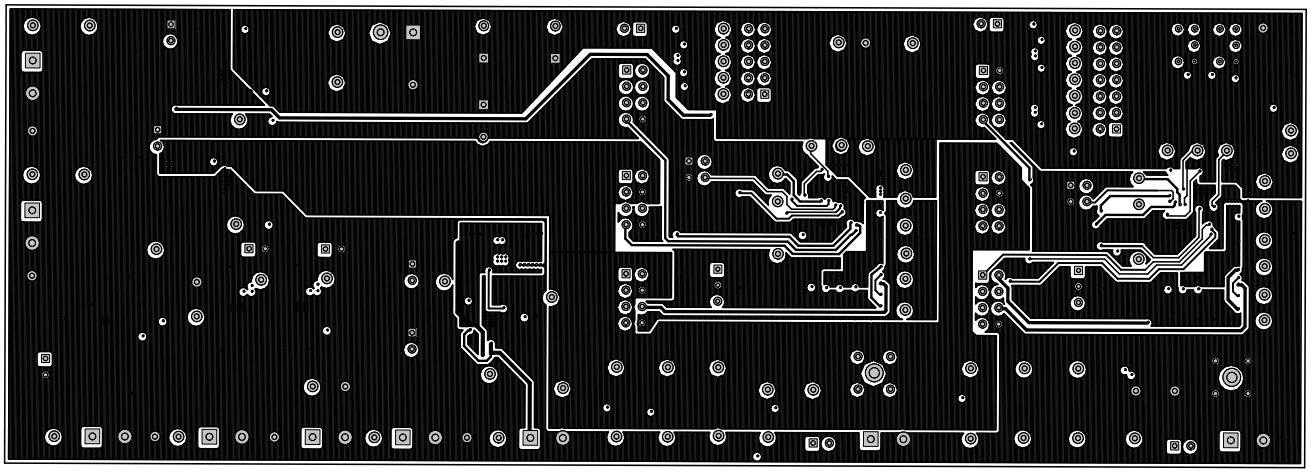


Figure 69. TPS59610EVM-675 Internal Layer 3, Top View

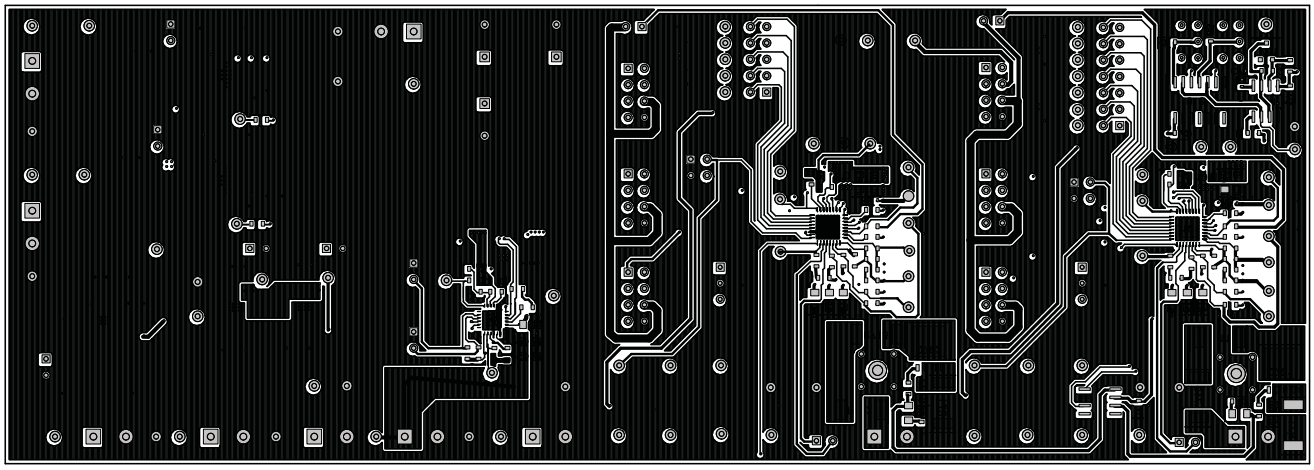


Figure 70. TPS59610EVM-675 Bottom Layer, Bottom View

10 Bill of Materials

Table 17 list the EVM major components according to the schematic shown in Figure 2 through Figure 6.

Table 17. Bill of Materials

QTY	RefDes	Description	MFR	Part Number
3	C1, C2, C3	Capacitor, Aluminum, 1000 µF, 6.3V, 20%, 105°C	Rubycon	6.3ZL1000M10x12.5
4	C101, C102, C201, C202	Capacitor, Ceramic, 100pF, 50V, C0G, 10%, 0603	STD	STD
15	C103, C108, C110, C203, C208, C210, C304, C311, C313, C317, C320, C601, C702, C704, C705	Capacitor, Ceramic, 1 µF, 16V, X7R, 20%, 0603	STD	STD
2	C104, C204	Capacitor, Ceramic, 68 pF, 50V, C0G, 10%, 0603	STD	STD
27	C106, C107, C112–C116, C120, C206 ,C207, C212–C216, C220, C301–C303, C306, C308,C401, C402, C501, C506, C507, C603	Capacitor, Ceramic, 10 µF, 6.3V, X5R, 20%, 0805	STD	STD
2	C109, C209	Capacitor, Ceramic, 1000 pF, 50V, X7R, 20%, 0603	STD	STD
2	C111, C211	Capacitor, Polymer, 220 µF, 2V, 20%, 9mohm, 7343	Panasonic-ECG	EEF-SX0D221R
3	C121, C221, C315,	Capacitor, Ceramic, 2200 pF, 50V, X7R, 20%, 0805	STD	STD
5	C122, C123, C222, C223, C602	Capacitor, Ceramic, 0.01 µF, 50V, X7R, 20%, 0603	STD	STD
4	C307, C403, C503,C605	Capacitor, Ceramic, 0.1 µF, 50V, X7R, 20%, 0603	STD	STD
8	C309, C310, C405, C406, C508, C509, C607, C608	Capacitor, Ceramic, 22 µF, 6.3V, X5R, 20%, 0805	STD	STD
5	C312, C316, C318, C319, C321	Capacitor, Ceramic, 4.7 µF, 6.3V, X5R, 20%, 0603	STD	STD
1	C314	Capacitor, Ceramic, 0.033 µF, 50V, X7R, 20%, 0603	STD	STD
1	C305	Capacitor, Polymer, 100 µF, 2V, 20%, 7343D	Panasonic-ECG	EEF-CD0D101R
2	C404, C504	Capacitor, Ceramic, 0.015 µF, 50V, X7R, 20%, 0603	STD	STD
2	C407, C502	Capacitor, Ceramic, 8200 pF, 50V, X7R, 20%, 0603	STD	STD
1	C604	Capacitor, Ceramic, 0.022 µF, 50V, X7R, 20%, 0603	STD	STD
1	C701	Capacitor, Ceramic, 0.01 µF, 25V, X7R, 20%, 0402	STD	STD
1	C703	Capacitor, Ceramic, 0.1 µF, 16V, X7R, 20%, 0402	STD	STD
2	D101, D201	Diode, Schottky, 0.5A, 30V, SOD-123,	On Semi	MBR0530T1G
1	D701	Diode, Schottky, 200mA, 30V, SOT-23,	Micro	BAT54-TP
2	D702, D703	Diode, LED, Green Clear, 20mcd, 0.079x0.049	Lite On	LTST-C170GKT
3	L101, L201, L401	Inductor, SMT, 1 µH, 9.2A , 13.2mΩ, 0.204" x 0.216"	Vishay	IHLP2020CZER1R0M01
2	L301, L501	Inductor, SMT, 1.5 µH, 9A , 15mΩ, 0.255" x 0.270"	Vishay	IHLP2525CZER1R5M01
1	L601	Inductor, SMT, 1.5 µH, 7.2A, 20.7mΩ, 0.204" x 0.216"	Vishay	IHLP2020CZER1R5M01
3	Q101, Q201, Q301	MOSFET, Synchronous Buck NexFET Power Block SON 3.3 x 3.3mm	TI	CSD86330Q3D
2	Q701, Q702	MOSFET, Nchan, 25V, 31A, 2.5mΩ, QFN5X6mm	TI	CSD16407Q5
4	R101, R103, R201, R203	Resistor, Chip, 475, 1/16W, 1%, 0603	STD	STD
23	R102, R119–R122, R202, R219–R222, R301, R303,R308, R312, R405, R503, R603, R605, R703–R705,R406, R506	Resistor, Chip, 10k, 1/16W, 1%, 0603	STD	STD
2	R112, R212	Resistor, Chip, 2.00k, 1/16W, 1%, 0603	STD	STD
2	R104, R204	Resistor, Chip, 45.3k, 1/16W, 1%, 0603	STD	STD
4	R105, R107, R205, R207	Resistor, Chip, 10, 1/16W, 1%, 0603	STD	STD
2	R106, R206	Resistor, Chip, 6.19k, 1/16W, 1%, 0603	STD	STD
2	R109, R209	Resistor, Chip, 1, 1/16W, 5%, 0603	STD	STD
4	R110, R123, R210, R223	Resistor, Chip, 1.00k, 1/16W, 1%, 0603	STD	STD
1	R402	Resistor, Chip, 1.15k, 1/16W, 1%, 0603	STD	STD
1	R502	Resistor, Chip, 2.15k, 1/16W, 1%, 0603	STD	STD
2	R111, R211	Resistor, Chip, 0, 1/16W, 5%, 0402	STD	STD
1	R213	Resistor, Chip, 5.90, 1/16W, 1%, 0603	STD	STD
2	R114, R214	Resistor, Metal Film, 0.003, 1/4W, 1%, 1206	STD	STD
3	R115, R215, R306	Resistor, Metal Film, 0.47, 1/8W, 5%, 0805	STD	STD
2	R116, R216	Resistor, Chip, 78.7k, 1/16W, 1%, 0603	STD	STD
3	R117, R118, R217	Resistor, Chip Array, 100k, 62.5mW, 5%, 612	Yageo	TC164-JR-07100KL
8	R218, R302, R311, R315, R401, R501, R604, R702	Resistor, Chip, 100k, 1/16W, 1%, 0603	STD	STD
1	R304	Resistor, Chip, 4.02k, 1/16W, 1%, 0603	STD	STD
1	R305	Resistor, Chip, 5.11, 1/16W, 5%, 0603	STD	STD
2	R307, R113	Resistor, Chip, 0, 1/16W, 5%, 0603	STD	STD

Table 17. Bill of Materials (continued)

QTY	RefDes	Description	MFR	Part Number
1	R309	Resistor, Chip, 6.81k, 1/16W, 1%, 0603	STD	STD
2	R310, R314	Resistor, Chip, 7.87k, 1/16W, 5%, 0603	STD	STD
1	R313	Resistor, Chip, 2.49k, 1/16W, 1%, 0603	STD	STD
1	R403	Resistor, Chip, 49.9, 1/16W, 1%, 0603	STD	STD
1	R404	Resistor, Chip, 3.09k, 1/16W, 1%, 0603	STD	STD
1	R504	Resistor, Chip, 453, 1/16W, 1%, 0603	STD	STD
1	R505	Resistor, Chip, 30.9k, 1/16W, 1%, 0603	STD	STD
1	R601	Resistor, Chip, 68.1, 1/16W, 1%, 0603	STD	STD
1	R602	Resistor, Chip, 5.62k, 1/16W, 1%, 0603	STD	STD
1	R701	Resistor, Chip, 8.06k, 1/16W, 1%, 0603	STD	STD
2	R706, R707	Resistor, Chip, 330, 1/16W, 1%, 0603	STD	STD
2	R708, R709	Resistor, Chip, 100, 1/16W, 1%, 0603	STD	STD
2	R714, R715	Resistor, Chip, 0.001, 2W, 1%, 2512	STD	STD
4	R710–R713	Resistor, Chip, 0.100, 2W, 1%, 2512	STD	STD
2	RT101, RT210	NTC Thermistor, 150k, 0603, 5%	Panasonic-ECG	ERTJ1VV154J
2	U101, U210	IC, Single phase, D-CAP Synchronous Buck Controller, QFN-32	TI	TPS59610RHB
1	U301	IC, Synchronous controller w/Termination LDO, QFN-24	TI	TPS59116RGE
2	U302, U303	IC, 1.5A LDO Regulator with soft start, SON-10	TI	TPS74801DRC
2	U401, U501	IC, 1.62V-17V Synchronous buck PWM controller with integrated MOSFET, QFN-14	TI	TPS54620RGY
1	U601	IC, 4.5-18V Input, 3A Step down Regulator with integrated Switcher, QFN-16	TI	TPS54326RGT
1	U502	IC, Timer, Lower power CMOS, SO-8	TI	TLC555CD
1	U503	IC, Dual 4A high speed low side MOSFET driver, SO-8	TI	UCC37324DR
1	U504	IC, Quadruple 2 Input positive And Gates, SO-14	TI	SN74HC08D

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 4.5 V to 5.5 V and the output voltage range of 0.9 V to 3.3 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265