Using the TPS54672 Tracking/Termination Synchronous PWM Switcher With Integrated FETs (SWIFT™) for DDR and Bus Termination Applications

John Tucker *High Performance Analog, Power Management Products*

Introduction

Integrated FET, SWIFT™ TPS54672 regulators from Texas Instruments are a simple and low-cost solution for DDR memory bus and other high-speed logic bus termination voltage (V_{TT}) applications. These applications are typically high-performance designs requiring fast transient response, the ability to track an external voltage reference, and current source and sink capability. Additionally, since the V_{TT} generation circuit should be placed as close as possible to the termination resistors on the bus, many of these applications are also space critical and require a solution that uses a minimum amount of board space. By operating the TPS54672 at the optimum frequency of 700 kHz, a low-value, small size output inductor may be used. This, along with the small number of external components required by the TPS54672, allows for a complete 6-A DDR memory bus termination point of load regulator in a space of only 1.33” x 0.445” x 0.3” (see Figure 1).

For the output supply voltage, V_{DDQ}, the TPS54610 can provide a complementary solution in a similar board space.

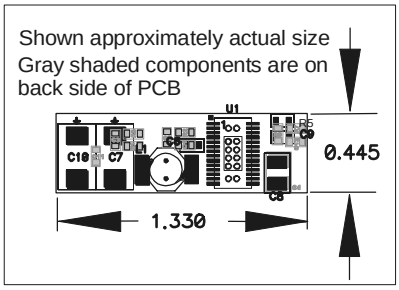

Figure 1. TPS54672 Layout

Design Requirements

For DDR memory bus termination, the V_{TT} voltage generation circuit must be able to accurately track a reference voltage, V_{REF}, that is 50% V_{DDQ}.

Additionally, V_{TT} must remain within ± 40 mV of V_{REF} under all load and transient conditions. In this application, the circuit generating V_{TT} must be able to sink current when the output buffer (line driver) is at a logic high state as well as source current when the output buffer state is low. While in the current sinking mode, the current through the output inductor is reversed from the normal direction in a buck configuration. In the sinking mode, the switching process is similar to that of a boost converter; however, control circuits of the TPS54672 are designed to function properly in this mode, and the feedback loop compensation network is also not affected. High efficiency is also an important consideration.

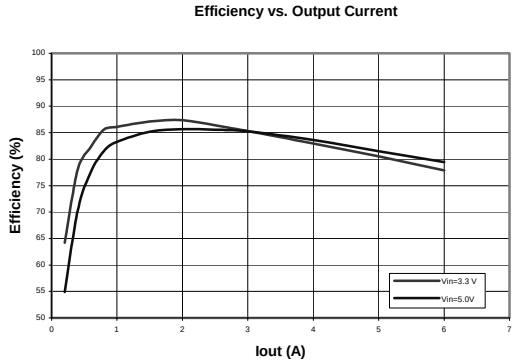

Figure 2. Typical Efficiency

SWIFT is a trademark of Texas Instruments.

Design Considerations

Figure 4 shows the electrical schematic of the TPS54672 V_{TTQ} voltage generation circuit. To generate the reference voltage V_{REF}, a simple resistor divider (R6, R7) is used. To enhance performance, a decoupling capacitor (C12) to V_{SS} is included. To improve symmetry an additional decoupling capacitor to V_{DDQ} can be included.

The output filter is composed of L1, C7, C10, and C11. The inductor L1 is 0.56 µH and was selected to provide the smallest size and to provide for fast transient response. Two low ESR special polymer output filter capacitors are used, based on ± 2 A transients at a slew rate of 10 A/µsec. For increasingly larger transient steps, additional output capacitors may be required, three for ± 3 A, four for ± 6 A. A small ceramic capacitor (C11) is included to reduce the effects of parasitic inductances in the layout and output capacitors.

Capacitors C4 and C10 provide input decoupling to the TPS54672. For proper operation, these parts need to be placed as close as possible to the VIN and PGND pins of the device. In this design C8 is located on the top side, while C4 is placed on the back of the PCB.

Loop Compensation

Besides the output filter, the other important component in achieving good transient response characteristics is the compensation network in the feedback path. The high unity gain bandwidth (3 MHz minimum) and fast slew rate (1.4 V/µsec) of the internal error amplifier permit the use of closed loop crossover frequencies up to 150 kHz. It is important to get maximum gain at frequencies below the crossover frequency to ensure that the regulator is able to react to load transients in the immediately successive switching cycle. Proper placement of the poles and zeros of the type 3 compensation network used in this design allows for a very fast transient recovery time of 5 µsec and a dynamic peak-to-peak voltage change of only 62 mV, lower than the required ± 40 mV. Figure 3 shows the output voltage response to a ± 2 A transient.

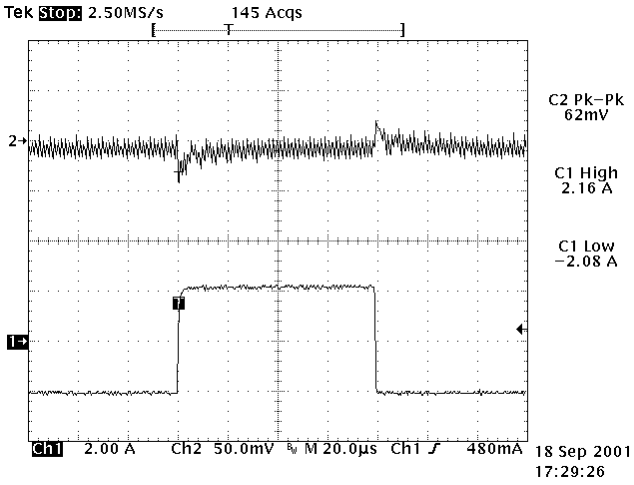

Figure 3. TPS54672 Transient Response

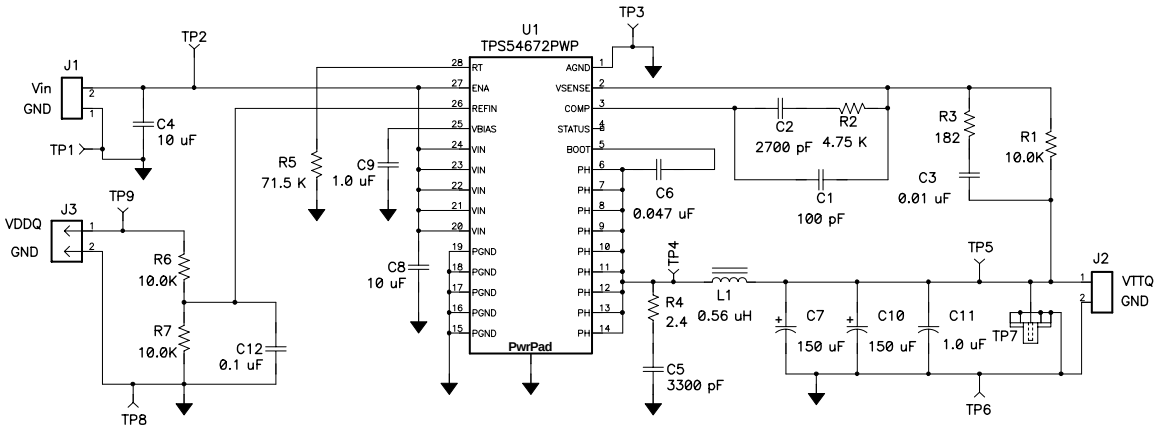

Figure 4. Electrical Schematic of Evaluation Module TPS54672EVM-200

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265