Application Report
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Implementing a Buck Converter With the TPS23753A

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ABSTRACT

The TPS23753A is intended for isolated applications and does not incorporate an internal voltage-regulation error amplifier. Due to its integration and features, it may be advantageous to use the TPS23753A in non-isolated applications. This application report shows additional circuits necessary to implement a low-side switch buck converter using the TPS23753A.

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1 Introduction

The TPS23753A is a combined IEEE 802.3-2008 (or IEEE 802.3at type 1) power over Ethernet (PoE) interface and dc/dc controller for powered devices (PDs). Examples of PDs are VoIP telephones and wireless access points (WAP). The TPS23753A is a part of a family including the TPS23753, TPS23754, TPS23756, and TPS23757. The techniques and solutions discussed also apply to the other members of this family.

Isolation between the Ethernet wiring and all other potentials is required by IEEE 802.3 (functional requirement), and isolation of customer-accessible potentials from the Ethernet wiring is required by the IEC60950 standard (safety). Isolation usually is included to strictly meet the requirements, or for its implied added safety margin in cases where it is uncertain. Some applications are clearly able to meet the requirements without isolation; an example is an active-message sign that did not have any metallic I/O ports besides the Ethernet.

Removing converter input-output isolation is perceived as reducing part count and thus complexity, size, and cost. The flyback topology provides both isolation and duty-cycle (efficiency and stress) advantages. The simple inductor of a buck converter, however, is perceived as being less expensive than the flyback transformer.

This application report shows the necessary external circuits to use the TPS23753A in the inverted buck-converter topology. The buck converter of application report *Practical Guidelines to Designing an EMI-Compliant PoE Powered Device With Non-Isolated DC/DC* (SLUA454) is used as a basis for this design. That application report uses the TPS23750 as the key PD and dc/dc control element. The TPS23753A belongs to the same family; it has the advantage, however, that it works from 12-V supplies and has ORing support, but also has disadvantages in lacking a bias regulator, level translator, and error amplifier.

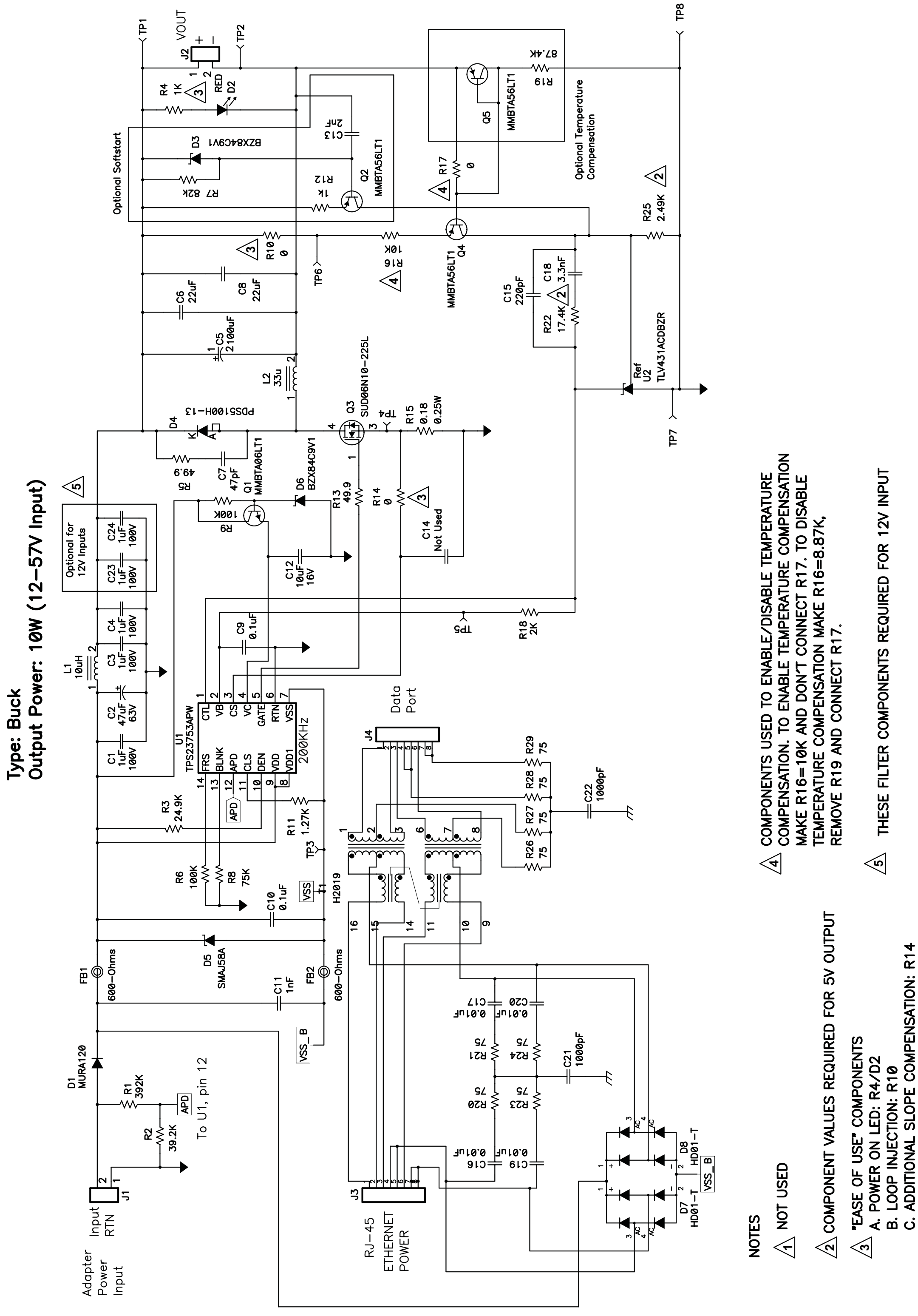
2 Non-Isolated Buck Converter

Figure 1 is the schematic for the TPS23753A Non-Isolated Buck Converter. This 10-W (5 V at 2 A) converter design operates at 200 kHz. It operates in both continuous and discontinuous modes depending on the output loading. The TPS23753A, U1, provides the pulse-width modulation (PWM), primary MOSFET current-sense comparator, and slope compensation for current-mode stability. The TLV431, U2, acts a reference and error amplifier to provide the 5-V output regulation.

Components Q4, Q5, R17, R16, and R19 implement a level shifter that translates the output voltage to a point where it can be compared with the reference voltage internal to U2. This variant of the level shifter features temperature compensation by Q5 and its bias R19. A simplified version consisting of just Q4 and R16 suffices for many implementations. It was tested on this board by removing Q5 and R19, installing R17, and changing R16 to 8.87 kΩ.

Control loop error amplifier and compensation is provided by U2, C15, C18, R22, R25, and R18. This simple circuit implements a type 2 compensator (pole-zero-pole).

A bias supply regulator consisting of R9, Q1, and D9 establishes an 8.5-V bias voltage on V_C. A softstart circuit composed of R7, D3, Q2, R12, and C13 controls the turnon rate, eliminating output voltage overshoot at turnon. All the measurements performed are done using the adapter ORing input.



Type: Buck
Output Power: 10W (12–57V Input)

NOTES

1 NOT USED

2 COMPONENT VALUES REQUIRED FOR 5V OUTPUT

3 "EASE OF USE" COMPONENTS
A. POWER ON LED: R4/D2
B. LOOP INJECTION: R10
C. ADDITIONAL SLOPE COMPENSATION: R14

4 COMPONENTS USED TO ENABLE/DISABLE TEMPERATURE COMPENSATION. TO ENABLE TEMPERATURE COMPENSATION MAKE R16=10K AND DON'T CONNECT R17. TO DISABLE TEMPERATURE COMPENSATION MAKE R16=8.87K, REMOVE R19 AND CONNECT R17.

5 THESE FILTER COMPONENTS REQUIRED FOR 12V INPUT

Figure 1. TPS23753A Non-Isolated Buck Converter Schematic

3 Load Transient Response

Figure 2 shows the transient response of the non-isolated buck converter with an input voltage of 48 V and 200-Hz pulsed load current (I_{LOAD}). The two cases are a 1.2-A to 2-A load step to show continuous conduction mode (CCM) operation and 0.1-A to 0.9-A step to show the behavior of the circuit in and out of discontinuous conduction mode (DCM).

As can be observed, V_{OUT-PP} is 280 mV in CCM and 320 mV in DCM about the desired output voltage for their respective I_{LOAD} changes. When I_{LOAD} steps up (down) V_{OUT} goes down (up) as a result of the ESR and ESL of the output capacitor, power block source impedance, and current-mode operating point. V_{OUT} returns to the regulated value once the feedback loop responds and corrects the perturbation. This also demonstrates the stability of the system in the time domain.

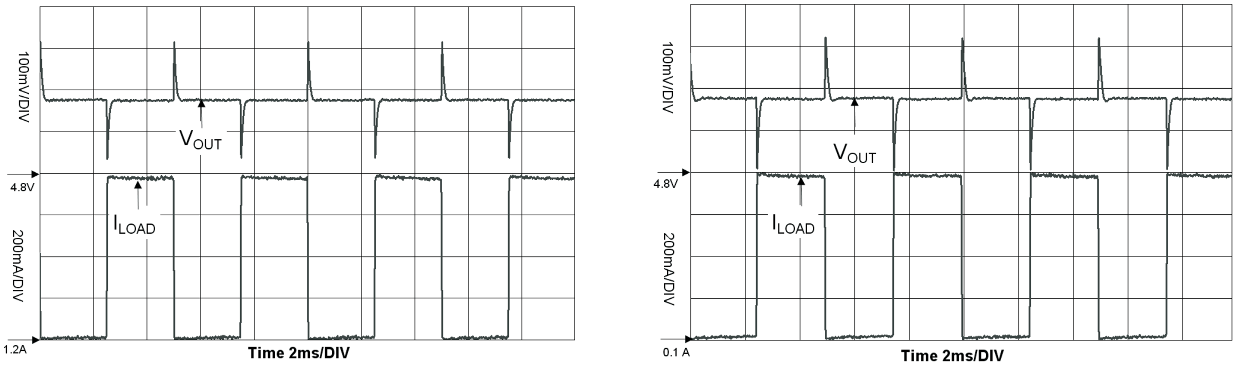


Figure 2. Transient Response

4 Start-Up and Softstart

Figure 3 shows the start-up response for an I_{LOAD} of 2 A on the left side of the figure and without a load (I_{LOAD} equal to 0 A) on the right-side plot. In both cases, the input voltage was 48 V. This test shows the ability of the error amplifier to control the output during start-up and the action of the softstart circuit to avoid overshoots. Systems typically prefer monotonically rising supply voltages to avoid ambiguous states during start-up. With maximum I_{LOAD} and with zero I_{LOAD}, the circuit responds in a similar way and with the same speed (approximately 1 ms). The system has well-controlled start-up with little or no output voltage overshoot.

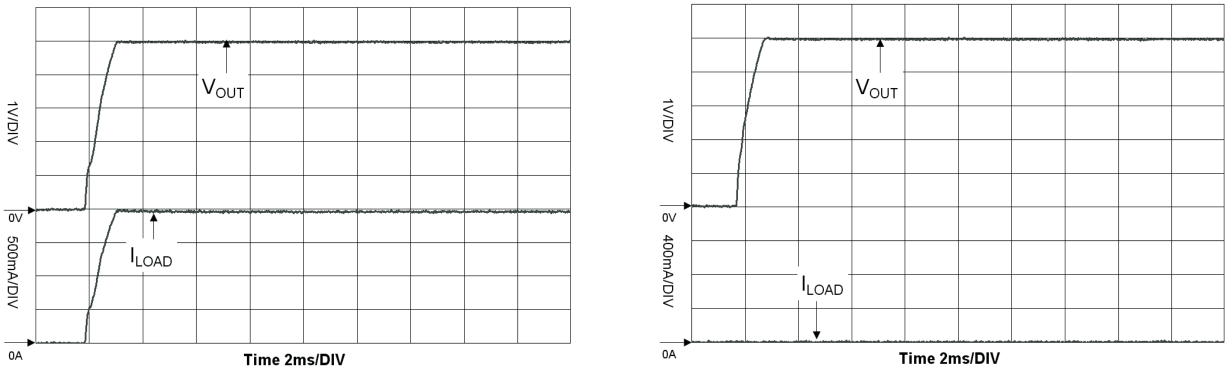


Figure 3. Start-Up

5 Start-Up Without Softstart

Figure 4 shows the start-up response without the softstart circuit. This plot shows the response of the circuit for an I_{LOAD} of 2 A on the left side of the figure and without a load (I_{LOAD} equal to 0 A) on the right-side plot. In both cases, the input voltage was 48 V. It appears feasible to eliminate the softstart circuit to lower costs at the expense of having a small current overshoot during turnon. This eliminates the need for R7, D3, Q2, R12, and C13.

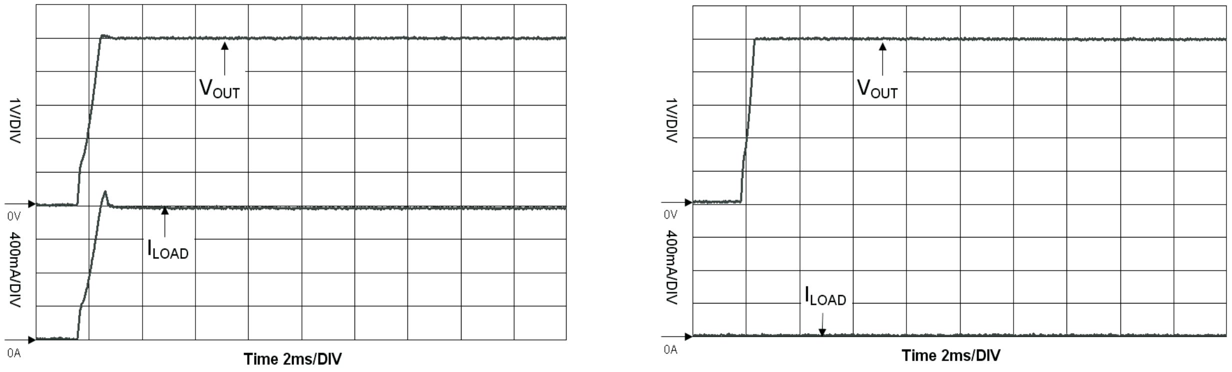


Figure 4. Start-Up With No Softstart Circuit

6 Loop Stability

Figure 5 shows the gain and phase response of the complete system control loop for an input voltage of 48 V and a load current of 1 A. The phase of the system at the gain crossover (0 dB) is used as a measure of relative stability because it is an indication to the designer how far the system is from the oscillation condition. This figure is a complement to the quick stability conclusions that can be made from the step response already presented. In this case, the phase margin was 67.62° and the crossover frequency was 16.5 kHz. This means that the system is stable with a phase margin that is consistent with the step response.

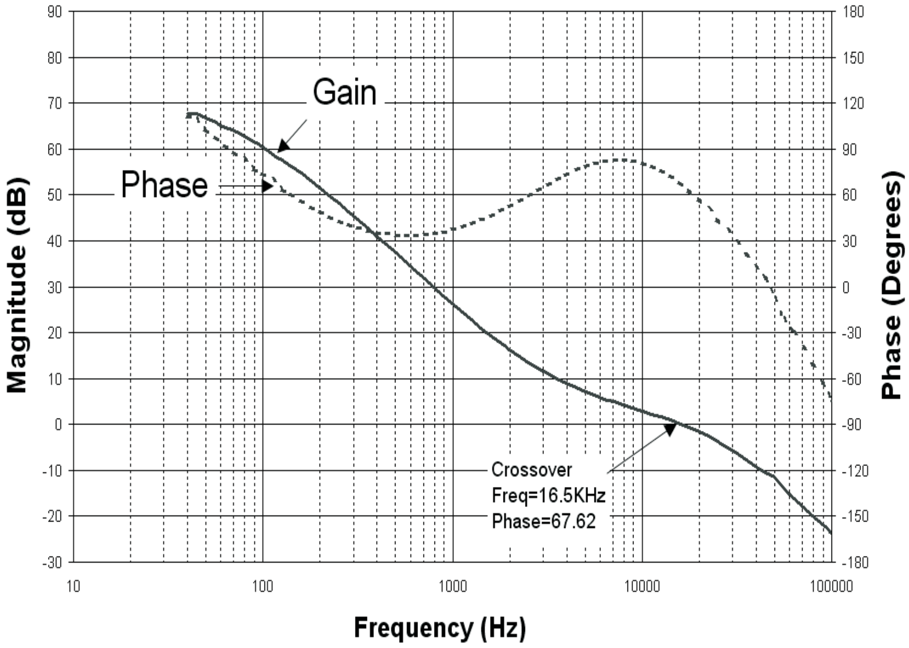


Figure 5. Phase/Gain Response

7 Efficiency

Figure 6 shows the efficiency of the buck converter for different load conditions and input voltages. Efficiency measurements were made for just the converter section, that is, from the adapter input of Figure 1 (J1) (including the ORing diode) to the output.

Efficiency measurements were performed using the temperature-compensated level shifter already mentioned. Additional sources of loss were the output ON LED, and the APD divider. No extraordinary measures were taken to boost the efficiency.

Finally, the efficiency plot for a 12-V input required adding C23 and C24 to prevent the input filter from causing oscillation. This was discovered later in the evaluation as the 12-V operation was not a part of the original plan.

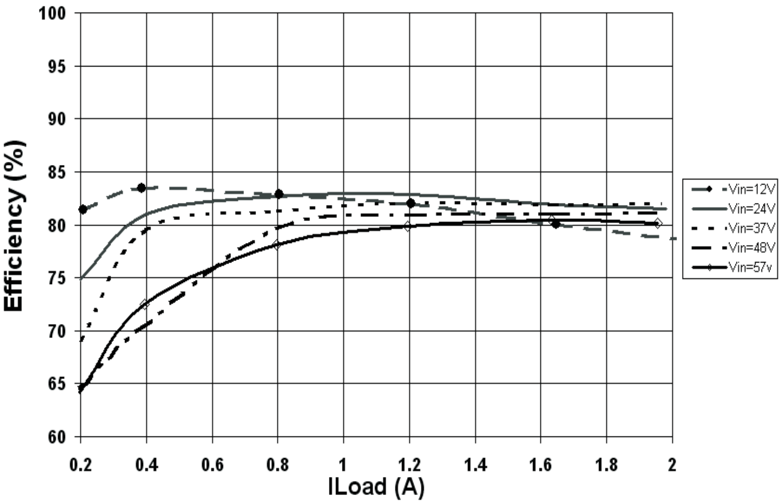


Figure 6. Efficiency

8 Line and Load Regulation

8.1 *Performance With Temperature Compensation Network*

Figure 7 shows the line regulation for an I_{LOAD} of 1 A on the left side of the figure and the load regulation for V_{IN} equal to 48 V on the right side of the figure. Both figures were measured including the temperature-compensated level shifter. The maximum V_{OUT} variation presented while changing V_{IN} was 80 mV (1.6%) for an input voltage range of 12 V to 57 V. This is mainly due to the different currents flowing through R19 which modifies the collector-emitter voltage of Q5 when the input voltage changes.

The V_{OUT} variation with load was only 8 mV (0.16%). This points out that the main source of error is the biasing changes of Q5. Although this may not matter as much over a narrow input range (say 37 V to 57 V), a wide range circuit can benefit from stabilization of the R19 bias current.

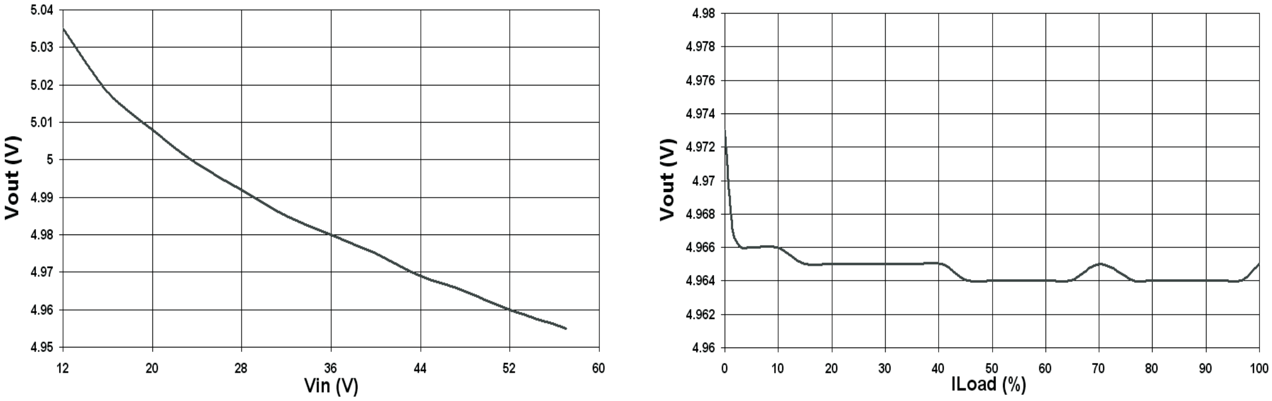


Figure 7. Line/Load Regulation for Temperature-Compensated Circuit

8.2 Performance Without Temperature Compensation Network (Q5)

Figure 8 shows the line regulation for an I_{LOAD} of 1 A on the left-side figure and the load regulation for V_{IN} of 48 V on the right-side figure. Both figures were measured without including the temperature compensation afforded by Q5 and R19. The maximum V_{OUT} variation presented while changing V_{IN} was 29 mV, or about 0.6% over a wide span of 12 V to 57 V. This shows a lower sensitivity to line variations. The output voltage variation with load was 23 mV or about 0.5%.

Because the level shifter is not temperature compensated, the Q4 base-emitter voltage plays a role in the voltage translation from the output of the converter to the input of the control block. This can be seen in the output voltage variation with load, which is almost 3 times larger. The load regulation is most likely due to thermal variations of Q4 (the board heated up with increasing load current). For example, if Q4's V_{BE} varies by 2 mV/°C, an 11°C temperature change can result in the 23-mV output variation observed.

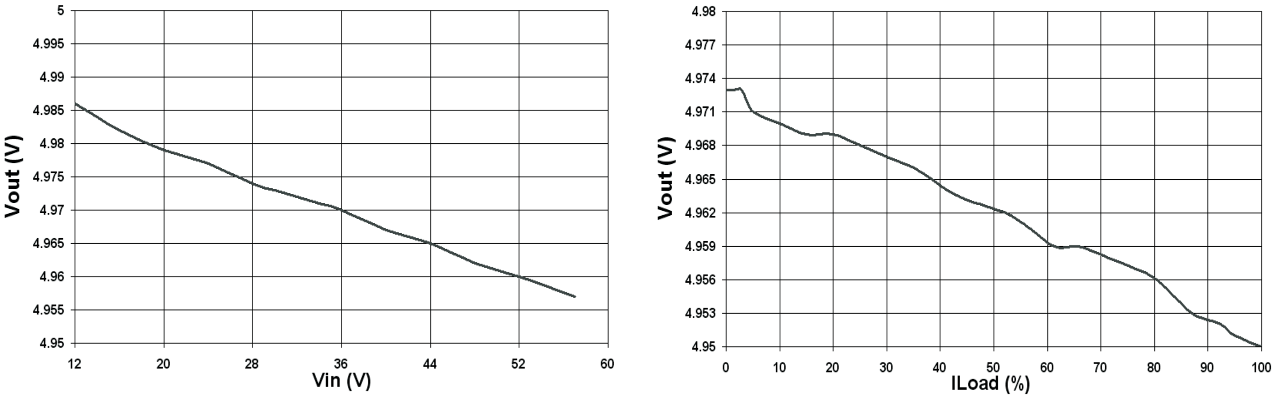


Figure 8. Line/Load Regulation for the Non-Temperature Compensated Circuit

9 Conclusions

This application report demonstrates the design of an inverted buck converter with the TPS23753A as the PoE Interface and dc/dc controller. Circuits for biasing the TPS23753A, translating the output voltage, and implementing an error amplifier are shown. The resulting transient response, turnon, efficiency, line regulation, and load regulation show performance as expected for this type of circuit. Trade-offs in the level shift and softstart features are presented to allow the designer to add/remove the circuits as necessary depending on the desired application.

10 References

1. *Using the TPS23753A (and Family) with an External Error Amplifier* application report (SLVA433)
2. *TPS23753A IEEE 8.2.3 PoE Interface and Converter Controller with Enhanced ESD Immunity* (SLVS933)
3. *TLV431/431A/431B, Low-Voltage Adjustable Precision Shunt Regulator* data sheet (SLVS139)
4. *IEEE Std 802.3at™-2009*, IEEE, 2009
5. *IEC 60950-1, Information Technology Equipment – Safety – Part 1: General Requirements, Second Revision*, IEC, Geneva Switzerland, 2009
6. *Practical Guidelines to Designing an EMI-Compliant, PoE-Powered Device With Non-Isolated DC/DC* application report (SLUA454)

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