TEXAS INSTRUMENTS

Optimizing the TPS62125 Output Filter

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ABSTRACT

The TPS62125 uses a variation of the hysteretic control called DCS-Control[TM]. Use of this control topology allows for a wider range of inductor and output capacitor values to accomplish specific design goals. The designer is able to optimize many factors such as control loop stability, transient response, operation in CCM mode, or output voltage ripple, based on an application's needs. In addition, the use of a feed-forward capacitor can help increase performance. This application report discusses how to choose the output filter for the TPS62125 in order to meet the specific requirements of a design.

1   Analyzing the Stability of the Design

The designer must consider many factors when choosing an inductor and output capacitor combination for any switching regulator. For example, lower inductances can be physically smaller due to fewer windings, which saves board space; however, this causes the peak switch current and output voltage ripple to increase. Larger voltage ripple can be lowered by then using a higher output capacitance if the design can tolerate the larger size and slower transient response.

Stability is a key factor that the inductor and output capacitor values affect. Regardless of what goals need to be met through optimizing the output filter, the design has to be stable. The LC filter forms a double pole in the control loop, which has a strong impact on the frequency response and system stability. Testing shows that both small and large LC combinations can cause instability. Large and small LC combinations translate to low and high corner frequencies, respectively. Equation 1 calculates the corner frequency of the LC filter:

$$f_C = \frac{1}{2\pi\sqrt{LC}}$$ (1)

Table 1 shows the stability of different LC combinations that have been tested with an input voltage of 12 V and a load current of 300mA. All stability measurements were taken at both 3.3-V and 8-V out, and it is shown that there are minor differences between the two output voltages. Though some performance metrics differ between the two output voltages, the stability range shown in Table 1 applies to both output voltages. The corner frequency of every LC combination is calculated using the nominal inductor value and the nominal capacitor value de-rated by 50% to account for DC bias. 6.3-V rated capacitors were used for the 3.3-V output and 16-V rated capacitors were used for the 8-V output.

Nominal Inductance Value	Nominal Ceramic Capacitance Value (effective = 1/2 nominal)					
	4.7µF	10µF	22µF	47µF	100µF	200µF
	Effective Corner Frequencies (in kHz)					
4.7µH	47.9	32.8	22.1	15.1	10.4	7.34
10µH	32.8	22.5	15.2	10.4	7.12	5.03
15µH	26.8	18.4	12.4	8.48	5.81	4.11
22µH	22.1	15.2	10.2	7	4.8	3.39
47µH	15.1	10.4	7	4.79	3.29	2.32
100µH	10.4	7.12	4.8	3.29	2.25	1.59
150µH	8.48	5.81	3.92	2.68	1.84	1.3

	Recommended by the TPS62125 Data sheet
	Stable (within recommended LC corner frequency range)
	Stable (outside recommended LC corner frequency range)
	Unstable

Table 1. Stability vs. Effective LC Corner Frequency

Although the stable combinations in the table satisfy the requirements for control loop stability, certain combinations may not work in every system due to other measures of performance, such as output voltage ripple or load transient response. For more information on control loop measurement procedures, see the application report *How to Measure Control Loop of TPS62130/40/50/60/70 DCS-Control*^{TM} *Devices (SLVA465)*. For more information on determining the stability from the load-step response and Bode plot measurements, see the application report *Simplifying Stability Checks (SLVA381A)*. Using these application reports, the LC filter combinations in Table 1 were determined to be stable by having at least 45 degrees of phase before and at the crossover frequency and having less than 3 rings in the transient response.

2   Optimizing Load Transient Response

The transient (or "load step") response can be optimized for a lower voltage drop or for a faster response. When the load is quickly increased (or "stepped"), the output capacitor supplies the load with current until the regulator reacts to the change and increases its output current. A larger output capacitor provides this current with a smaller amount of output voltage droop; however, a smaller capacitor increases the bandwidth of the device and provides faster response. Figure 1 shows the TPS62125 transient responses from no load to a 300mA load using a (a) 10-µF and (b) 200-µF output capacitor with a 4.7µH inductor at 8-V out. The response with the 200-µF capacitor has approximately 30% less voltage droop but takes almost twice as long to react to the load transient.
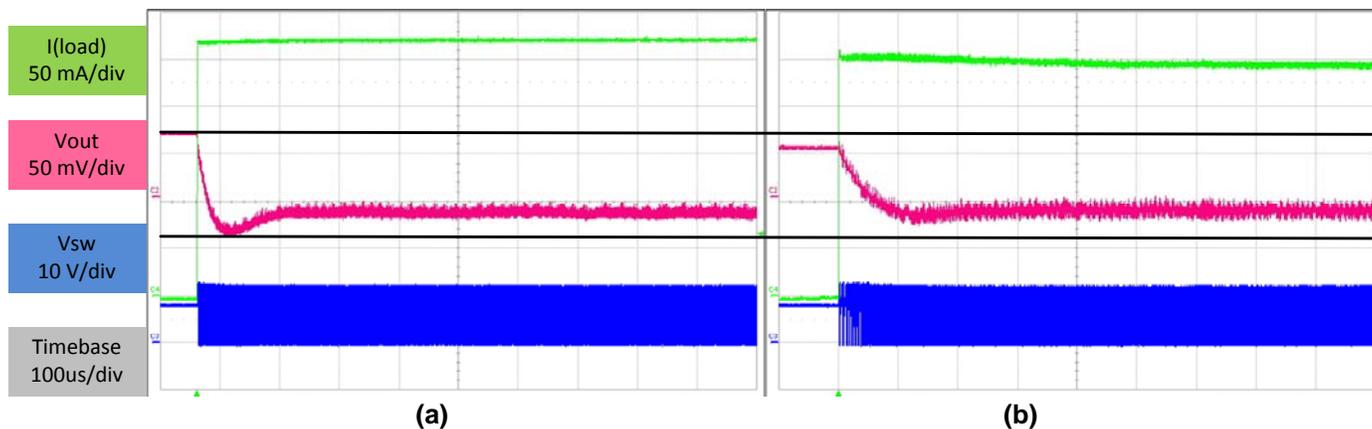
Figure 1. TPS62125 Load transient response using a (a) 10-μF and (b) 200-μF output capacitor

Figure 2 shows the TPS62125 closed-loop frequency response at a load of 300mA and 8-V out verifying the increased bandwidth that yields a faster response. The 10-μF output capacitor gives a bandwidth of 260 kHz as shown in (a) while the 200-μF capacitor gives a 1 kHz bandwidth as shown in (b):
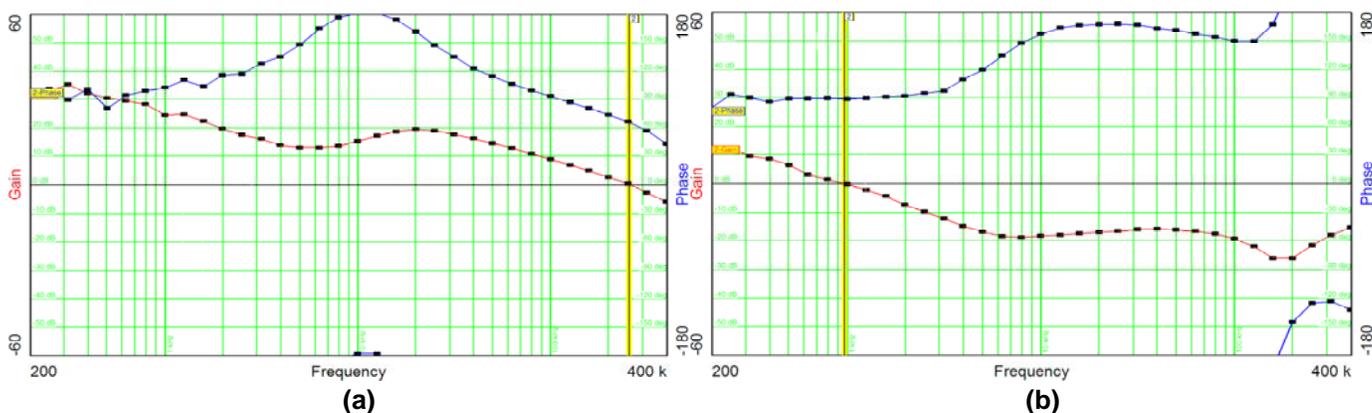

Figure 2. TPS62125 Closed-loop frequency response using a (a) 10-μF and (b) 200-μF output capacitor

3   Ensuring Continuous Conduction Mode (CCM) Operation

DCS-Control[TM] is designed, not only for a seamless transition into power save mode, but also for a low output voltage ripple and noise in power save mode. Because of this, applications that with previous generations of converters would have required operating in CCM mode to achieve the required noise performance can now, with DCS-Control[TM], operate in power save mode and maintain the same output voltage performance while obtaining the benefit of increased efficiency at light loads. For those applications requiring the reduction of the already low ripple in power save mode, more output capacitance can be used to further reduce the power save mode ripple. The effect of increasing the output capacitance within the range of Table 1 is shown in the next section, Reducing Output Voltage Ripple.

If the application requires the constant frequency performance of CCM mode, then Table 1 is also used to size the inductance large enough to maintain inductor current at the lowest system load. In this case, the solution size is larger, transient response slower, and efficiency at higher loads reduced compared to increasing the output capacitance to achieve the desired noise performance. In most cases, the noise in power save mode (DCM) is more than sufficient to meet the application's needs, but if CCM is demanded by the application then it is easy to calculate an inductance that guarantees CCM.

In order for a buck converter to operate in CCM, the inductor current should not reach zero. To do this, first define the circuit parameters of maximum input voltage, output voltage, and minimum load current. Then, use Equations 2 and 3 to determine the minimum inductance that maintains CCM operation at the minimum load:

$$\Delta I_L = \frac{\left(V_{in} - V_{out}\right)}{L} \; x \; \frac{V_{out}}{V_{in}} \; x \; \frac{1}{f_{SW}} \tag{2}$$

$$I_{L,min} = I_{out,min} - \frac{\Delta I_L}{2} \tag{3}$$

As an example, consider a case where the lightest load current that the circuit needs to supply is $I_{out,min} = 50mA$. From Equation 3, the ripple current should not exceed 100mA to keep $I_{L,min}$ above 0. From Figure 22 in the TPS62125 data sheet, the switching frequency with $V_{in} = 12V$ at $V_{out} = 3.3V$ is approximately 650-kHz at a 50-mA output current. Given all these values, Equation 2 is rearranged to solve for L. In this case, the inductance should be at least 37-µH, so the next highest common value of 47-µH would be used.

4   Reducing Output Voltage Ripple

Output voltage ripple can pose a problem to processors that have tight voltage tolerances and systems that are sensitive to power supply noise. The output voltage ripple is approximated using the following equations:

$$\Delta V_{out} = \Delta I_L \; x \; Z_C \tag{4}$$

$$Z_C = R_{ESR} - \frac{j}{2\pi \; x \; f_{SW} \; x \; C} + j \; x \; 2\pi \; x \; L_{ESL} = R_{ESR} + j\left(2\pi \; x \; f_{SW} \; x \; L_{ESL} - \frac{1}{2\pi \; x \; f_{SW} \; x \; C}\right) \tag{5}$$

$$\left|Z_C\right| = \sqrt{R^2_{ESR} + \left(2\pi \; x \; f_{SW} \; x \; L_{ESL} - \frac{1}{2\pi \; x \; f_{SW} \; x \; C}\right)^2} \tag{6}$$

From the equations, there are two ways to reduce the output voltage ripple. One way reduces the amount of ripple current in the inductor; however, if the inductance is already chosen then the other course of action is to reduce the magnitude of the impedance of the capacitor at the switching frequency, Z_C, shown in Equation 6. Because a ceramic capacitor has low ESR and a relatively high resonant frequency, the most effective way to reduce the output voltage ripple is to use a larger capacitance. Although effective, at some point, increasing

the capacitance begins to have a negligible effect due to the impedance from ESR and ESL. Note that ESL varies based on the physical geometry of the capacitor and therefore manufacturer data sheets must be consulted when choosing a capacitor to ensure low impedance at the switching frequency. Placing multiple capacitors of large and small values in parallel is frequently done to achieve low impedance across a wide frequency range. Figure 3 shows the TPS62125 output ripple voltage using a (a) 10-µF and (b) 200-µF output capacitor with a 4.7-µH inductor at 3.3-V out. The ripple with the 200-µF capacitor is significantly less.

(a)   (b)
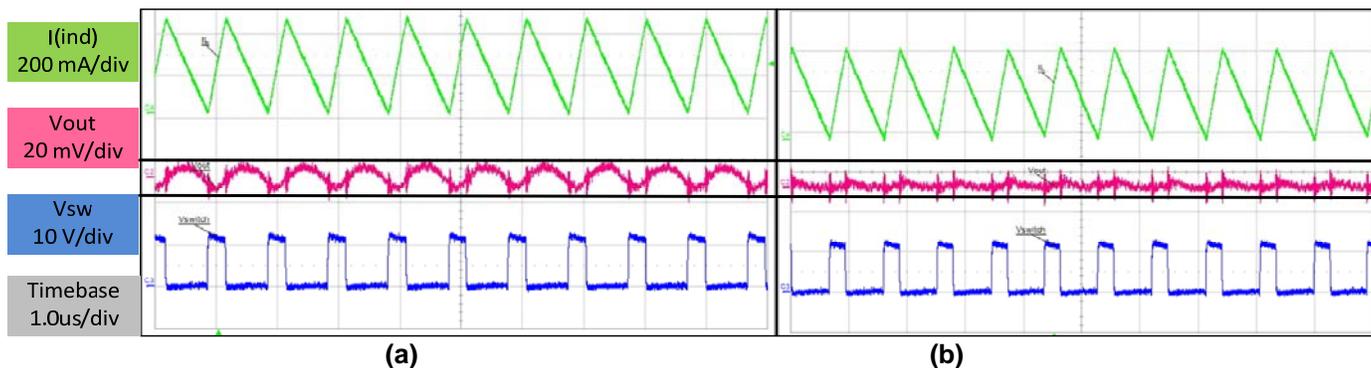
Figure 3. TPS62125 output voltage ripple using a (a) 10-µF and (b) 200-µF output capacitor

5 Extending Bandwidth Using a Feed-Forward Capacitor

Figure 4 shows a typical TPS62125 application circuit. Along with the feedback resistors, R1 and R2, the feed-forward capacitor, C_{ff}, adds a zero and a pole to the closed-loop transfer function of the circuit. When properly located, this boosts the phase so that it reaches a maximum at the geometric mean of the pole and zero frequencies and boosts the gain which gives the circuit higher bandwidth. The application report *Optimizing Transient Response of Internally Compensated DC-DC Converters With Feedforward Capacitor (SLVA289)* details the process of empirically selecting a feed-forward capacitor for an internally compensated converter.
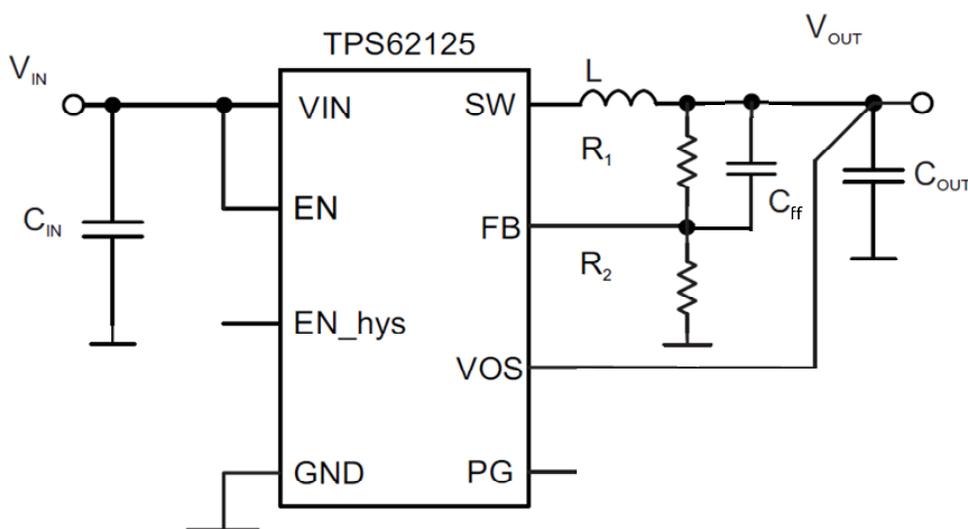
Figure 4. Typical TPS62125 Application Circuit

For optimum stability, C_{ff} selection is a two-step process. First, the crossover frequency without C_{ff} needs to be determined by measuring and analyzing the Bode plot. Once the crossover frequency is determined, Equation 7 is used to calculate the C_{ff} that provides the maximum phase boost at the crossover frequency.

$$C_{ff} = \frac{1}{2\pi \text{ x } f_{noCff}} \text{ x } \sqrt{\frac{1}{R1} \text{ x } \left(\frac{1}{R1} + \frac{1}{R2}\right)} \tag{7}$$

Using the circuit in Figure 4 with a 12-V input voltage, 8-V output voltage, 100-µH inductor, 100-µF output capacitor, 806-kΩ R1 value, and 90.9-kΩ R2 value, the stability and load transient response are analyzed. Figure 5 shows the (a) load-step response with and without the optimally calculated 120-pF C_{ff} (b) closed-loop frequency response without a C_{ff} and (c) closed-loop frequency response with a C_{ff}. The voltage deviation in the load step response is significantly lessened and there is no ringing. The closed-loop bandwidth increased from 5 kHz to 29.6kHz by simply adding the feed-forward capacitor. At the expense of phase margin, a larger C_{ff} can further increase the bandwidth of the device.
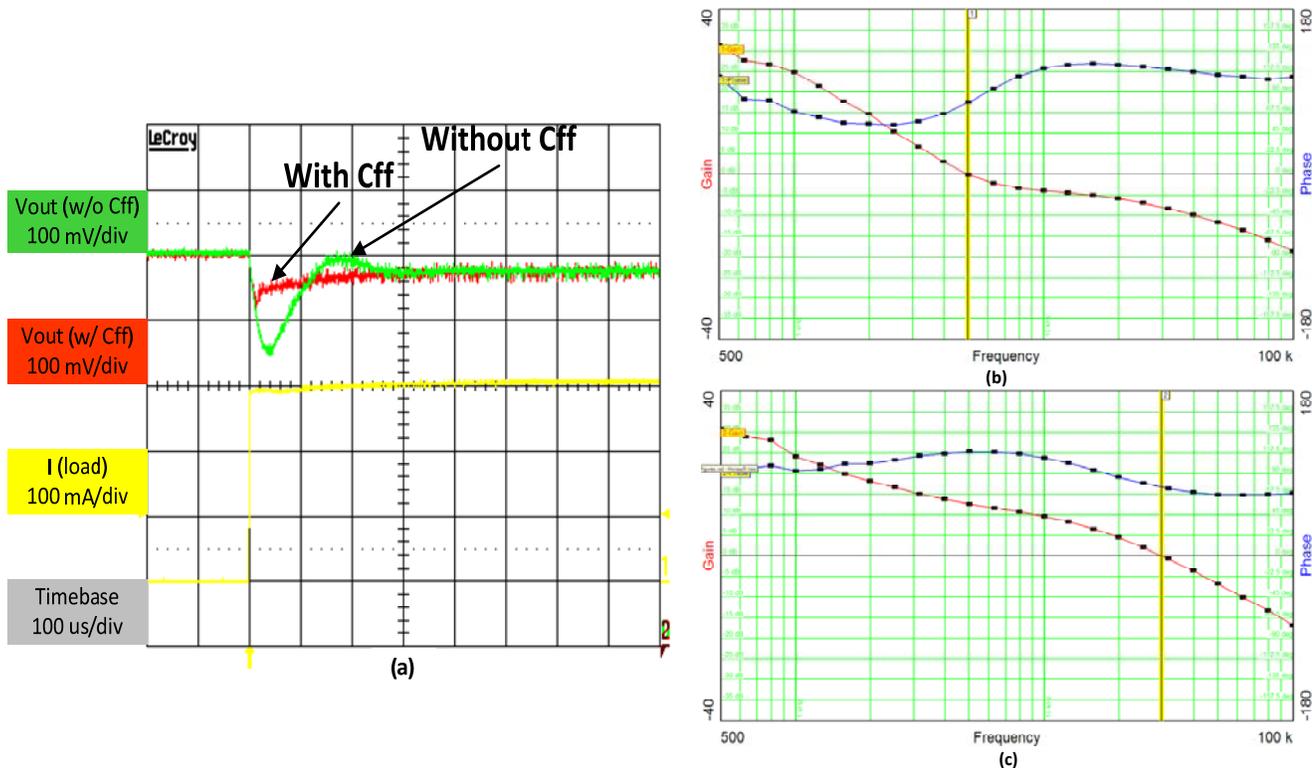
Figure 5. (a) Load Transient Response and (b) Closed-Loop Frequency Response without C_{ff} and (c) with C_{ff} = 120pF

6 Conclusion

This application report has presented methods to analyze control loop stability, optimize transient response, ensure operation in CCM mode, minimize output voltage ripple, and use a feed-forward capacitor to extend bandwidth for the TPS62125 device. The methods presented in the application report, as well as in the references, allow for a wide variety of external components to be used to achieve the desired power supply performance. The benefits and tradeoffs associated with designing the output filter, as discussed in this document, aid with the design of a TPS62125 power supply.

References

1. *Simplifying Stability Checks (SLVA381A)*.
2. *Optimizing Transient Response of Internally Compensated DC-DC Converters With Feedforward Capacitor (SLVA289)*
3. *How to Measure Control Loop of TPS62130/40/50/60/70 DCS-Control^{TM} Devices (SLVA465)*
4. *TPS62125, 3V-17V, 300mA Buck Converter With Adjustable Enable Threshold And Hysteresis (SLVSAQ5)*

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