Application Report
SLVA844B–November 2016–Revised July 2018

PD Alternate Mode: DisplayPort

ABSTRACT

The DisplayPort Alternate Mode allows transmission of native DisplayPort video signals over a USB Type-C cable. The mode is negotiated using USB Power Delivery messaging according to the USB PD specification. This application report explains the implementation of the DisplayPort alternate mode and how it can be used with Texas Instruments TPS6598x family of USB Type-C and USB PD controllers and associated software tools.

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1 Introduction

The USB Power Delivery (PD) Specification defines a standard set of messages for communicating between an upstream-facing port (UFP) and a downstream-facing port (DFP) using a bi-phase marked coding (BMC) modem on a dedicated channel of the USB Type-C cable called the configuration channel (CC). The primary function of these USB PD messages is to negotiate a power contract between the two connected devices, but the USB PD specification also defines a framework for vendors and standards bodies to extend USB PD using alternate modes. Alternate modes may be applied towards a variety of uses, but the most common and powerful functionality is to re-purpose the SuperSpeed differential pairs of the USB Type-C cable from their default USB3 signaling to carry other high-speed signals, such as DisplayPort or Thunderbolt. This allows a single Type-C connector on a device such as a laptop PC to replace many previously-required connectors, and there are already laptop and tablet devices available that have no connector type other than USB Type-C.

The TPS6598x family of USB Type-C and PD Port Controllers offer the highest level of integration available on the market today. These devices contain all of the hardware needed to detect a Type-C port connection, negotiate a PD contract, and route this negotiated power using integrated power switches. These power switches provide over-voltage protection (OVP), under-voltage protection (UVP), over-current protection (OCP) and reverse-current protection (RCP). In addition to this robust power path, the TPS6598x devices support DisplayPort, Thunderbolt (not available on TPS65986) and even user-defined alternate modes, controlling external SuperSpeed multiplexers and re-drivers as needed using GPIO or I2C.

The most common USB PD Alternate Mode is for transmitting DisplayPort video data over the USB Type-C cable. The DisplayPort Alternate Mode can be used by any licensed member of the VESA community, and it uses the VESA DisplayPort Standard ID (SID), 0xFF01. As it was one of the first USB PD Alternate Modes, the PD DisplayPort specification is mature and a copy of the specification can be requested by any employee of a company that is a VESA member.

2 Specifications for the DisplayPort Alternate Mode

The USB PD specification is generalized to allow alternate modes to be defined by any vendor or standards body. USB PD specifies a framework that is common across all alternate modes, including standard messages to discover supported alternate modes and enter and exit alternate modes. USB PD does not define the messages used within the context of an alternate mode, but it does define the two message types that may be used, structured vendor-defined messages (VDMs) and unstructured vendor-defined massages (UVDMs). The VESA specification uses structured VDMs.

This document describes the basic DP Alternate Mode messages, but it is recommended that users of the DisplayPort alternate mode will also study the more detailed VESA DP Alternate Mode specification to fully understand the underlying details.

2.1 USB PD Specification for Alternate Modes

The USB Power Delivery Specification explicitly describes when and how an Alternate Mode may be entered and exited as well as the format of the messages used for Alternate Mode entry and exit. Within the context of the Alternate Mode, however, the PD Specification only defines the structure of message headers. The payload of these VDMs and UVDMs are defined by the vendor's specification for the Alternate Mode. VDM extensions of the DP Alternate Mode are defined in Section 2.2, and further details are provided in the details of the flow of entering and exiting the DP Alternate Mode in Section 4.

Before discussing the basic rules defined by USB PD for alternate modes, it is helpful to begin with a review of some definitions. The terms DFP and UFP are defined in the USB Type-C specification. These terms are often used within the context of USB PD, but may lead to confusion because, unlike a system that supports USB Type-C without USB PD, a USB PD system may be concurrently a data source and a power sink (or vice-versa.) In this context, it is necessary to distinguish between the data DFP, which may also be referred to as the "host," and the power DFP, which may also be referred to as the "source." Likewise, it is necessary to distinguish between the data UFP, also known as the "device," and the power UFP, also known as the "sink."

Some of the relevant rules defined by the USB PD specification for the implementation of alternate modes are as follows:

- Alternate modes may only be entered after the completion of a successful PD Power Negotiation.

- An alternate mode *Enter Mode* request may only be initiated by the Data DFP (Host).
- An alternate mode *Exit Mode* request may only be initiated by the Data DFP (Host).
- An alternate mode is defined by the combination of a Standard or Vendor ID (SVID) and a mode number. Standard and Vendor IDs are assigned by the USB IF. Once a vendor applies for and is assigned a Vendor ID (VID), that vendor may defined as many mode numbers for use in conjunction with this VID as desired.
- The data DFP (host) determines the SVIDs and corresponding modes supported by the UFP by initiating a sequence of *Discover SVIDs* and *Discover Modes* messages that are responded to by the UFP.
- The data DFP my initiate entry into any alternate mode (SVID and mode number pair) that is supported by both the DFP and the UFP.
- Data-role swaps are not allowed while any alternate mode is active (currently entered.)
- A cable disconnect or a PD hard reset implies exit from all currently active alternate modes even though no *Exit Mode* message is sent.

Alternate Modes can be public (open-source), licensable, or proprietary. Because the VESA DP Alternate Mode specification can be licensed but is not open-source, only critical excerpts from the specification will be shown in this document. Refer to the full specification document for more details.

2.2 VESA Specification for the DisplayPort Alternate Mode

The *VESA DisplayPort Alternate Mode on USB Type-C Standard* specification defines the messages that will occur inside the context of the DP Alternate Mode, which is defined by all messages marked with the 0xFF01 SVID. The electrical wiring for different types of products supporting DP over USB Type-C and USB PD connections is also defined within the specification. This wiring is referred to as "Pin Assignment" in the specification, and understanding of these different wiring formats is critical to correctly configuring the TPS6598x device for the underlying hardware. Although the DP Alternate Mode data is fully supported by the TPS6598x devices, mis-configuration of the firmware can result in failed or incorrect DP Alternate Mode entry, ultimately leading to a lack of video on a monitor or TV screen. Understanding the details of the DisplayPort alternate mode specification allows these problems to be resolved in a logical manner to get a system up and running quickly. A basic comparison of the Pin Assignments defined in the VESA DisplayPort alternate mode standard are shown in Table 1. It is worth noting that pin assignments A, C and E utilize all four of the SuperSpeed pairs available in the USB Type-C cable for DisplayPort data, providing the highest available bandwidth. Pin assignments B, D, and F use two SuperSpeed pairs to carry DisplayPort data and the remaining two SuperSpeed pairs to carry USB3 data. These modes are referred to as Multi-Function DisplayPort (MFDP). Though MFDP has a lower DisplayPort bandwidth, it allows an independent USB3 data connection to be made in parallel over a single cable.

Ensuring the schematic matches the DisplayPort specification is critical and may not be resolved by simple FW changes. The system is assumed to be wired correctly as the electrical portion of the DP Alternate Mode specification is outside the scope of this document, and only the PD messaging will be considered. Although knowing the meaning of each bit in the specification is not always necessary, it is worth pointing out that the DisplayPort-related Registers (Capabilities and Status) and PD analyzers of the TPS6598x follow the specification exactly and these similarities can be seen throughout this chapter.

Table 1. DisplayPort DFP_D Receptacle Pin Assignment Summary

Pin Assignment	Cable Type	DisplayPort Signaling	Receptacle Pin Number					
			A11-A10	A2-A3	B11-B10	B2-B3	A8	B8
A	USB Type-C to USB Type-C or Protocol Converter	GEN2_BR	Open/ ML2	ML1	Open/ ML3	ML0	AUX_CH_P	AUX_CH_N
B		GEN2_BR	Open/ ML1	SSTX	SSRX	ML0	AUX_CH_P	AUX_CH_N
C	USB Type-C to USB Type-C or Protocol Converter	DP_BR	ML0	ML2	ML3	ML1	AUX_CH_P	AUX_CH_N
D		DP_BR	ML0	SSTX	SSRX	ML1	AUX_CH_P	AUX_CH_N
E	USB Type-C to DisplayPort (DP)	DP_BR	ML0	ML2	ML3	ML1	AUX_CH_P	AUX_CH_N
F		DP_BR	ML0	SSTX	SSRX	ML1	AUX_CH_P	AUX_CH_N

For the pin assignment Summary of UFP_D Receptacles and the pin assignment Requirements for DFP_D Receptacles, DFP_D Plugs, UFP_D Receptacles, and UFP_D Plugs, refer to the VESA DisplayPort Alternate Mode on USB Type-C Standard documentation.

The terms "DFP" ("Downstream-facing Port") and "UFP" ("Upstream-facing Port") were introduced in section Section 2.1 in the context of USB Type-C and PD. These terms are also used in the VESA DisplayPort Documentation to refer to the source (DFP) and sink (UFP) of DisplayPort data in the system. In order to distinguish the DisplayPort DFP and UFP from the USB Type-C DFP and UFP, the annotations "DFP_D" and "UFP_D" are used by the DisplayPort specification to refer to the DisplayPort source and sink, and the terms "DFP_U" and "UFP_U" are used to refer to the USB Type-C and PD data DFP (host) and data UFP (device.) This document will use this same notation. Note that the "DFP_D" is not necessarily also a "DFP_U" for a given system, so the two configurations must be tracked independently.

The primary objectives of the DisplayPort alternate mode flow are to determine the DisplayPort configurations supported by both connected devices and choose the optimal configuration from those supported on both ends of the connection. This negotiation typically follows these steps:

- Discover SVIDs Request sent by DFP_U
- Discover SVIDs ACK sent by UFP_U, including DisplayPort SVID (0xFF01)
- Discover Modes Request sent by DFP_U, specifying DisplayPort SVID
- Discover Modes ACK sent by UFP_U. This message specifies the configurations supported by the UFP_U.
- Enter Mode Request sent by DFP_U for DisplayPort SVID
- Enter Mode ACK sent by UFP_U

- Status Message Request sent by DFP_U.
- Status Message ACK sent by UFP_U
- DP Configure Request sent by DFP_U
- DP Configure ACK sent by UFP_U
- Status Message sent by UFP_D to update Hot-plug Detect (HPD) status (if appropriate)

The Discover SVIDs and Discover Modes Request and ACK are standard PD messages, with the exception that the Discover Modes ACK sent by the UFP in step replaces the mode value that would normally be returned with the data structure specified in table Table 2. This re-purpose of the 32-bit mode value is possible because there is only one mode defined for the DisplayPort SVID. The advantage of communicating the UFP_U capabilities in the Discover Modes ACK is that it allows the UFP_U to specify its capabilities to the DFP_U without entering the mode. This allows the DFP_U to evaluate whether or not a DisplayPort configuration exists that is supported on both sides and avoid entering the mode if it determines that there are no compatible configurations.

Table 2. DisplayPort Capabilities Message

Bits	Description	Value	Value Description
1:0	Port capability	00	RESERVED
		01	UFP_D-capable (including branch device)
		10	DFP_D-capable (including branch device)
		11	Both DFP_D and UFP_D-capable
5:2	Signaling for transport of DisplayPort protocol	xxx1	Supports DP v1.3 signaling rates and electrical specification (is always be set apart from diagnostic purposes).
		xx1x	Supports USB Gen 2 signaling rate and electrical specification.
		x1xx	RESERVED
		1xxx	RESERVED
6	Receptacle indication	0	DisplayPort interface is presented on a USB Type-C plug
		1	DisplayPort interface is presented on a USB Type-C Receptacle
7	USBr2.0 signaling not used	0	USB r2.0 signaling may be required on A6 – A7 or B6 – B7 while in DisplayPort configuration
		1	USB r2.0 signaling is not required on A6 – A7 or B6 – B7 while in DisplayPort configuration
15:8	DFP_D pin assignments supported if the port is a receptacle. (These fields are instead the UFP_D pin assignments supported when the port is a plug)	00 00 00 00	DFP_D pin assignments are not supported
		xx xx xx x1	pin assignment A is supported
		xx xx xx 1x	pin assignment B is supported
		xx xx x1 xx	pin assignment C is supported
		xx xx 1x xx	pin assignment D is supported
		xx x1 xx xx	pin assignment E is supported
		xx 1x xx xx	pin assignment F is supported
		x1 xx xx xx	RESERVED
		1x xx xx xx	RESERVED
23:16	UFP_D pin assignments supported if the port is a receptacle. (These fields are instead the DFP_D pin assignments supported when the port is a plug.)	00 00 00 00	UFP_D pin assignments are not supported
		xx xx xx x1	pin assignment A is supported
		xx xx xx 1x	pin assignment B is supported
		xx xx x1 xx	pin assignment C is supported
		xx xx 1x xx	pin assignment D is supported
		xx x1 xx xx	pin assignment E is supported
		xx 1x xx xx	RESERVED
		x1 xx xx xx	RESERVED
		1x xx xx xx	RESERVED
31:24	RESERVED	0x00	RESERVED (always 0)

Upon receiving the capabilities of the UFP_U, the DFP_U will attempt to find a match by comparing its own capabilities to those of the UFP_U according to the following criteria:

- (Bit [6]) A valid connection may be made between two receptacles (assumes a cable between the receptacles) or between a plug and a receptacle, where the plug is a captive-cable device such as a dongle. Connections cannot be made between two plugs.
- (Bits [1:0]) When both ends of the connection are receptacles, valid connection must have one DFP_D (DisplayPort source, such as a computer) and one UFP_D (DisplayPort sink, such as a monitor).
- (Bits [1:0]) When one end of the connection is a plug and the other is a receptacle, a valid connection is either a DFP_D plug connected to a DFP_D receptacle or a UFP_D plug connected to a UFP_D receptacle.
- (Bit [2]) The DisplayPort signaling rate must match between DFP_D and UFP_D in order to make any DisplayPort connection (Pin configurations A-F).
- (Bit [3]) The USB signaling rate must match between DFP_D and UFP_D in order to make any MFDP connection (Pin configurations B, D, F)
- (Bits [13:8] and [20:16]) A valid connection must have a common pin assignment between the two ends. Note that bits [13:8] only apply to a connection made if the UFP_U is either a DFP_D receptacle or a UFP_D plug and the bits [20:16] only apply if the UFP_U is either a UFP_D receptacle or a DFP_D plug.

It is important to understand these criteria of a valid DisplayPort connection because most DFP_U devices (including all TPS6598x devices) will only issue an *Enter Mode* request if these criteria are met.

Upon successful entry into the DisplayPort alternate mode the DFP_U must issue a *Status* request. The format of this message's payload is shown in table Table 3. While there is no explicit time limit specified for initiating this request, the following configuration step, which is required to complete the DisplayPort connection, can not be issued until the UFP_U status is received. For this reason, the *Status* request is usually made immediately upon entry into the DisplayPort alternate mode. When making a *Status* request of the UFP_U, the DFP_D will also send its current status.

Table 3. DisplayPort Status Message

Bits	Description	Value	Value Description
1:0	DFD_D/UFP_D connected	00	Neither DFP_D nor UFP_D is connected, or adaptor is disabled
		01	DFP_D is connected
		10	UFP_D is connected
		11	Both DFP_D and UFP_D are connected
2	Power low	0	Adaptor is functioning normally or is disabled
		1	Adaptor has detected low power and disabled DisplayPort support
3	Enabled	0	Adaptor DisplayPort functionality is disabled
		1	Adaptor DisplayPort functionality is enabled and operational
4	Multifunction preferred	0	No preference for multifunction.
		1	Multi-function preferred
5	USB configuration request	0	Maintain current configuration
		1	Request switch to USB configuration (if in DisplayPort configuration).
6	Exit DisplayPort mode request	0	Maintain current mode
		1	Request exit from DisplayPort mode (if in DisplayPort mode)
7	HPD state	0	HPD_Low
		1	HPD_High
8	IRQ_HPD	0	No IRQ_HPD since last status message
		1	IRQ_HPD.e
31:9	RESERVED	0x00 00 00 or 0x00 00 01	RESERVED (always 0)

The two most important fields of the first received status message, which occurs before the configuration step, are the connected bits [1:0] and the multifunction preferred bit [4]. These two fields are used in conjunction with the information received from the capabilities discovered via the *Discover Modes* message to determine the DisplayPort configuration. In order for a valid DisplayPort configuration to be made in a system with two receptacles, there must be both a DFP_D and a UFP_D currently connected as specified in the *Status* in addition to a DFP_D and UFP_D capabilities. In many systems, the connected bits of the *Status* message will exactly match the capabilities of the port, but the DisplayPort standard does allow the connected bits to be dynamically updated.

An example where this might be used is a laptop computer. Generally the output of a laptop computer to a monitor is dynamically configurable and might be enabled or disabled by the user. Such a system could be configured to always advertise the DFP_D capabilities of the laptop's USB Type-C port, regardless of whether or not the user has currently enabled this output, and then dynamically set or clear the connected bits via successive *Status* messages as the user enables or disables the DisplayPort output. This would allow the DisplayPort alternate mode to be entered immediately upon connection, even if the user has not yet enabled the DisplayPort output. DisplayPort connections could then be made and removed, based on user input, without having to exit and re-enter the alternate mode. It should be noted that this dynamic connection management capability is available on the newer TPS65987D and TPS65988 devices, but not on the previous-generation TPS65981, TPS65982 and TPS65986 devices.

In addition to the connected bits, the multifunction preferred bit is used to determine whether a 4-lane DisplayPort-only connection should be made (pin configurations A, C or E) or whether a 2-lane DisplayPort with two lanes of USB3 (MFDP) connection should be made (pin configurations B, D or F) in systems where both are supported.

Assuming that the conditions to form a connection are met, the DFP_U will proceed to the configuration phase by sending a *Configuration* request to the UFP_U. The format of this message's payload is shown in table Table 4.

Table 4. DisplayPort Configuration Message

Bits	Description	Value	Value Description
1:0	Select configuration	00	Set configuration for USB
		01	Set configuration for UFP_U as DFP_D
		10	Set configuration for UFP_U as UFP_D
		11	RESERVED
5:2	Signaling for transport of DisplayPort protocol	0000	Signaling unspecified (used only when *Select Configuration* field is set for USB configuration).
		0001	Select DP v1.3 signaling rates and electrical settings
		0010	Select Gen 2 signaling rates and electrical specifications
		0011 to 1111	All other values are RESERVED
7:6	RESERVED	0	RESERVED (always 0)
15:8	Configure UFP_U with DFP_D pin assignment (assumes UFP_U is a receptacle.)	00 00 00 00	De-select DFP_D pin assignment
		00 00 00 01	Select pin assignment A
		00 00 00 10	Select pin assignment B
		00 00 01 00	Select pin assignment C
		00 00 10 00	Select pin assignment D
		00 01 00 00	Select pin assignment E
		00 10 00 00	Select pin assignment F
		xx xx xx xx	All other values are RESERVED
23:16	Configure UFP_U with UFP_D pin assignment (assumes UFP_U is a receptacle.)	00 00 00 00	De-select UFP_D pin assignments
		00 00 00 01	Select pin assignment A
		00 00 00 10	Select pin assignment B
		00 00 01 00	Select pin assignment C
		00 00 10 00	Select pin assignment D
		00 01 00 00	Select pin assignment E
		xx xx xx xx	All other values are RESERVED

Table 4. DisplayPort Configuration Message (continued)

Bits	Description	Value	Value Description
31:24	RESERVED	0x00	RESERVED (always 0)

The configuration message is the final step in the USB PD DisplayPort alternate mode protocol that is required to form the physical DisplayPort connection between source and sink. This configuration step determines the orientation of the DFP_D (DisplayPort source) and UFP_D (DisplayPort sink), specifies the signaling rates and selects the pin configuration. The DisplayPort DFP_D/UFP_D orientation is specified relative to the USB UFP_U/DFP_U orientation. Allowed values are either "UFP_U as DFP_D," indicating that the USB device will also be DisplayPort source or "UFP_U as UFP_D," indicating . Note that, in the rare case that both connection orientations are possible, TPS6598x firmware will align the orientation of USB and DisplayPort by selecting "UFP_U as UFP_D."

The configuration message also selects the pin assignment. In cases where more than one pin assignment is matched between the DFP_D and UFP_D, the following priorities are applied:

- E/F pin configurations have priority over C/D pin configurations, which have priority over A/B configurations
- If "multifunction preferred" is set on either the DFP_D or the UFP_D, then B/D/F pin configurations have priority over A/C/E. Otherwise, the A/C/E pin configurations have priority.

Unlike the capabilities and status messages, which allow multiple pin assignments to be specified according to the capabilities of the port, only one pin configuration may be selected in the configuration message.

3 DisplayPort Alternate Mode Capabilities Host Interface Registers

The following configuration registers affect the negotiation and behavior of the DisplayPort alternate mode on TPS65981, TPS65982, TPS65986, TPS65987D and TPS65988 devices:

- 0x38, Alternate Mode entry sequence
- 0x47, TX identity data objects
- 0x51, DisplayPort capabilities
- 0x5C, GPIO event map

The USB PD DisplayPort capabilities are configured using the TPS6598x Configuration Tool. The majority of settings that are specific to the DisplayPort alternate mode are set in the DisplayPort capabilities register (0x51), which configures the USB PD-specific settings, and the GPIO event map register (0x5C), which is used to drive an external SuperSpeed multiplexer device as well as the DisplayPort Hot-Plug Detect (HPD) signal. The remaining registers set various system settings that can have an indirect effect on the DisplayPort alternate mode. The Alternate Mode Entry Sequence register (0x38) is used to specify the priority order of mutually exclusive alternate modes. Because both DisplayPort and Thunderbolt use the SuperSpeed pairs of the Type-C cable, only one of these alternate modes can be entered at a time. Users should confirm that the DisplayPort SVID (0xFF01) and mode number (1) are entered in the Alternate Mode Entry Sequence register. For more information on this register and its usage, please refer to the TPS65981, TPS65982, TPS65986 Host Interface TRM or TPS65987D Host Interface TRM as appropriate. It is also important to verify that the "modal operation supported" bit is set in the Transmit Identity Data Objects register (0x47) because some DFP_U devices may not initiate an alternate mode discovery sequence if this bit is not set in the response to a *Discover Identity* request.

The DisplayPort Capabilties (0x51) and GPIO Event Map (0x5C) registers are far more involved and application specific in their settings, so two application examples will be studied in detail. The first is a DFP_D (DisplayPort Source) with an external TUSB10646 USB Type-C DisplayPort 10 Gbps Linear Redriver Crosspoint Switch. The second is a UFP_D (DisplayPort Sink) with an external HD3SS460 USB Type-C 5 Gbps 4x6 Differential Switch. First the configuration of the DisplayPort Capabilties (0x51) and GPIO Event Map (0x5C) registers will be reviewed for each example, and then the LeCroy PD Analyzer trace will be analyzed for the connection of these two systems to each other.

3.1 DFP_D with TUSB1046 Settings

The TPS6598x Configuration Tool is used to generate the "App Config" configuration data table that is prepended to the firmware or patch. Figure 1 shows the configuration of the DisplayPort Capabilities register for the DFP_D DisplayPort Source used in this example. This screen capture is taken for the configuration of a TPS65987D device. For TPS65981, TPS65982 and TPS65986 devices, the DisplayPort Capabilities register contains a subset of these fields. Specifically, the TPS65981, TPS65982 and TPS65986 do not have the "Preferred DP Role," "Force USB Connection" or "DFP_D / UFP_D Connected" bits, which are used for dynamic reconfiguration of the DisplayPort alternate mode at run time. The TPS65981, TPS65982 and TPS65986 devices support the same static configuration capabilities as the TPS65987D, but the TPS65987D provides the additional capability to support these dynamic reconfiguration capabilities.

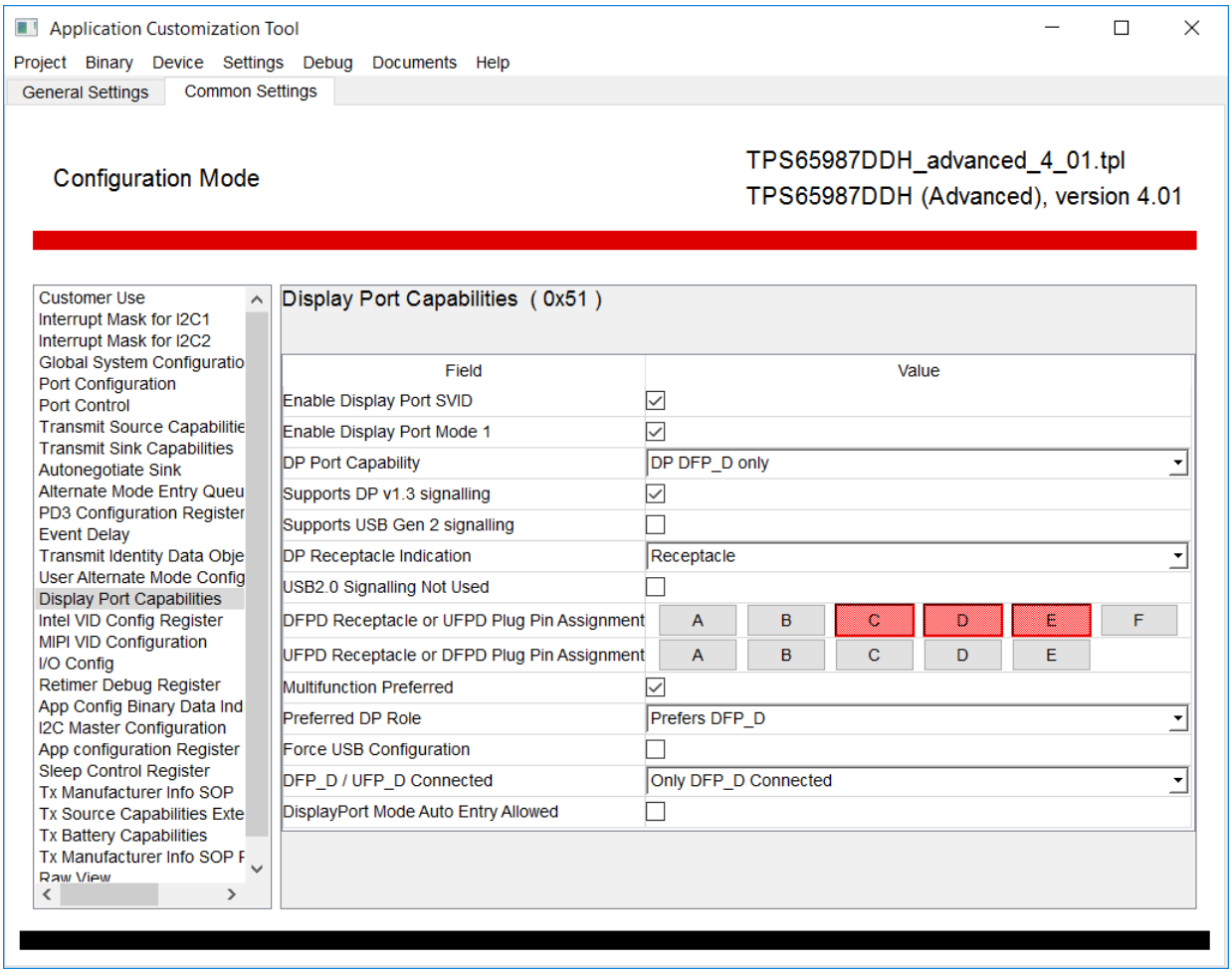

Figure 1. DisplayPort Capabilities Register of example DFP_D

The "Enable Display Port SID" and "Enable Display Port Mode" settings must be set for the Display Port alternate mode to be entered. The next seven fields of the DisplayPort Configuration Register ("Port Capabilities" through "UFPD Receptacle or DFPD Plug Pin Assignment") are a direct one-to-one copy of the Display Port Capabilities message as shown in table Table 2, as defined by the VESA DisplayPort Alternate Mode on USB Type-C Standard. Refer to section Section 2.2 for the details of the individual fields in this message. The remaining fields correspond to fields [1:0] (DFP_D/UFP_D Connected), [4] (Multifunction Preferred) and [5] (Force USB Connection) of the *DisplayPort Status* message Table 3. In most cases, the DFP_D/UFP_D Connected bits are set to match the value specified in the "Port

Capability" setting of this same register. Note that the "Connected" bits must always be an exact match or a subset of the "Port Capability" setting. It is not allowed for the device to indicate a connection exists for a port type that it did not previously specify in its capabilities. The values configured in the DisplayPort Configuration register correspond directly to the values that will be set in the corresponding USB PD messages.

Figure 2 shows the GPIO Event Map register (0x5C) settings used to drive the TUSB1046 Crosspoint Switch. There are two commonly-used sets of GPIO signals used to drive DisplayPort multiplexer devices. The TUSB1046 and HD3SS460 were chosen for the two examples studied in this document because they represent these two sets. Must multiplexer devices suited to this application should be configurable using one or the other of these signal sets. Note that in addition to the three GPIO events used to drive the TUSB1046, GPIO #3 is mapped as the DisplayPort Hot-Plug Detect signal for Port 0. This is not actually a GPIO event, but rather dedicated hardware that exists on the device that is multiplexed onto the same physical pin as GPIO #3. For the TPS65981, TPS65982 and TPS65986 devices, similar hardware exists but is multiplexed onto the same physical pin as GPIO #4.

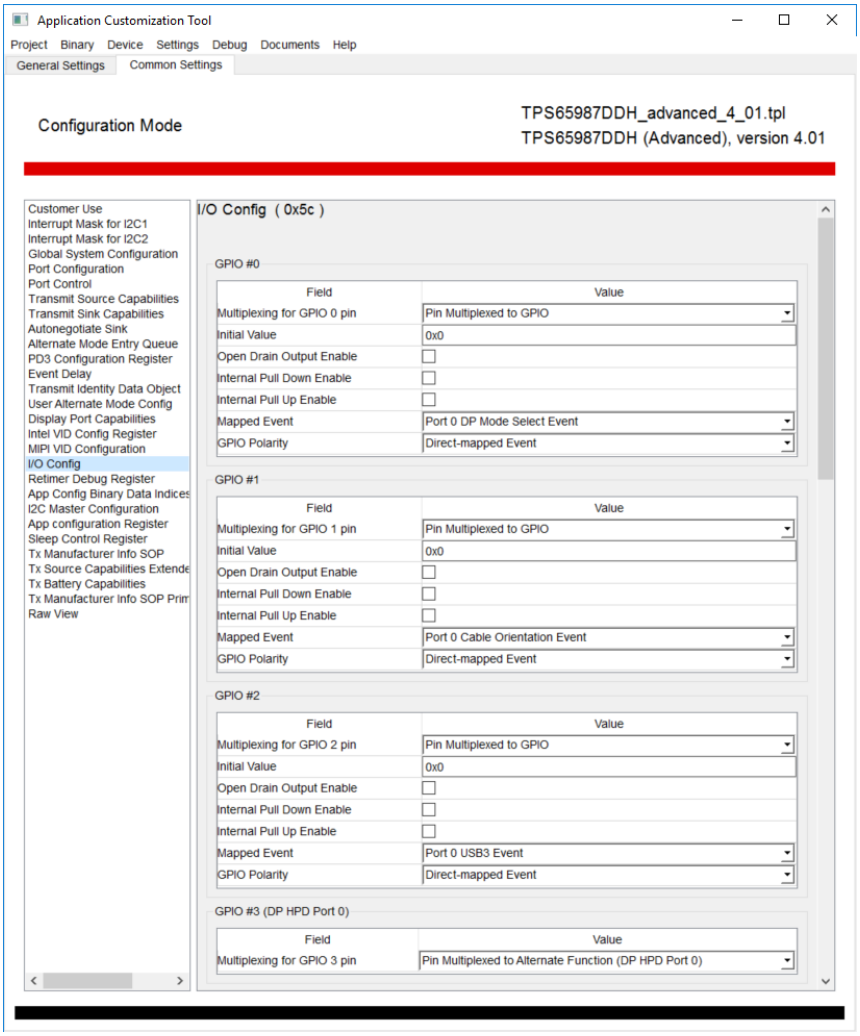

Figure 2. GPIO Event Map Register of example DFP_D with external TUSB1046

The examples studied in this document are configured for a system that supports DisplayPort but does not support Thunderbolt. Note that Thunderbolt controllers such as Alpine Ridge and Titan Ridge also support DisplayPort. The settings discussed in this application note are all applicable to these Thunderbolt systems as well, except that the three GPIO used to control the TUSB1046 or HD3SS460 multiplexers are not needed as this information is instead communicated to the Thunderbolt controller over I2C. In some cases, the HPD signal is not required either as the Titan Ridge controller is capable of supporting a virtual HPD signal that is also communicated over I2C. For more information on Thunderbolt systems, please refer to the application note PD Alternate Mode: Thunderbolt.

3.2 UFP_D with HD3SS460 Settings

Figure Figure 3 shows the configuration of the DisplayPort Capabilities register for the UFP_D DisplayPort Sink used in this example. As with the DFP_D configuration, these settings map directly to the *DisplayPort Capabilties* and *DisplayPort Status* messages that will be sent from the device and must be configured to match the characteristics of the underlying hardware.

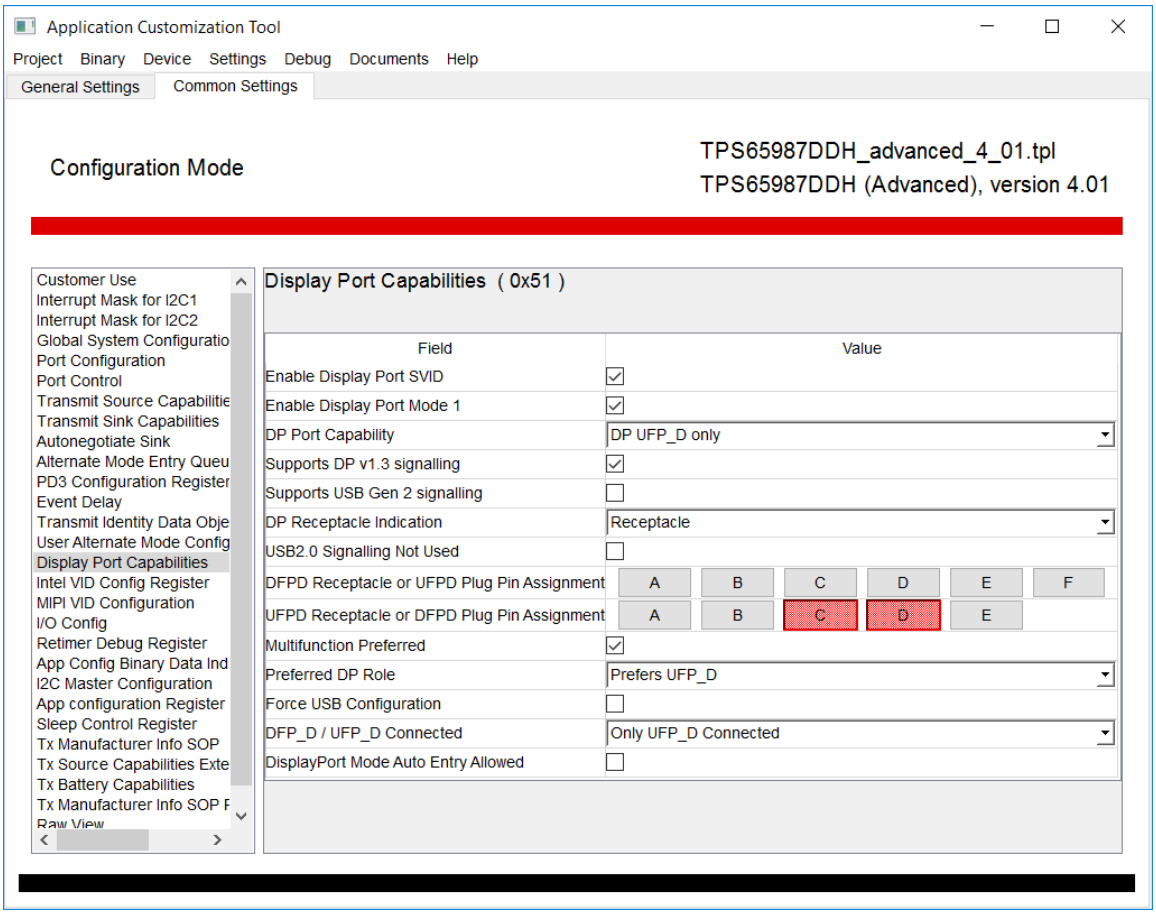

Figure 3. DisplayPort Capabilities Register of example UFP_D

Figure 4 shows the I/O Configurations register (0x5C) settings used to control the HD3SS460 4x6 Differential Switch.

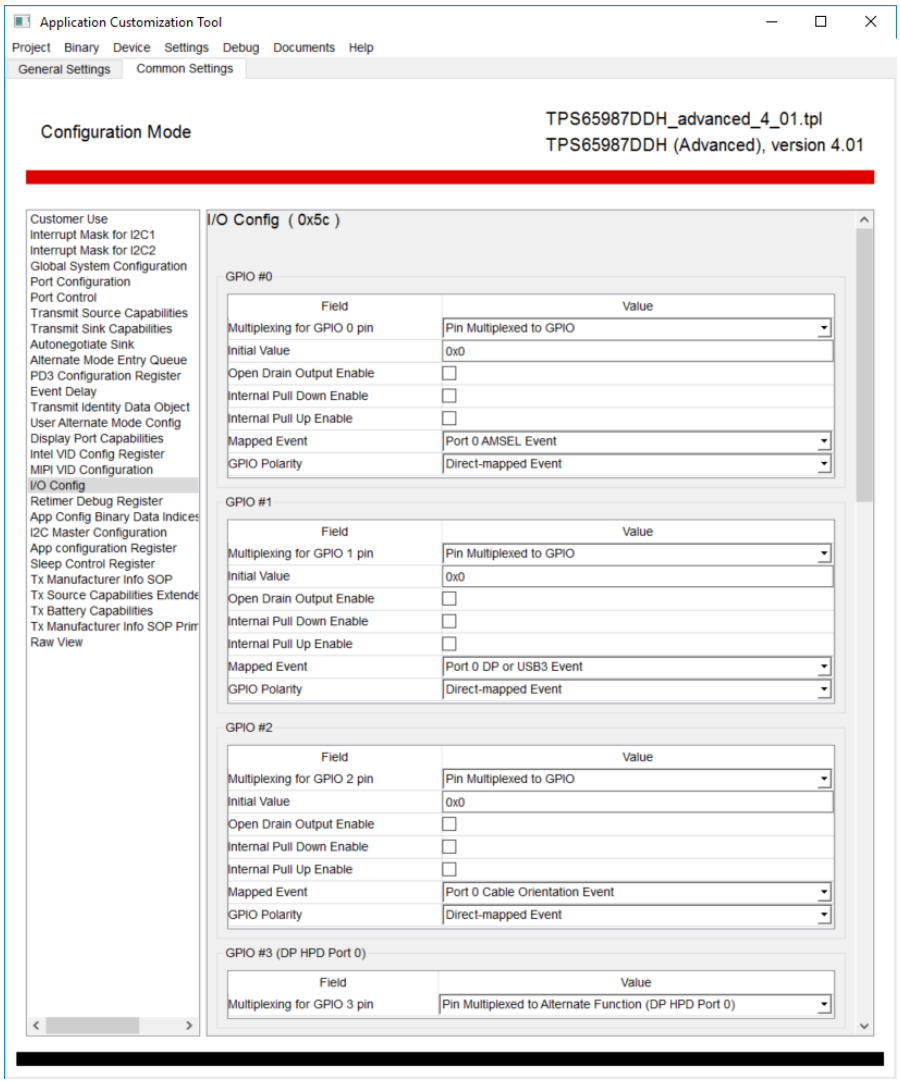

Figure 4. GPIO Event Map Register of example UFP_D with external HD3SS460

4 USB PD and VESA DP Alternate Mode Flow

Figure 5 shows the official state diagram of entry to any VDM Mode (including DisplayPort) according to the USB Power Delivery Specification.

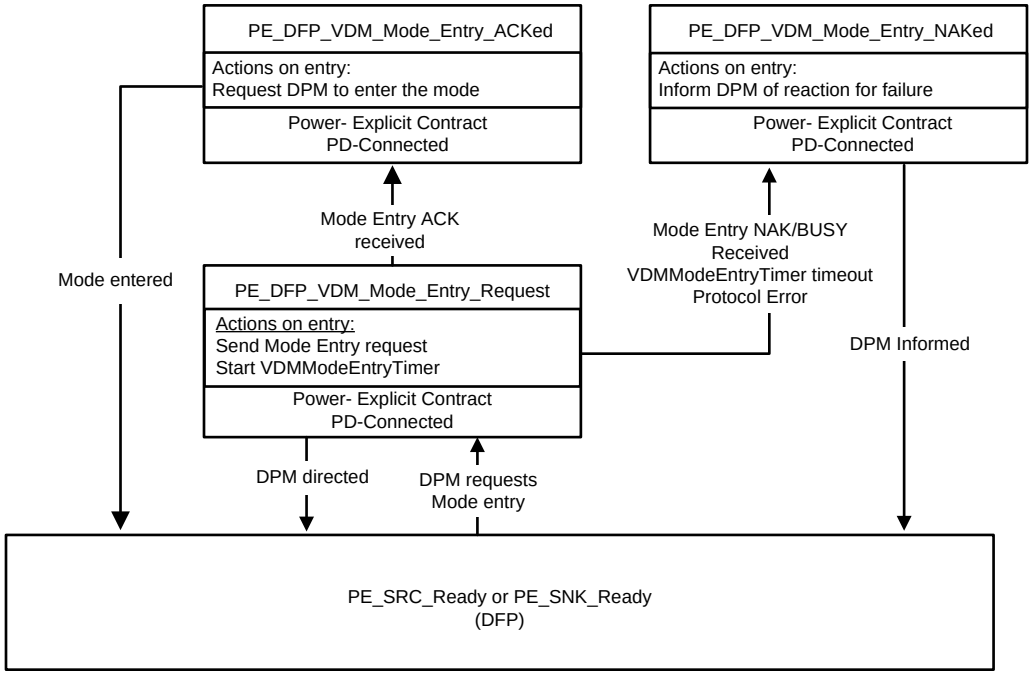

Figure 5. Successful Alternate Mode Entry State Diagram from USB PD Specification

The flow diagram (Figure 5) for entering VDM Modes (Alternate Modes) appears complex, but remember that it is within the context of power negotiations and other types of PD messages. For simplicity, the steps to enter the DisplayPort Alternate Mode within the USB PD specification are shown in Step 1 through Step 8 of the DisplayPort PD negotiation steps that follow. The VESA DisplayPort Specification adds five more unique DP Alternate Mode steps to that are common to the flow for simple configuration.

For simplicity, this application report assumes the following: all CRC calculations are correct, no missing PD packets have been sent, and every message is responded to with a GoodCRC. The PD analyzer used in Section 4.1 hides GoodCRC responses but they are still recorded and saved. All commands sent from the DFP are assumed to be responded to with an ACK signal by the UFP, as opposed to a NAK or BUSY signal.

The resulting list is a total of 13 PD messages plus 13 GoodCRC responses (hidden) required to successfully enter (USB PD) and configure (VESA DP) the DisplayPort Alternate Mode under normal circumstances which are listed as follows:

Step 1. The DFP sends a *Discover Identity* command message to discover the product at the far-end of the Type-C cable.

Step 2. The UFP responds with the *Discover Identity* acknowledgement response, the *TX Identity* message, copied from register 0x47, built by the policy engine and transmitted through the PHY.

Step 3. The DFP detects and sends a *Discover SVIDs* command message to determine alternate modes supported by the product at the far-end of the Type-C cable.

Step 4. The UFP responds with the *Discover SVIDs* acknowledgement response, a list of all SVIDs required for Alternate Modes enabled in the TPS6987D device. In this example, only the DisplayPort (SVID = 0xFF01) is supported.

Step 5. The DFP sends a *Discover Modes* command message to determine alternate modes supported by the product for a given SVID. When the TPS65987D device is used in both products, the first SVID and Mode combination supported by both the DFP and UFP in the Alternate Mode Auto-Entry Sequence register (0x38) of the DFP is the first Alternate Mode

that will be entered.

Step 6. The UFP responds with the *Discover Modes* acknowledgement response, a list of all Alternate Modes enabled in the TPS6987D device. In this example, only DisplayPort Mode 1 is supported.

Step 7. The DFP sends a *Enter Mode* command message, combining the SVID and Mode number along with any payload data defined by the vendor for that SVID-Mode combination.

Step 8. The UFP responds with the *Enter Mode* acknowledgement response, along with any payload data defined by the vendor for that SVID-Mode combination.

Step 9. The DFP_D sends a *DP Capabilities* command message to determine the capabilities of the UFP_D connected.

Step 10. The UFP_D responds with the *DP Capabilities* acknowledgement message, where the payload confirms to the VESA DP Alternate Mode specification, copied from register 0x51, built by the policy engine and transmitted Thevia the PHY.

Step 11. The DFP_D examines the DP capabilities of the UFP_D and selects the configuration that is a best match for the two products (if any). If the two products are compatible, the DFP_D sends a *DP Configure* command message to configure the UFP_D and prepare both products for DP video data.

- At this time, the TPS65987D device on both sides sets the GPIOs correctly to enable the correct paths of the SuperSpeed multiplexer.
- If the products are not compatible, the TPS65987D device acting as the DFP_D automatically sends the *Exit Mode PD* command message to resume normal DFP and UFP data roles.

Step 12. The UFP_D responds with the *DP Configure* acknowledgement message where the payload confirms to the VESA DP Alternate Mode specification, built by the policy engine and transmitted through the PHY.

Step 13. When applicable, the UFP_D will send a self-initiated *Attention* message, telling the host about updates to the DP video status that the DFP_D must know to react appropriately. The most common change in DP video status is toggling the IRQ bit from 0 to 1, which will be sent when the HPD Rx signal at the UFP_D has been active for the minimum amount of time defined in the VESA DP specification.

- The *Attention* message with IRQ set to 1 is the end of USB PD DP Alternate Mode communication and the beginning of legacy DP operation, where DP signals are now mapped correctly to Type-C cable connections

4.1 PD Analysis of DisplayPort Alternate Mode Entry Flow

Referring to the steps listed in Section 4, this section analyzes an actual PD trace of a DisplayPort Alternate Mode entry or configuration sequence captured between two TPS65987D-EVMs to verify if it is successful.

The PD message trace shown in Figure 6 was taken with a Teledyne LeCroy PD analyzer between two TPS65987D-EVMs, one loaded with a binary created from the DFP example outlined in section Section 3.1 and the other loaded with the UFP example of section Section 3.2.

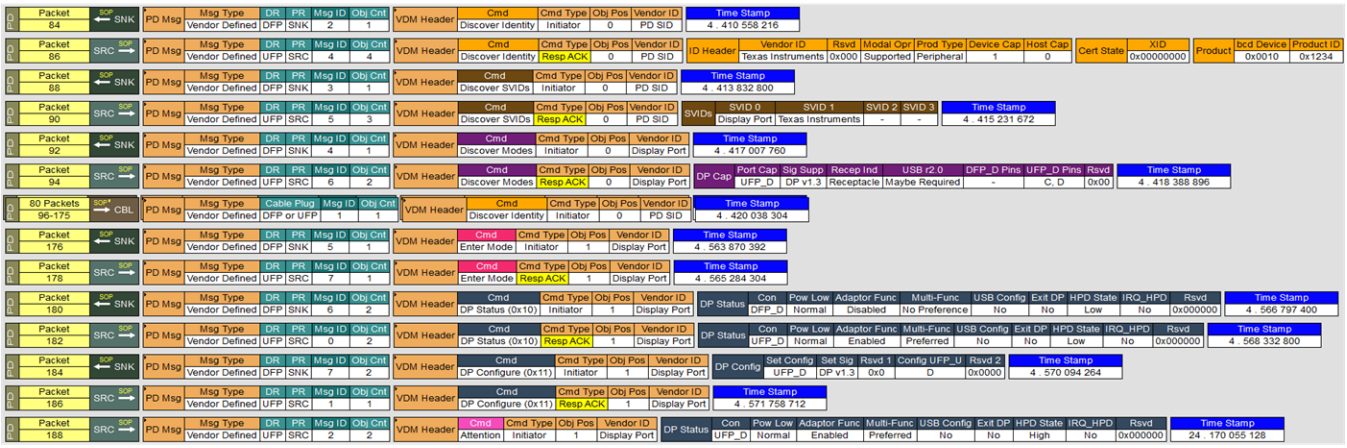

Figure 6. PD Trace of Successful DisplayPort Alternate Mode Entry

Figure 6 shows the expected sequence of PD messages for this example and provides specific details on the 26 steps introduced in Section 4:

1. Packet 84—The DFP sends the *Discover Identity* command message
2. Packet 86—The UFP sends the *Discover Identity* acknowledgment response
3. Packet 88—The DFP sends the *Discover SVIDs* command message
4. Packet 90—The UFP sends the *Discover SVIDs* acknowledgment response
5. Packet 92—The DFP sends the *Discover Modes* command message
6. Packet 94—The UFP sends the *Discover Modes* acknowledgment response
   - Packets 96-175—DFP attempts to communicate to Type-C cable, but the cable used is not e-marked so it cannot respond; the DFP times out and moves on to the next message
7. Packet 176—The DFP sends the *Enter Mode* command message
8. Packet 178—The UFP sends the *Enter Mode* acknowledgment response
9. Packet 180—The DFP_D sends the *DP Capabilities* command message
10. Packet 182—The UFP_D sends the *DP Capabilities* acknowledgment message
11. Packet 184—The DFP_D sends the *DP Configure* command message
12. Packet 186—The UFP_D sends the *DP Configure* acknowledgment message
13. Packet 188—The UFP_D sends the self-initiated *Attention* message

5 DisplayPort Status Registers and 4CC Commands

The preceding section explains how a PD analyzer can be used to confirm that a successful PD power negotiation has occurred, but this information can also be extracted from the host interface registers of the TPS65987D.

- Status registers:
  - 0x5F, Data Status
  - 0x58, DisplayPort Status
- 4CC PD commands (sent to CMD1/2 after populating necessary data in DATA1/2):

- HRST, PD Hard Reset
- AMEn, Alternate Mode Enter
- AMEx, Alternate Mode Exit
- VDMs, Vendor-Defined Message send

Reading the previously listed registers gives an indication of the DisplayPort Alternate Mode entry or configuration sequence that occurred, even if a USB PD analyzer is unavailable in a lab. In addition to configure a system and flash this configuration to a SPI flash device, the TPS6598x Configuration Tool has a debug mode for reading and writing registers and issuing host interface commands over I^2C . This provides a low-cost way to analyze, debug, and test the DisplayPort capabilities of a real system.

The Data Status register (0x5F) provides an overview of the various protocols that utilize the SuperSpeed pairs of the USB Type-C cable. While this register provides much less information about the DisplayPort connection than the DisplayPort Status (0x58) register, it is a good place to start when analyzing the alternate modes of the system. Figure 7, is the read of the Data Status register on the DFP_D side. It shows that USB3 is active on two of the four SuperSpeed data pairs, that Display Port is active, that the device that was read is the DFP_D, and that it is in either C or D pin configuration. Since USB3.1 is shown as active, this is the D pin configuration in which two SuperSpeed data pairs are used for USB 3.1 and two are used for DisplayPort, providing up to 2K resolution. If the USB3.1 were shown as inactive, this would be pin configuration C, in which all four SuperSpeed pairs are used for Display Port, providing up to 4K resolution. Finally, the Data Status register shows that ThunderBolt Mode is not entered. Thunderbolt cannot be entered at the same time as the DisplayPort Alternate Mode because Thunderbolt requires all four of the SuperSpeed pairs.

All bits in this register will be the same for the UFP_D, except that *ConnectionOrient* may change depending on the orientation in which the Type-C cable is plugged into the DFP_U device.

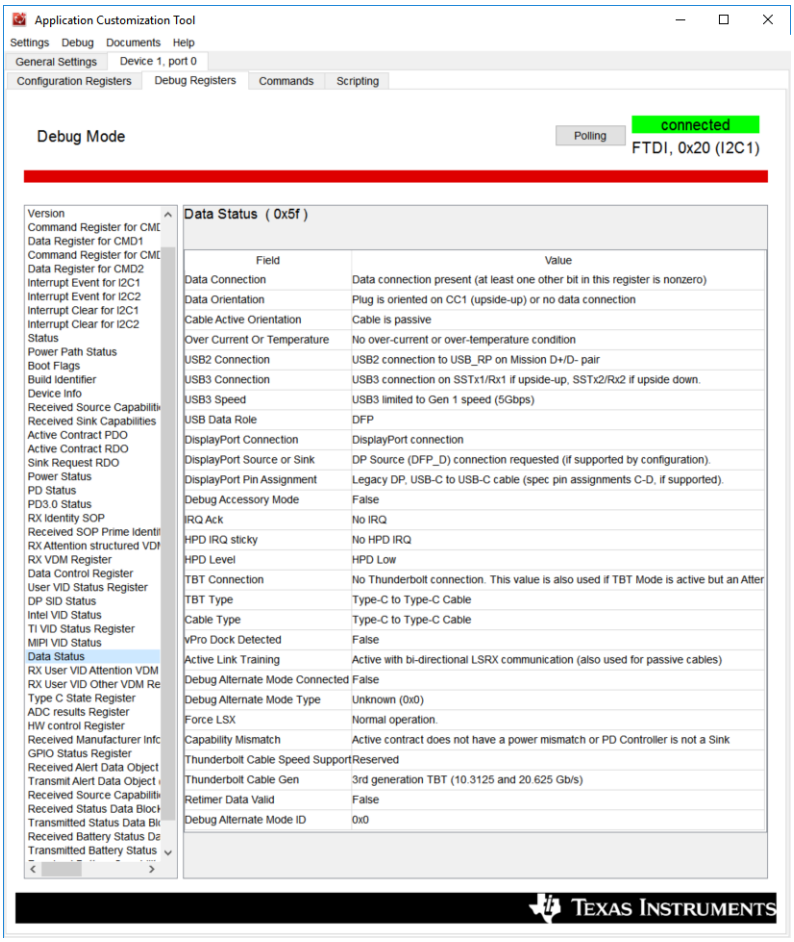

Figure 7. Data Status Register Read from TPS65987D Acting as DFP_D

The DisplayPort Status Register (0x58) was read from the DFP_D side and the results are displayed in Figure 8, showing that the DP Alternate Mode is entered and that this TPS65987D-EVM is indeed acting as a DFP_D within the Alternate Mode.

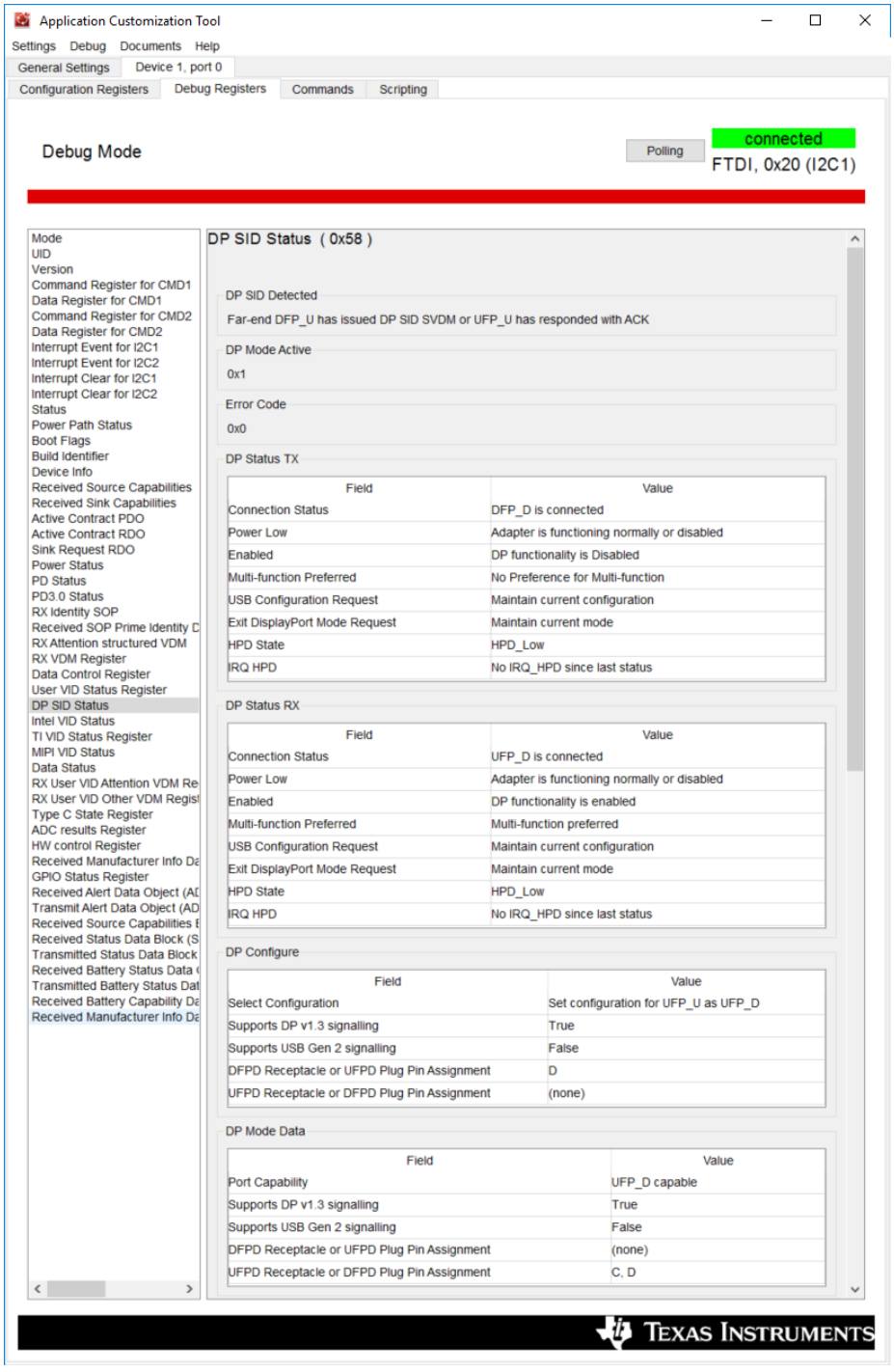

Figure 8. DisplayPort Status Register read from TPS65987D acting as DFP_D

The DisplayPort Status Register (0x58) was read from the UFP_D side and the results are displayed in Figure 8. Comparing this register to Figure 6, note that the register stores packets 180 (DP Status TX), 182 (DP Status RX) , 184 (DP Configure) and 94 (DP Mode Data). This allows the user not only to determine the current state of the system (DP Configure), but to examine the steps leading up to the final configuration, including the full list of Pin Assignments and Port Capabilities supported on each side. From the standpoint of testing and debugging DisplayPort systems, this register is often just as useful as a full PD analyzer trace.

5.1 Modifying DisplayPort Capabilities

This section explains how to modify the DisplayPort capabilities in the TPS6598x Configuration Tool (TPS6598X-CONFIG) to match the actual needs of a system. Although the templates are a great starting point to verify that the FW is successfully entering and configuring the DP Alternate Mode, the real system being designed will have may have different capabilities.

For example, a dongle adapter is a common requirement for new single-Type-C port tablets to connect to legacy DisplayPort monitors, USB3.1 devices, and a power supply to charger the battery at the same time. Although a dongle seems very simple, it requires some changes to the DP Capabilities configurations to behave properly in the DisplayPort Alternate Mode.

First of all, the dongle connects to the laptop directly through a Type-C plug with no Type-C cable. The dongle must be configured as a Type-C plug. In addition to identifying as a plug in DisplayPort Capabilities, the dongle must also be configured for pin DFP_D pins assignments. In addition, dongles are often low-cost and do not have an additional circuit to detect an active USB3.1 device. As a result, this dongle would never be able to achieve 4K resolution because then the USB3.1 Type-A port would be useless and pin assignment C should be disabled, leaving only pin assignment D enabled. Figure 9 shows the new capabilities of the UFP_D, now resaved as *Dongle_2-Lane_DP-USB3.pjt*.

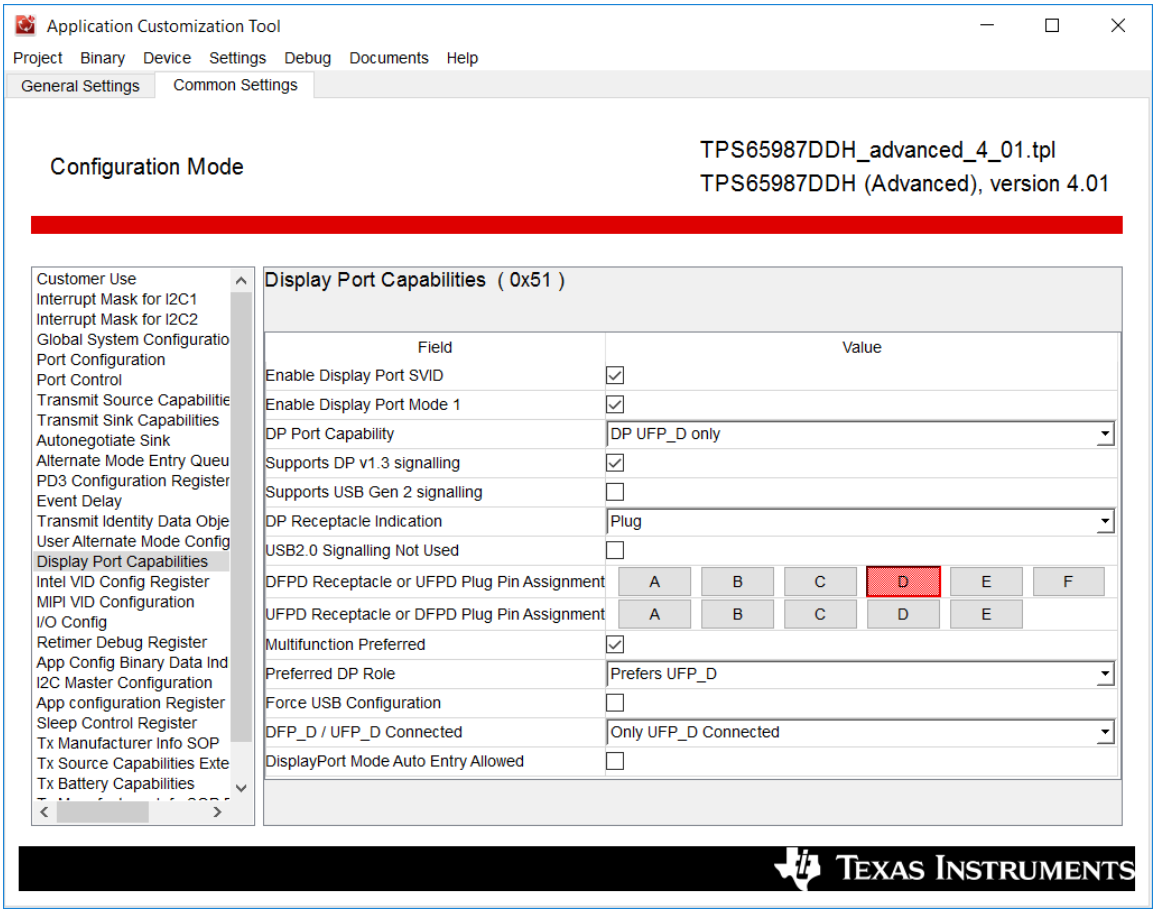

Figure 9. New DisplayPort Capabilities *Dongle_2-Lane_DP-USB3.pjt* **Project**

Figure 10 shows a PD Trace captured after loading the new *Dongle_2-Lane_DP-USB3.pjt* binary FW image on the TPS65987D-EVM and connecting it to the unchanged TPS65987D-EVM acting as the DFP_D,.

NOTE: DisplayPort Mode is now entered and correctly configured with pin assignment D so that the USB3.1 connection will be active in addition to DisplayPort video.

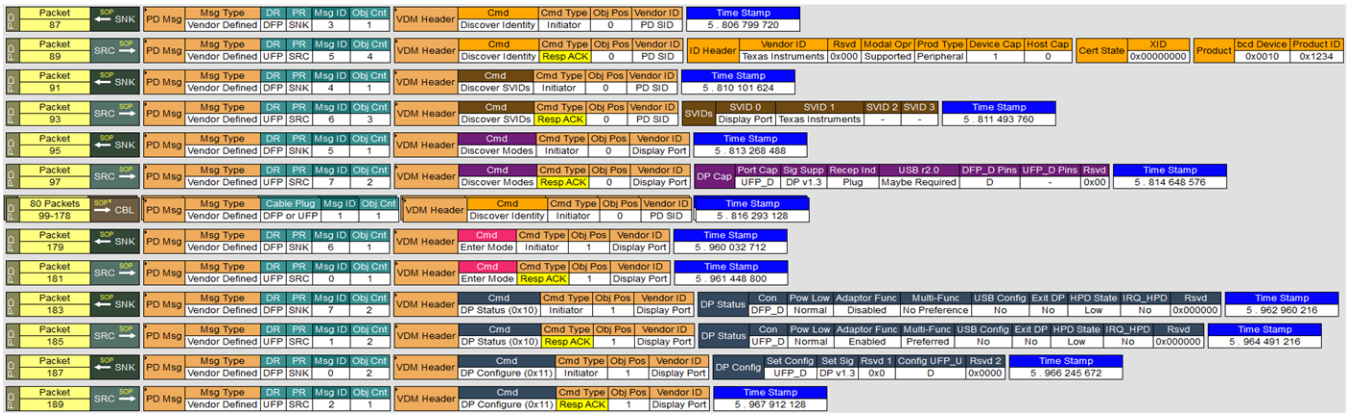

Figure 10. New DisplayPort Entry Sequence Between DFP_D and *Dongle_2-Lane_DP-USB3.pjt*

5.2 Re-Enter DisplayPort Alternate Mode Based on New System Conditions

The TPS65987D device automatically enters and configures the DisplayPort Alternate Mode for an initial plug event and the templates can match the default needs of any system perfectly. In some high-performance products, the product will have a system controller (I^2C master) that can give the product dynamic DisplayPort capabilities.

The following example is common because DisplayPort docks or monitors are commonly also USB hubs for plugging in USB3.1 flash memory drives or external hard drives to legacy Type-A USB ports. If DisplayPort mode resolution is currently 2K, the monitor can detect that a USB3.1 device is not plugged in, and a decision is made by the dock or the system controller of the monitor to increase the screen resolution to 4K, the UFP must be able to alert the DFP of this change in system conditions.

In this example, the multi-function preferred bit is initially set to 1 and the DFP_D originally configured pin assignment D for 2K video resolution and USB3.1 data. The DisplayPort capabilities of the UFP_D are modified so that the multi-function preferred bit is set to 0 (Figure 11) and then a PD hard reset *HRST* message is issued from the UFP_D (Figure 12) so that the PD power contract and DisplayPort Alternate Mode is re-entered. This time, when the entry or configuration sequence occurs, the DFP_D configures pin assignment C for 4K video resolution to maximize the screen resolution (Figure 13). The laptop will not have access to a USB3.1 flash or hard drive device but it is assumed that the dock or monitor detected a USB3.1 drive was not inserted to the legacy Type-A port.

All of the I^2C master control was performed using the TPS6598X Host Interface Utility Tool GUI and the PD traffic was recorded using a PD analyzer to verify the desired results were achieved. The monitor resolution USB3.1 data rate can also be verified from the operating system of the laptop .

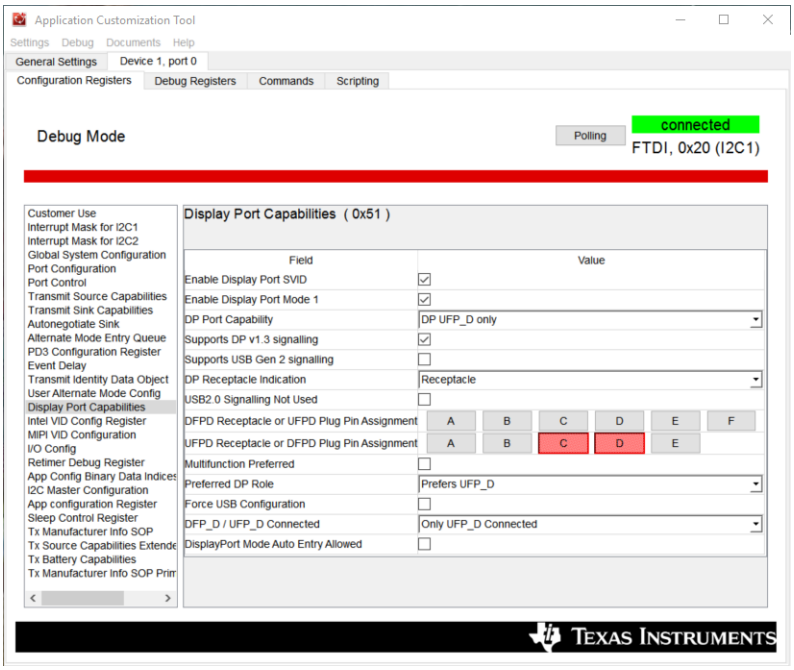

Figure 11. New DisplayPort Capabilities of the UFP_D

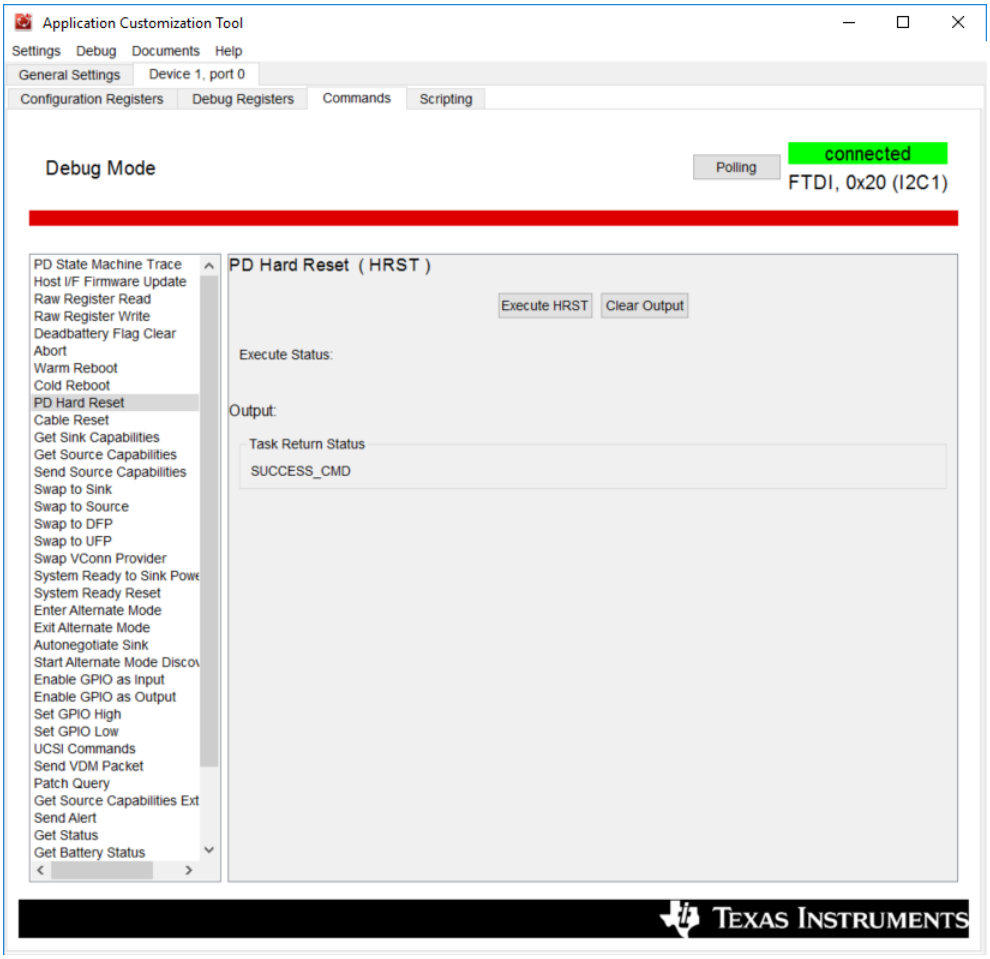

Figure 12. Success After Issuing HRST from the UFP_D to Reset PD Connection

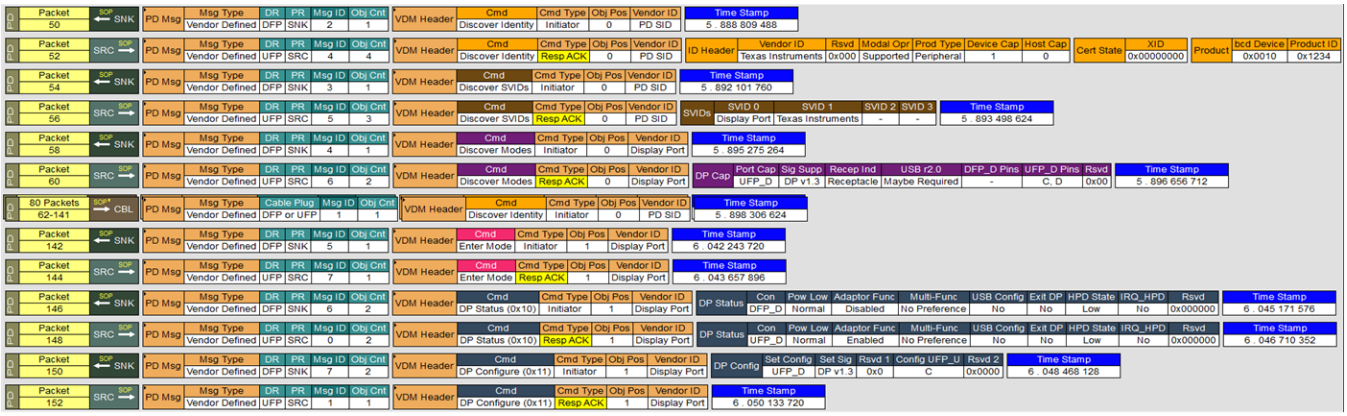

Figure 13. PD Traffic from Hard Reset to DisplayPort Configuration With Pin Assignment C

6 Debugging Common DisplayPort Alternate Mode Issues

The preceding sections discuss what happens when the DisplayPort Alternate is successfully entered and configured. This section discusses what should be done when the first attempt to output DisplayPort video is unsuccessful.

The most common problems with the DisplayPort Alternate Mode stem from the fact that the video connection is usually stable with using legacy laptops and monitors and many engineers are not familiar with the order of events that occur in DisplayPort and the added steps when DisplayPort video data is transmitted over a Type-C cable.

Table 5 provides a short list of sequential steps to walk through when debugging a DisplayPort video connection and possible problems that have occurred. All of these steps can be taken without a USB PD analyzer. Some steps can be done with a simple multi-meter, some can be done only from the laptops operating system, and a few can be done just using visual cues. The list can be stepped through forwards or backwards, but when an item in the list is verified as working the problem must occur after that debug step.

Table 5. Debug Steps for Common DisplayPort Alternate Mode Issues

Debug Step	Where and How to Check	Possible Problem and Resolutions
Observe that a PD Power Contract is active	PD Trace: was any PD data transmitted? Configuration/Debug Tool: Read the Active PDO register (0x34) and verify it is not filled with null data	The PD source or sink is not USB PD compliant and a successful power negotiation never occurred. The connection is dropping out because of repeated overcurrent condition
Verify DP Alternate Mode compatibility between systems	PD Trace: Read DP Capabilities ACK from UFP Configuration/Debug Tool: Inspect DP Config register (0x51) on both sides of system	Both sides are configured as UFP_D or DFP_D DP dongle is being designed and plug or receptacle + pin assignments are incorrect
Monitor the Hot-Plug Detect (HPD) signal	Visual Cue: Look at laptop screen. Does it flash black and then resume normal operation? PD Trace: Check to verify HPD high or attention message is sent with IRQ = Yes Multi-meter or Scope: Measure voltage on HPD signal on both UFP and DFP sides	GPIO4 or GPIO5 not wired or configured correctly HPD signal not meeting IRQ timing requirements
Look for auxiliary data communication	Visual Cue: Open *Display Preferences* in laptop OS. Does a second display appear? Multi-meter or Scope: Measure voltage on SBU1/2 or AUX_P/N signals on both UFP and DFP sides	SBU1/2 pins are not connected correctly or wired backwards
Check for video	Visual Cue: Final step. Look at monitor. Is a video feed coming from the laptop?	SuperSpeed pairs (TX1±, RX1±↔TX2±, RX2±) may be wired upside-down deliberately for easier PCB routing Mismatch between scalar settings and laptop video resolution settings Nonideal routing or poorly manufactured cable/connector

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2016) to A Revision	Page

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