Application Report
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Optimize the Loop Compensation for Start-up Using TPS61178x

Yangwei Yu

ABSTRACT

The response time becomes increasingly important for the power supplies of some applications to minimize the overshoot/undershoot during load transient. To accomplish the stringent requirements, a very common method is to increase the system bandwidth. However, for a boost converter with load disconnect, there are two sets of output capacitors before and after the disconnect FET, so the output capacitor configuration is different for two phases of disconnect being FET on and off. This application note addresses the design of loop compensation of the boost converter with load disconnect to ensure the stable operation for both disconnect FET on and off. An example of TPS61178x is illustrated to show the design details together with the real bench measurements.

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Trademarks

1 Introduction

As a boost with load disconnect function, there is an additional FET serving as the disconnecting input from the output when the device is in shutdown or fault condition. Output capacitance is placed both before and after the disconnect FET, which caused the different output capacitor configuration with the disconnect FET turning on and off. However, the loop compensation usually just covers the case with the disconnect on. It might cause the unexpected performance for the case of disconnect FET in off status. This application note illustrates the details of the loop compensation design to cover both the disconnect on and off using the TPS61178x as an example.

2 Start-up

Figure 1 shows the start-up behavior where VOUT2 is the output voltage after the disconnect FET, VOUT is the output voltage before the disconnect FET, and -VGS is the gate voltage between gate and source of the disconnect FET. IDIS is the gate discharge current of the disconnect FET.

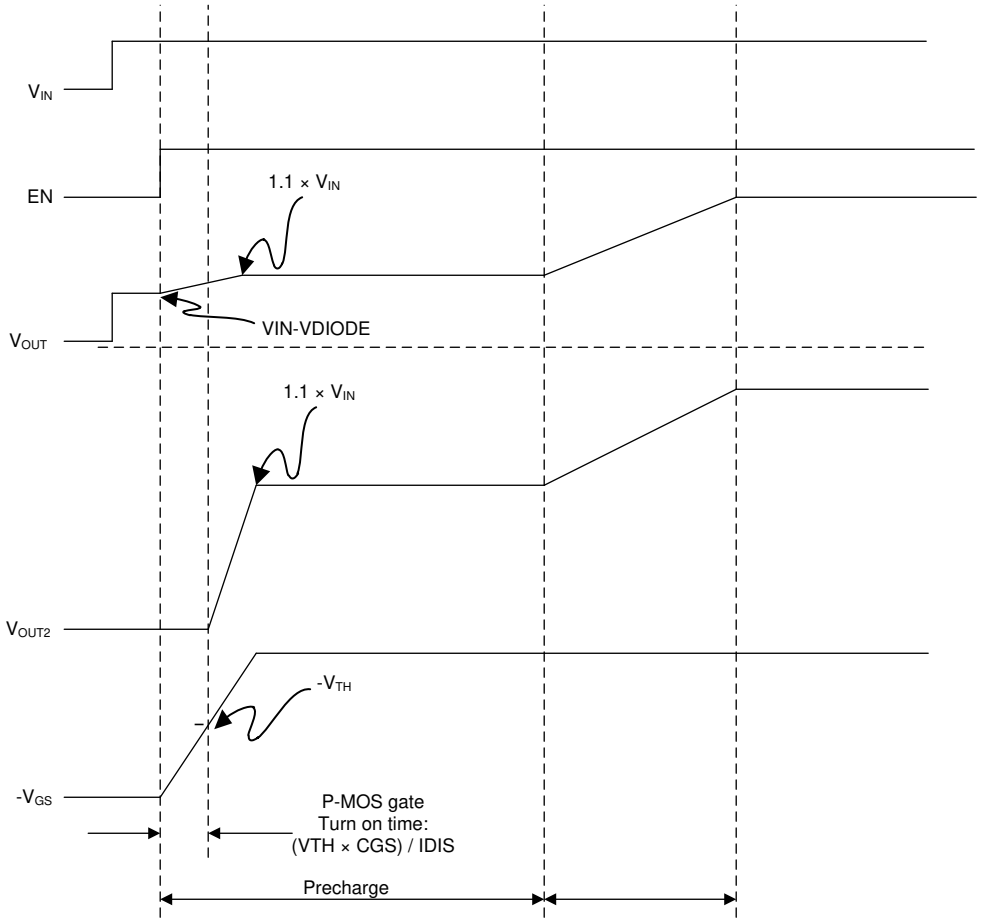


Figure 1. TPS61178x Start-up Behavior

When the input voltage to the device exceeds the UVLO threshold and EN pin pulled to high, the TPS61178x starts to ramp up the output voltage. There is a switching pre-charge phase and the output voltage is charged up to 10% higher than the input voltage (1.1 x VIN). The switching frequency is a fixed 500 kHz at the pre-charge phase. After the pre-charge phase ends (typical 2.6 ms), The TPS61178x regulates the FB pin to the internal soft-start voltage and results in a gradual rise of the output voltage starting from the input voltage level to the target output voltage. The soft-start time is typical 3.2 ms, which helps the regulator to gradually reach the steady state setting point, thus reducing the start-up stresses and surges.

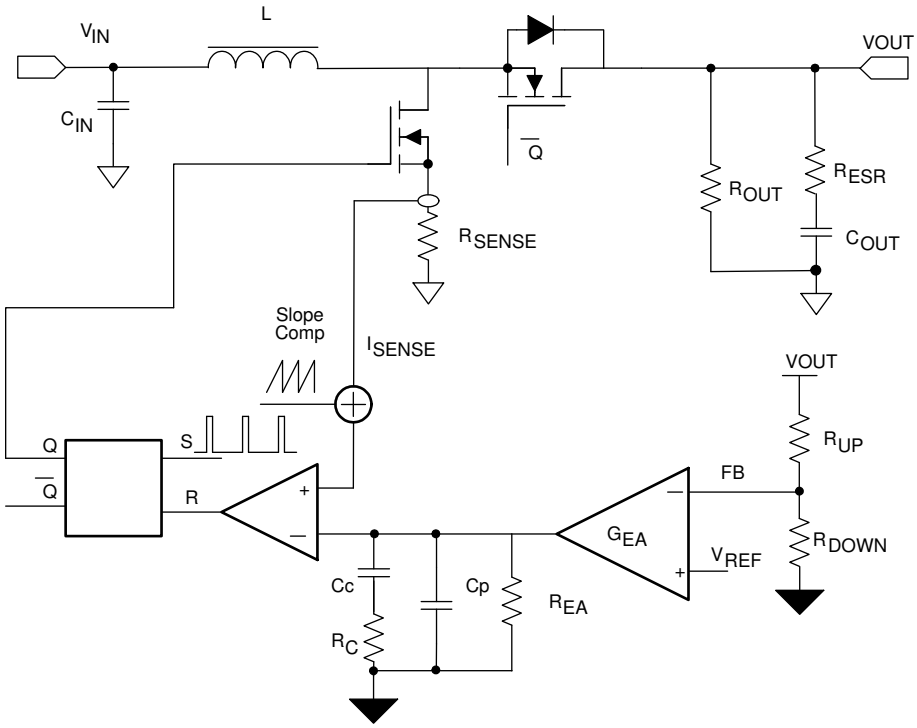


Figure 2. TPS61178x Control Loop of Normal Operation

3 Loop Compensation

The loop compensation with the normal control is illustrated in the *Loop Stability and Compensation* section *TPS61178x 20-V, 10-A Fully-Integrated Synchronous Boost with Load Disconnect Control Data Sheet*. The transfer function of the pre-charge phase is different from the one at steady state, including the following:

- Output capacitor
  - COUT1, only if the disconnect FET is OFF
  - COUT1 and COUT2 if the disconnect is ON (the same as steady state)
- The feedback network
  - The gain of the feedback loop is 1.1 × (VOUT / VIN) while the gain is RDOWN / (RDOWN + RUP) at steady state.

There are two different configurations for pre-charge and steady state. If the loop compensation is characterized at normal steady operation, there is an extra step that checks the stability at the pre-charge phase as well. Make sure the loop is stable for both pre-charge and steady state.

To check the stability for the pre-charge phase, set the output voltage to 1.1 × VIN (the gain of the loop is close to 1.1 × Vin), and measure the bode plot to check the stability.

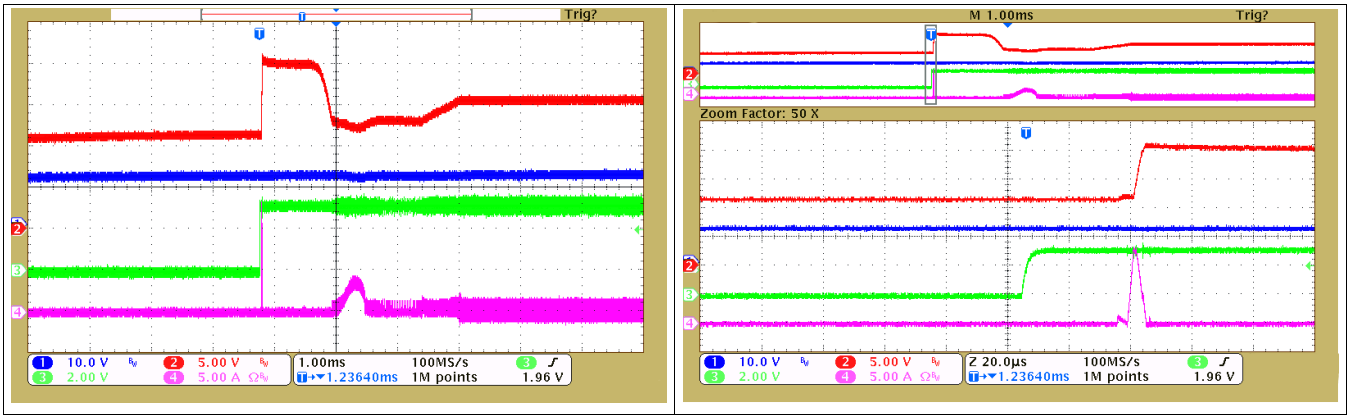
4 Initial Inrush Current After EN ON

For the initial cycles after EN is on (within 10 µs after EN is on), the output of the operation amplifier is charged to a high voltage, depending on the compensation resistor. With this, the inrush current of the initial cycle is caused by the high comp pin voltage due to the large compensation resistor. The voltage of the comp pin for the initial cycle equals the current times the Rcomp. The on-time of the switching is extended if the comp voltage is high, so the inductor peak current is very high if the on-time is long. The COMP voltage of the output of the error amplifier is Rcomp × Icomp = 2.4 V with 120 kΩ Rcomp and 20 µA sink current. It is suggested that make the comp voltage below 1.25 V to limit the for which the Rcomp = 1.25 / 20 µA = 62.5 kΩ.

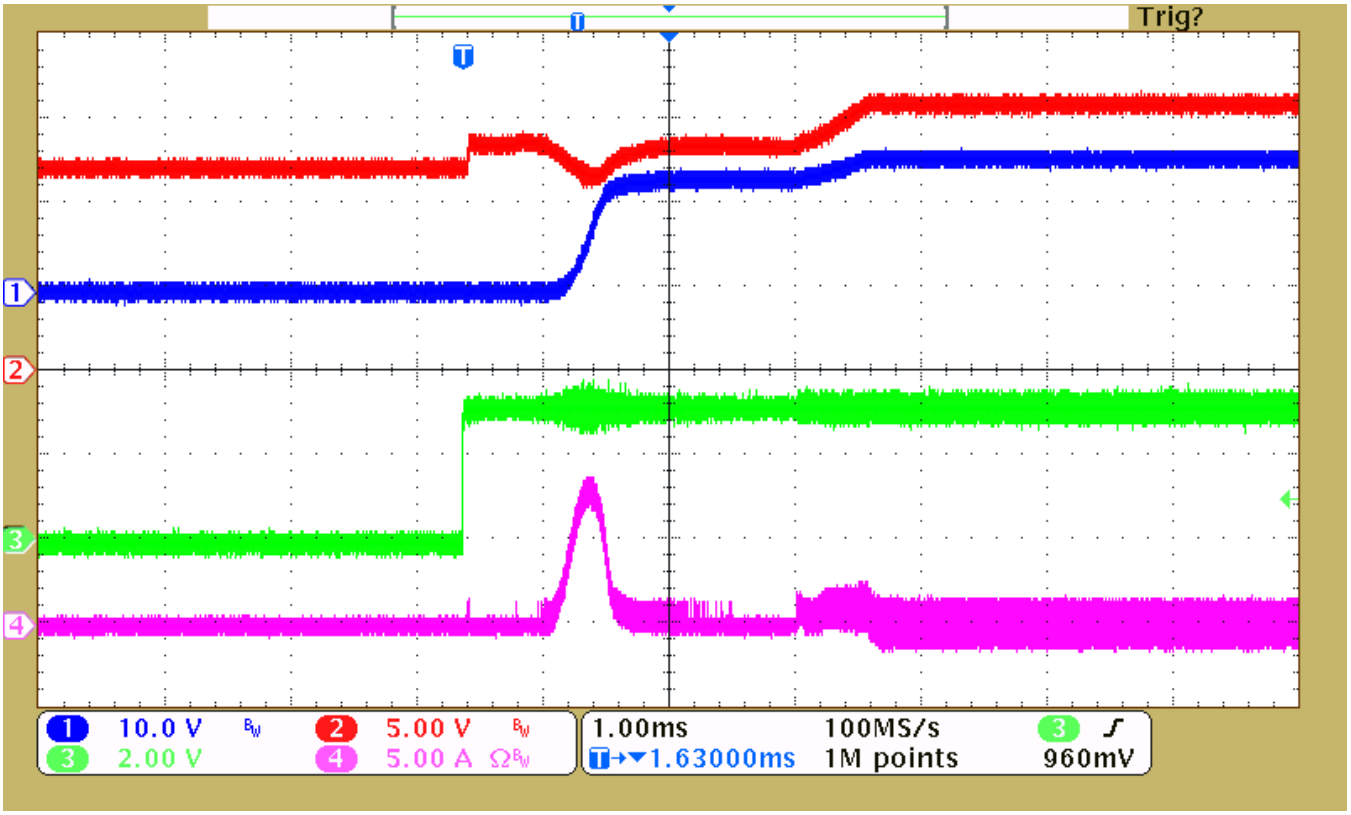
Test condition: Vin = 12 V, Vout = 16 V

Test Condition: Cout is 4 × 22 µF (two in parallel and two in series) Rc = 39.2 K, Cc = 1.5 nFm, Rg = 120 k, Cg = 10 nF before disconnect FET

CH1 VIN, CH2 VOUT (before the disconnected FET), CH3 EN, CH4 ICOIL



Test condition: Cout before ISO FET is 4 × 22 µF (two in parallel and two in series), Rc = 39.2 K, Cc = 1.5 nF, Rg = 39.2 k, Cg = 10 nF



Usually, these loop compensation components are chosen based on the stability in normal operation, but for this device, the components also affect inrush current during start-up. With a lower resistor (from COMP pin to GND), the inrush current of the initial cycles during start-up can be lowered.

5 References

- Texas Instruments, *TPS61178x 20-V, 10-A Fully-Integrated Synchronous Boost with Load Disconnect Control Data Sheet*

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