*Application Note*

# *Resolving Improper Implementation of the Static Voltage Offset on I2C Buffers*

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**ABSTRACT**

This application note discusses how the TCA9509 from Texas Instruments is implemented to resolve improper setup with static voltage offset (SVO) buffers like the TCA9517 and the TCA9617A/B.

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## Trademarks



## 1 Introduction

With the intention of being compliant with the I2C standard for maximum capacitance, I2C buffers or repeaters can be used to separate the parasitic capacitances associated at the inputs and outputs. Some I2C buffers such as the TCA9517, TCA9617A/B, and TCA9509 devices introduce a static voltage offset on one side of the device. A common design mistake is placing two I2C buffers with the SVO side facing each other. This application note takes a deeper look into this violation, the repercussions of not addressing this design mistake, and how to resolve this violation using the TCA9509.

## 2 Contrasting Setups of SVO Buffers

As seen in Figure 2-1, the two sides containing the SVO are connected together, which must not be carried out. Note that the SVO output voltage output low ($V_{OL}$) is considered to be “buffered low”, which is generally higher than the $V_{OL}$ levels of other peripheral devices. Similarly, the voltage output low of the external device ($V_{OL,EXT}$) is required to be less than the voltage input low contention ($V_{ILC}$) at the SVO side to be able to be propagated as an input low into the buffer. These characteristics of the SVO feature result in a gap between the buffered $V_{OL}$ of the first device and the $V_{ILC}$ requirement of the second device. In other words, the $V_{OL}$ of 0.52 V is higher than the $V_{ILC}$ of 0.4 V, so an input low of the first buffer is unable to propagate a low to the second buffer correctly. For more information regarding the SVO feature, see also the Why, When, and How to use $I^2C$ Buffers application note.

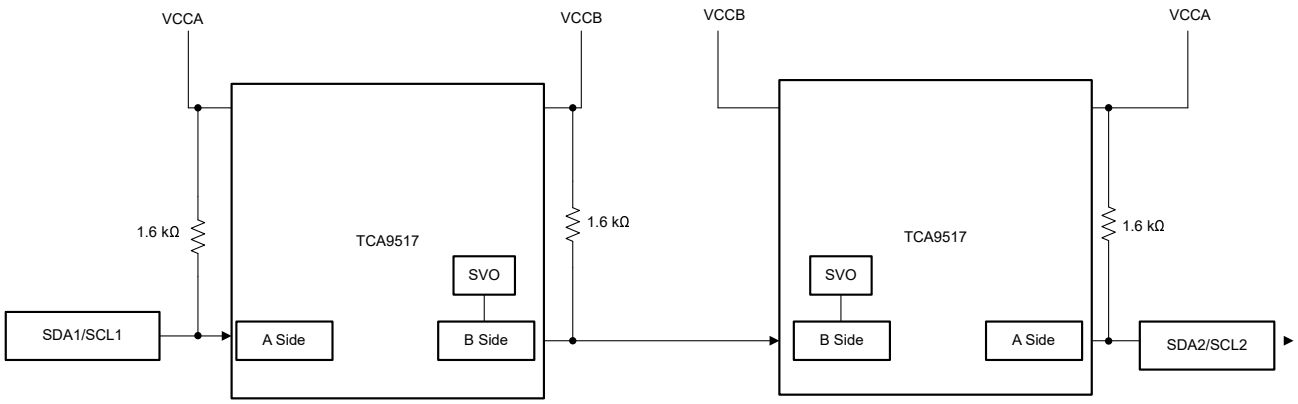


**Figure 2-1. Schematic of Improper Implementation of Two TCA9517s**

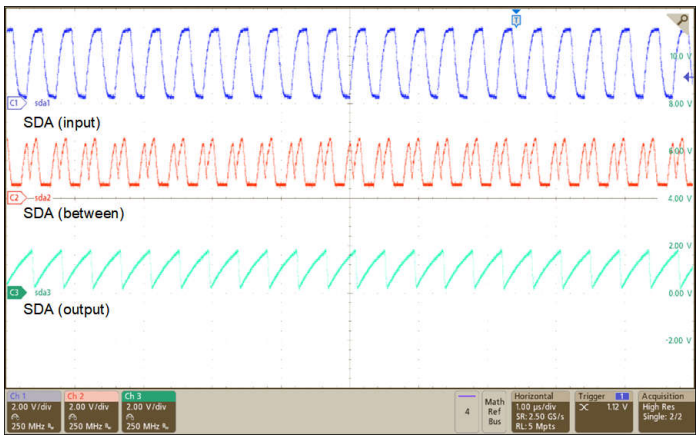


**Figure 2-2. Waveforms as a Result of Improper Setup (Address 0x70h Sent)**

To resolve the implementation issue, the TCA9509 can be used in place of the second TCA9517 as shown in Figure 2-3, allowing for both the B side of the devices to be connected together. This device has the SVO on the A side instead of the B side, which mitigates the concern of improper SVO sides being connected together. The improved performance is shown in Figure 2-4.

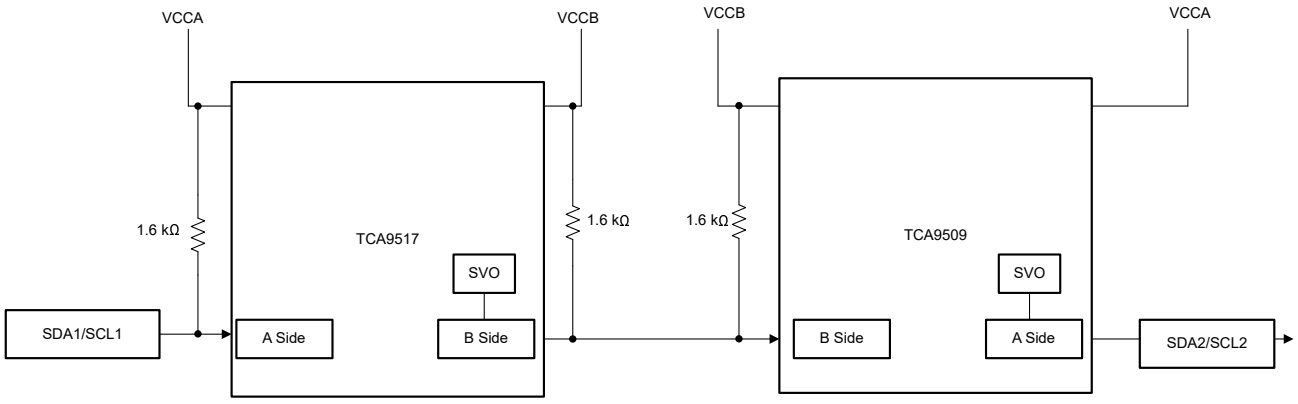


**Figure 2-3. Schematic of Proper Implementation of Buffers With SVO**

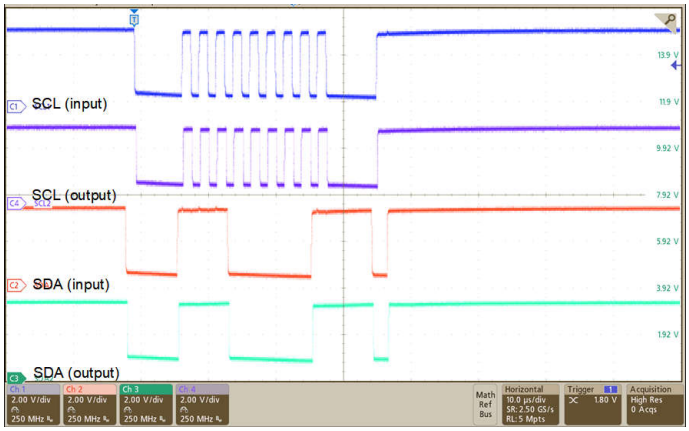


**Figure 2-4. Waveforms as a Result of Proper Setup (Address 0x70h Sent)**

## 3 Important Considerations When Using TCA9509

While the TCA9509 can be used to resolve invalid implementation of static voltage offsets on I2C buffers, there are several considerations that need to be made as well. The TCA9509 can only support I2C operations up to 400 kHz, meaning if the system requires a higher data rate, this device can not be used. Since the SVO feature is on the A-side of the device, system designers need to be aware that pullup resistors and series resistors on this side need to be removed to allow $V_{ILC}$ to be satisfied. The internal structure of the device also does not have an internal pull-up on the OE pin like the TCA9617A/B, so an external pull-up can be required. Furthermore, translation applications from one voltage to another with this device requires VCCA to be at least 1 V less than VCCB. The key differences between the I2C buffers with SVO can be found in Table 3-1.

**Table 3-1. Comparison of Different I2C Buffers With the Static Voltage Offset Feature**

| Device | TCA9517 | TCA9517A | TCA9617A/B | TCA9509 |
|---|---|---|---|---|
| Static Voltage Offset Side | B | B | B | A |
| Supported $V_{CC}$ Range | $V_{CCA}$: 0.9 to 5.5<br>$V_{CCB}$: 2.7 to 5.5 | $V_{CCA}$: 0.9 to 5.5<br>$V_{CCB}$: 2.7 to 5.5 | $V_{CCA}$: 0.8 to $V_{CCB}$<br>$V_{CCB}$: 2.2 to 5.5 | $V_{CCA}$: 0.9 to 5.5<br>$V_{CCB}$: 2.7 to 5.5 |
| $V_{OL}$ | 0.45 to 0.6 V (B-side) | 0.45 to 0.6 V (B-side) | 0.48 to 0.58 V (B-side) | 0.2 V (A-side) |
| $V_{ILC}$ | 0.4 V | 0.45 V | 0.4 V | 0.15 V |
| $V_{IL}$(max) Non offset side | 0.3 × $V_{CCA}$ | 0.3 × $V_{CCA}$ | 0.3 × $V_{CCA}$ | 0.3 × $V_{CCB}$ |
| Max data rate | 400 kHz | 400 kHz | 1 MHz | 400 kHz |
| Package options | VSSOP(8), SOIC(8) | VSSOP (8) | VSSOP (8) | VSSOP (8), X2QFN(8) |
| P2P | Y | Y | Y | Y |

## 4 Summary

Both the TCA9517 and TCA9617 have the SVO feature on the B-side of the device. When these two devices with B-side connect, the VILC requirements of both devices are bound to be violated. This leads to a bus lock up, potentially causing oscillations as shown in Figure 2-2. System designers can use the TCA9509 to fix existing violations of the Static Voltage Offset rules where two buffers are interfaced together with SVO since the $V_{ILC}$ requirement for TCA9509 is on the A-side. By using the TCA9509 in place of the second TCA9517, the SVO buffer B-side to B-side configuration is resolved.

## 5 References


- Texas Instruments, *Choosing the Correct I²C Device for New Designs*, application note
- Texas Instruments, *Why, When, and How to use I²C Buffers*, application note
- Texas Instruments, *TCA9517 Level-Translating FM+ I²C Bus Repeater*, data sheet
- Texas Instruments, *TCA9617A Level-Translating FM+ I²C Bus Repeater*, data sheet
- Texas Instruments, *TCA9617B Level-Translating FM+ I²C Bus Repeater*, data sheet
- Texas Instruments, *TCA9509 Level-Translating I²C and SMBUS Bus Repeater*, data sheet

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