Test Report: TPS7H3302-SEP

Single-Event Effects (SEE) Test Report of the TPS7H3302-SEP DDR Termination Regulator

ABSTRACT

The purpose of this study was to characterize the effect of heavy-ion irradiation on the SEE performance of the TPS7H3302-SEP sink/source DDR termination regulator. Heavy-ions with LET_{EFF} of 48 MeV-cm^2/mg were used to irradiate three production devices with fluences ranging from 9.98 × 10^5 to 1 × 10^7 ions/cm^2 per run, over a variety of DDR modes, input and output voltage conditions, load conditions, and temperatures. The TPS7H3302-SEP is completely SEL adn SEB free up to LET_{EFF} = 48 MeV-cm^2/mg at 125°C under all DDR modes. Forall DDR the device is also SET-free and SEFI-free up to LET_{EFF} = 48 MeV-cm^2/mg.

Table of Contents

List of Figures

List of Tables

Trademarks

National Instruments™ is a trademark of National Instruments.
Agilent™ is a trademark of Agilent Technologies.
Kevlar® is a registered trademark of E.I. du Pont de Nemours and Company.
LabVIEW® is a registered trademark of National Instruments.
All trademarks are the property of their respective owners.

1 Introduction

The TPS7H3302-SEP is a radiation-tolerant, sink/source, double-data-rate (DDR) 3-A termination regulator designed to provide a complete, compact, and low-noise solution for space DDR termination applications where small form-factor and low weight are key considerations. The TPS7H3302-SEP showcases a number of capabilities such as:

- Supporting DDR VTT termination applications
- Stable supply during read/write conditions through fast transient response
- Built-in VTT_{REF} supply to track VTT to reduce solution size
- Integrated Power Good (P_{GOOD})

The TPS7H3302-SEP is packaged in a 32-pin HTSSOP plastic package. Table 1-1 lists general device information and test conditions. For more detailed technical specifications, user-guides, and application notes, see www.ti.com/product/TPS7H3302-SEP/technicaldocuments.

Table 1-1. Overview Information

DESCRIPTION(1)	DEVICE INFORMATION
TI Part Number	TPS7H3302-SEP
Orderable Number	TPS7H3302MDAPTSEP
Device Function	DDR termination regulator
Technology	LBC7 (250-nm linear BiCMOS)
Exposure Facility	Radiation Effects Facility, Cyclotron Institute, Texas A&M University
Heavy Ion Fluence per Run	$5.95 \times 10^5 - 1 \times 10^7$ ions/cm^2
Irradiation Temperature	25°C (for SET and SEB/SEGR testing) and 125°C (for SEL testing)

(1) TI may provide technical, applications or design advice, quality characterization, and reliability data or service providing these items shall not expand or otherwise affect TI's warranties as set forth in the Texas Instruments Incorporated Standard Terms and Conditions of Sale for Semiconductor Products and no obligation or liability shall arise from Semiconductor Products and no obligation or liability shall arise from TI's provision of such items.

2 Single-Event Effects (SEE)

The TPS7H3302-SEP device does not operate at high voltages or high currents, so single-event burnout (SEB) and single-event gate-rupture (SEGR) events are not expected to be an issue. The primary SEE events of interest in the TPS7H3302-SEP are single-event latch-up (SEL), single-event functional interrupt (SEFI), and single-event transient (SET).

From a risk and impact point-of-view, the occurrence of a SEL is potentially the most destructive SEE event and the biggest concern for space applications. In mixed technologies such as the Linear BiCMOS 7 process used for the TPS7H3302-SEP, the CMOS circuitry introduces a potential SEL susceptibility. SEL can occur if excess current injection caused by the passage of an energetic ion is high enough to trigger the formation of a parasitic cross-coupled PNP and NPN bipolar structure (formed between the p-substrate and n-well and n+ and p+ contacts) ([1]) ([2]). The parasitic bipolar structure creates a high-conductance path (creating a steady-state current that is typically orders-of-magnitude higher than the normal operating current) between power and ground that persists (is latched) until power is removed or until the device is destroyed by the high-current state. For the design of the TPS7H3302-SEP, SEL susceptibility was reduced by maximizing anode-cathode spacing (tap spacing) while increasing the number of well and substrate ties in the CMOS portions of the layout. Additionally, junction isolation techniques were also used with buried wells and guard ring structures isolating the CMOS p- and n-wells ([3]) ([4]) ([5]). The design techniques applied for SEL-mitigation were sufficient as the TPS7H3302-SEP exhibited no signs of SEL during all of the heavy-ions up to an LET_{EFF} = 48 MeV-cm^2/mg at a fluence of 10^7 ions/cm^2 and a die temperature of 125°C.

Unlike the varied and unique failure signatures of SEFI events in complex digital processors usually requiring an external reboot or reset to clear, in simpler devices like the TPS7H3302-SEP voltage regulator, SEFI is defined as anything that can affect downstream electronic components, in this case, DDR memories using the TPS7H3302-SEP to generate V_{TT}/V_O and V_{TTREF} signals. It was assumed that SEFIs might manifest as an upset in the control logic causing either a system reset or inducing a false P_{GOOD}, an event where P_{GOOD} is pulled down without a concurrent collapse of V_{TT}/V_O. To mitigate this, all logic was triplicated with a hardened voter on key outputs. Another potential source of SEFI was an ion erroneously triggering the current-limiting clamp. To mitigate this type of SEFI, a redundant regulator loop with each loop having its own current limiting clamps was included in the design; with each regulator loop having its own independent biasing circuit. The design techniques applied for SEFI-mitigation (triple modular redundancy with hardened voters in key functional blocks) were sufficient because the TPS7H3302-SEP exhibited no signs of these type of SEFIs either in the logic or in the regulator loop itself under heavy-ions with LET_{EFF} of up to 48 MeV-cm^2/mg at fluences of up to 5 × 10^7 ions/cm^2.

Voltage regulators can exhibit positive, negative, and bipolar SETs whose magnitude and polarity depend on how the ionization is distributed (a function of the ion LET, location, trajectory, energy, the thickness and composition of the BEOL stack, and so forth) and what part of the circuit is hit ([6]) ([7]) ([8]) ([9]). All of the design techniques (previously mentioned) to mitigate SEFI will also mitigate some of the SETs from affecting the output. However, if the output transistors are hit, it is hard to fully avoid a transmission of the transient to the outputs. The actual shape and duration of the SETs is a strong function of output capacitance and can also be affected by the load conditions. SETs are generally only a concern if their magnitude and duration actually cause a disruption in downstream power.

In the case of the TPS7H3302-SEP the difference between V_{TT}/V_O and V_{TTREF} signals is the most important feature. In other words those two signals can vary, but they need to track so that the voltage margin during DDR memory accesses is stable. SETs of primary concern were those that caused the difference between these two signals to exceed a specified value. The JEDEC DDR specification states that any difference between V_{TT}/V_O and V_{TTREF} signals exceeding ±40 mV is problematic for the reliable read-write operation of a DDR memory system. The TPS7H3302-SEP exhibited no signs of SETs up to an LET_{EFF} = 48 MeV-cm^2/mg at a fluence of 10^6 ions/cm^2.

3 Test Device and Evaluation Board Information

The TPS7H3302-SEP is packaged in a 32-pin HTSSOP plastic package shown with the pinout in Figure 3-1. The TPS7H3302 evaluation board was used to evaluate the performance and characteristics of the DDR/DDR2/DDR3/DDR4 V_{TT} termination regulator of the TPS7H3302-SEP. Figure 3-2 shows the top and bottom views of the evaluation board used for radiation testing. For more information about the device or evaluation board, see www.ti.com/product/TPS7H3302-SEP/technicaldocuments.

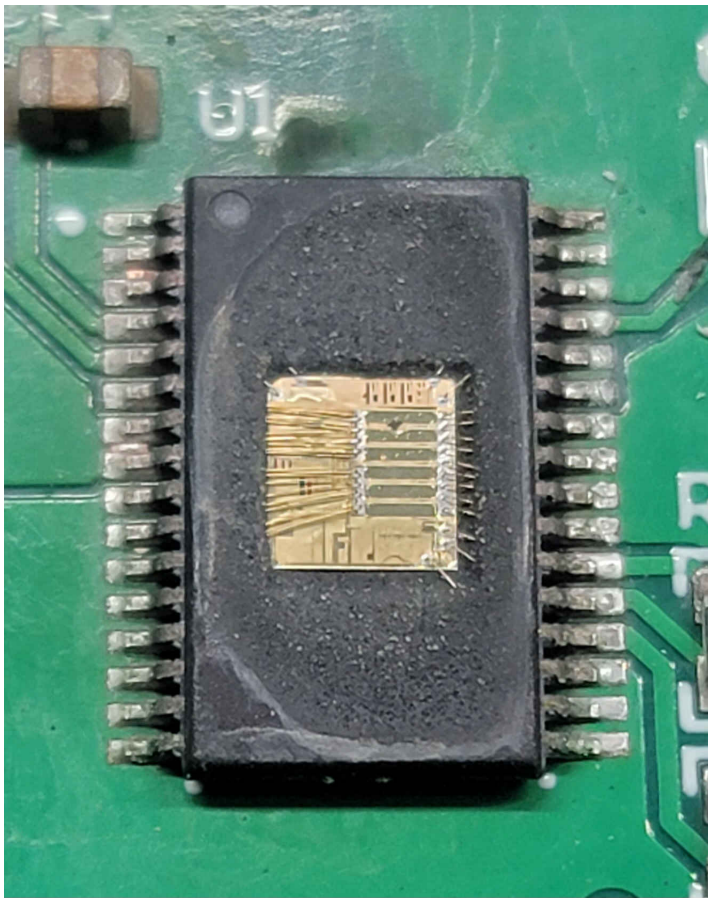


Figure 3-1. Photograph of the TPS7H3302-SEP Space DDR Termination Regulator Delidded

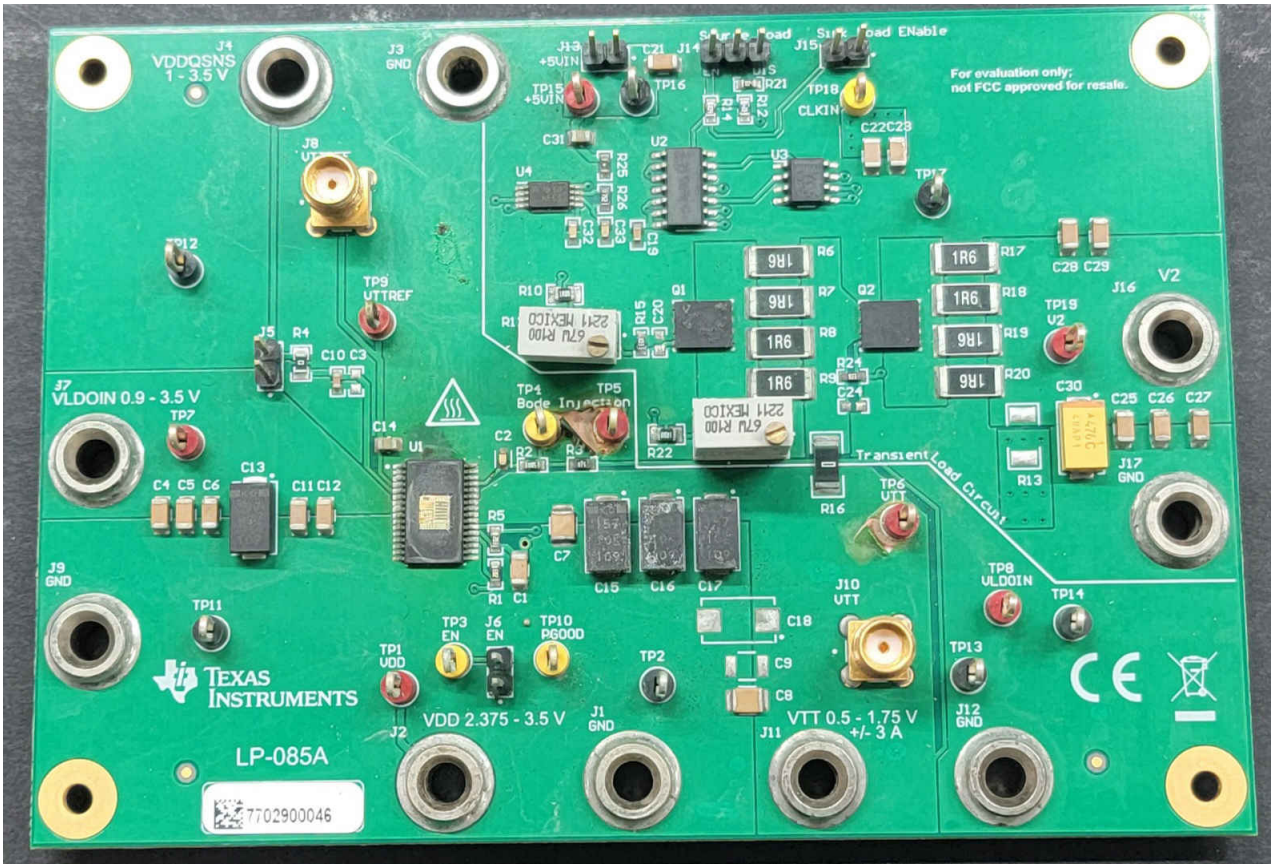


Figure 3-2. TPS7H3302-SEP Evaluation Board Top View

Figure 3-3 shows a simplified schematic of the configuration used for this radiation testing, based on the evaluation module for the TPS7H3302-SEP (TPS7H3302EVM.) For more information please see TPS7H3302EVM User's Guide.

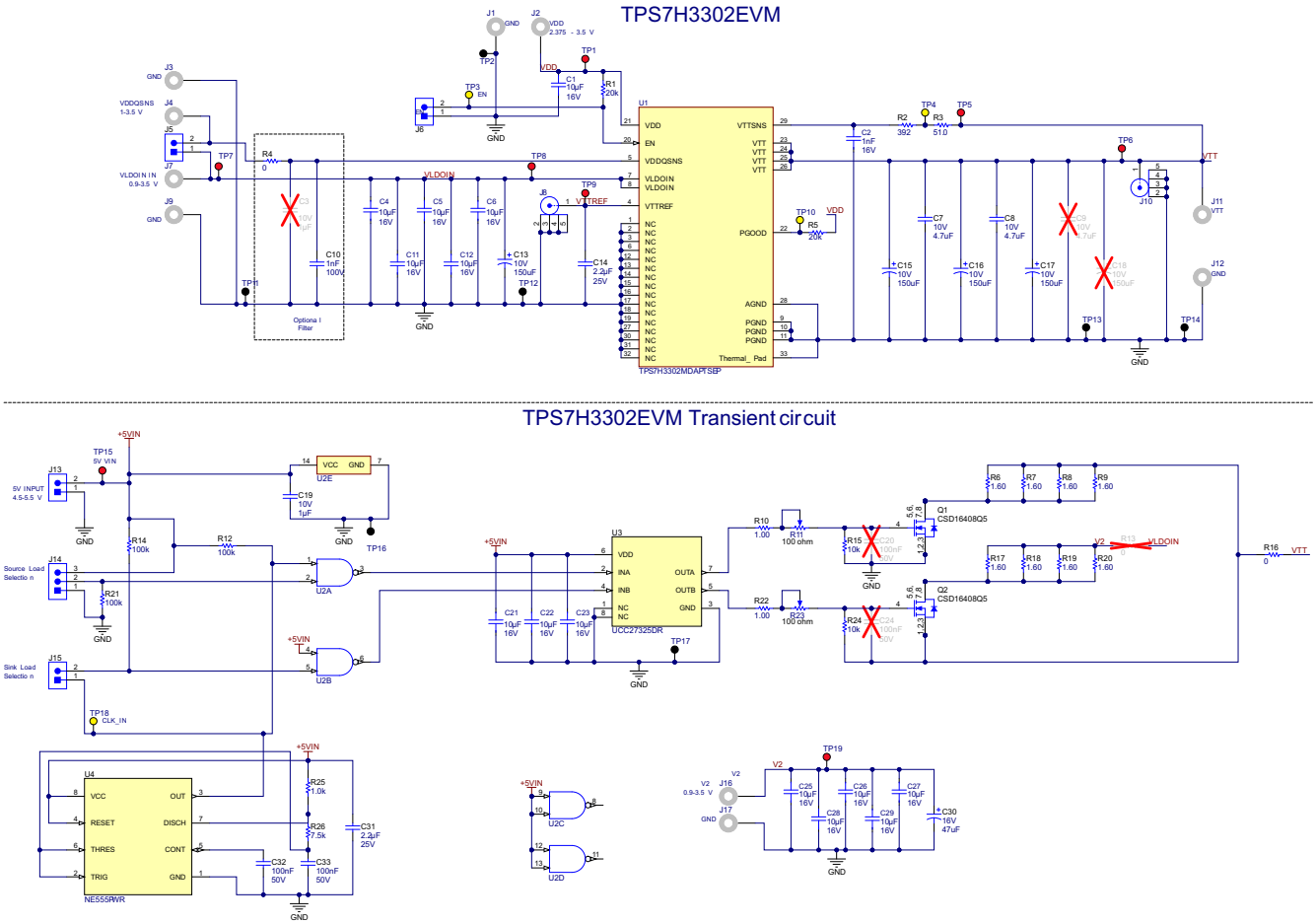


Figure 3-3. Schematic of the Prototype TPS7H3302 Evaluation Board Used to Perform the SEE Tests on the TPS7H3302-SEP Devices

4 Irradiation Facility and Setup

The heavy ion species used for the SEE studies on this product were provided and delivered by the TAMU Cyclotron Radiation Effects Facility ([10]) using a superconducting cyclotron and advanced electron cyclotron resonance (ECR) ion source. Ion beams are delivered with high uniformity over a 1-in diameter circular cross sectional area for the in-air station. Uniformity is achieved by means of magnetic defocusing. The intensity of the beam is regulated over a broad range spanning several orders of magnitude. For the bulk of these studies, ion fluxes between 10^4 and 10^5 ions/cm^2-s were used to provide heavy ion fluences between 10^6 and 10^7 ions/cm^2.

For these experiments, Silver (^{109}Ag) ions were used at a 0° (incident) angle for a LET of 48 MeV-cm^2/mg. ^{109}Ag ions hadve a total kinetic energy of 1.634 GeV in the vacuum (15 MeV/amu line). Ion beam uniformity for all tests was in the range of 92% to 97%. The TPS7H3302-SEP test board is shown in Figure 4-1 as it was used at the TAMU facility. Although not visible in this photo, the beam port has a 1-mil Aramica window to allow in-air testing while maintaining the vacuum within the accelerator with only minor ion energy loss. The in-air gap between the device and the ion beam port window was maintained at 40 mm for all runs.

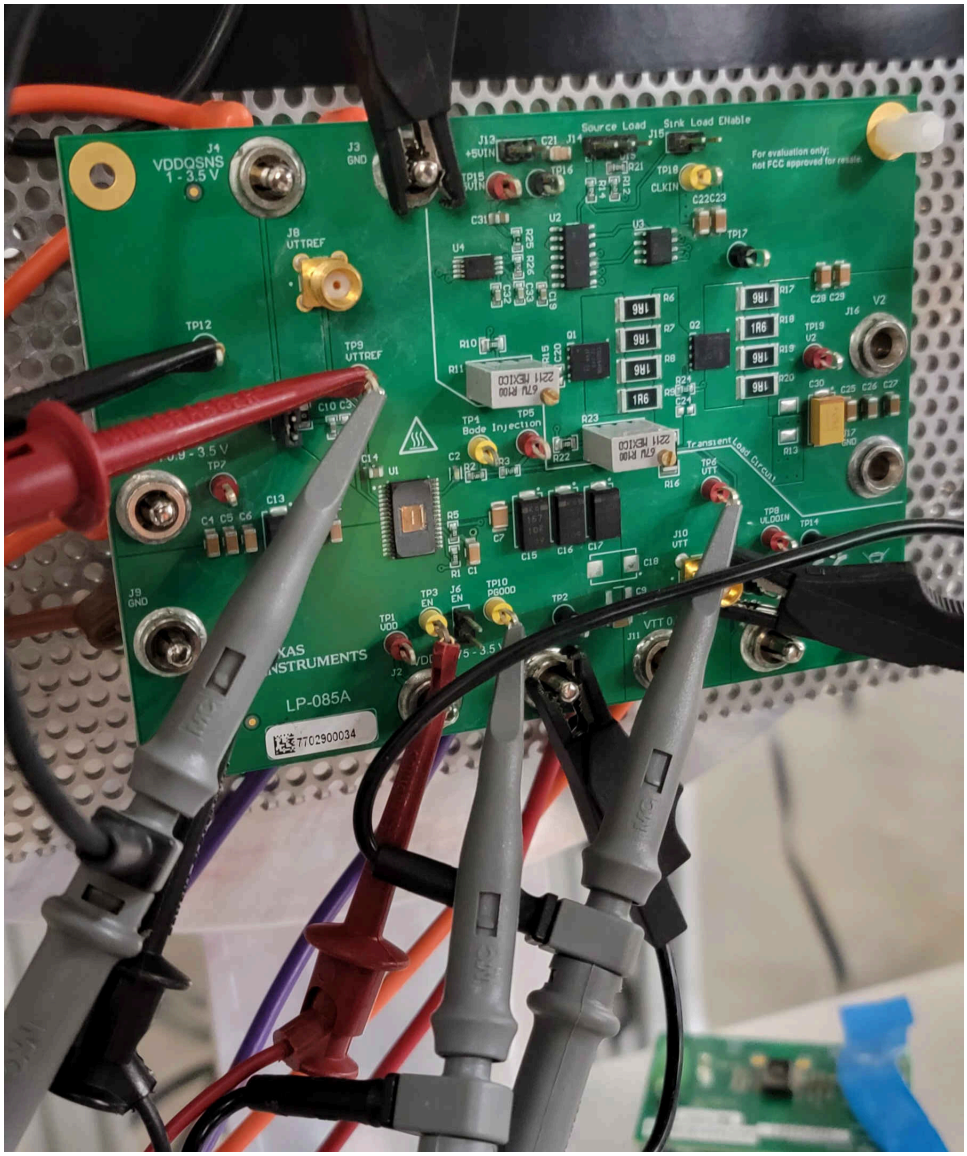


Figure 4-1. Photograph of the TPS7H3302-SEP Evaluation Board Mounted in Front of the Heavy Ion Beam Exit Port at the TAMU Accelerator Facility

5 Depth, Range, and LET_{EFF} Calculation

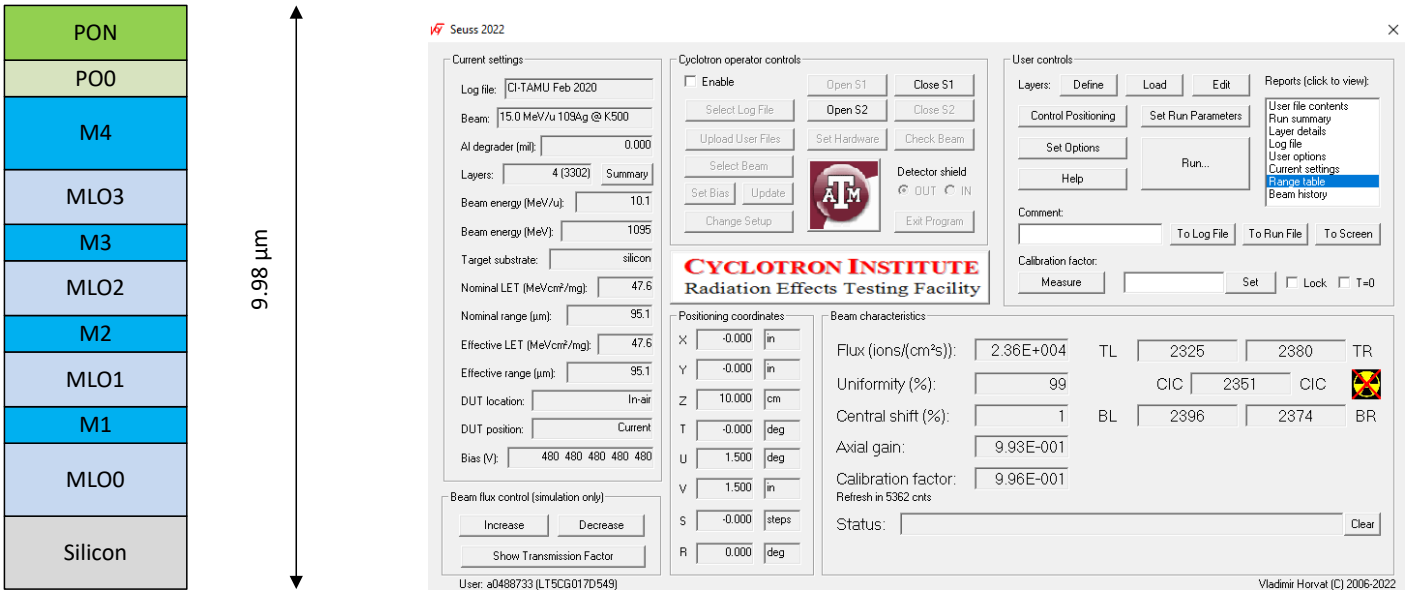


Figure 5-1. Layer Stack of TPS7H3302-SEP [Left] and RADsim-IONS Program [Right] Used to Determine Key Ion Parameters

The TPS7H3302-SEP is fabricated in the Texas Instruments Linear BiCMOS 250-nm process (LBC7) with a back-end-of-line (BEOL) stack consisting of three levels of standard thickness aluminum metal on a 0.6-µm pitch, and a 4th level of thick aluminum. The total stack height from the surface of the passivation to the silicon surface is 9.98 µm based on nominal layer thickness as shown in Figure 5-1. No polyimide or other coating was present so the uppermost layer was the nitride passivation layer (PON). Accounting for energy loss through the 1-mil thick Aramica (Kevlar®) beam port window, the 40-mm air gap, and the BEOL stack over the TPS7H3302-SEP, the effective LET (LET_{EFF}) at the surface of the silicon substrate and the depth and ion range was determined with the custom RADsim-IONS application (custom tool developed at Texas Instruments and based on SRIM ([11]) simulations) for the two primary ions used for the experiments. Table 5-1 shows the results. The stack was modeled as a homogeneous layer of silicon dioxide.

Table 5-1. Silver LET_{EFF}, Depth, and Range in Silicon

ION TYPE	Beam Energy (MeV/ nucleon)	ANGLE OF INCIDENCE	RANGE IN SILICON (µm)	LET_{EFF} (MeV-cm²/mg)
^{109}Ag	15	0°	95	48

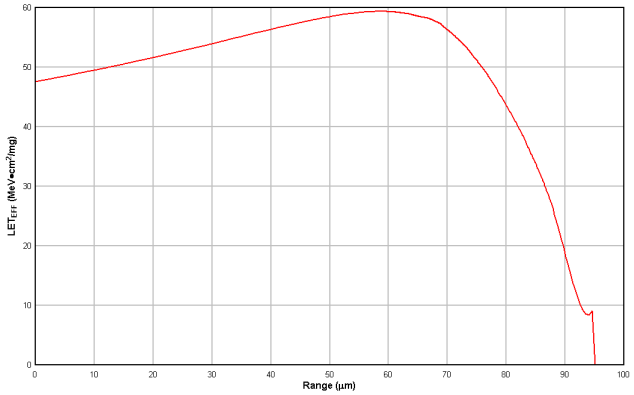


Figure 5-2. LET_{EFF} vs Range for ^{109}Ag at the Conditions Used for the SEE Test Campaign

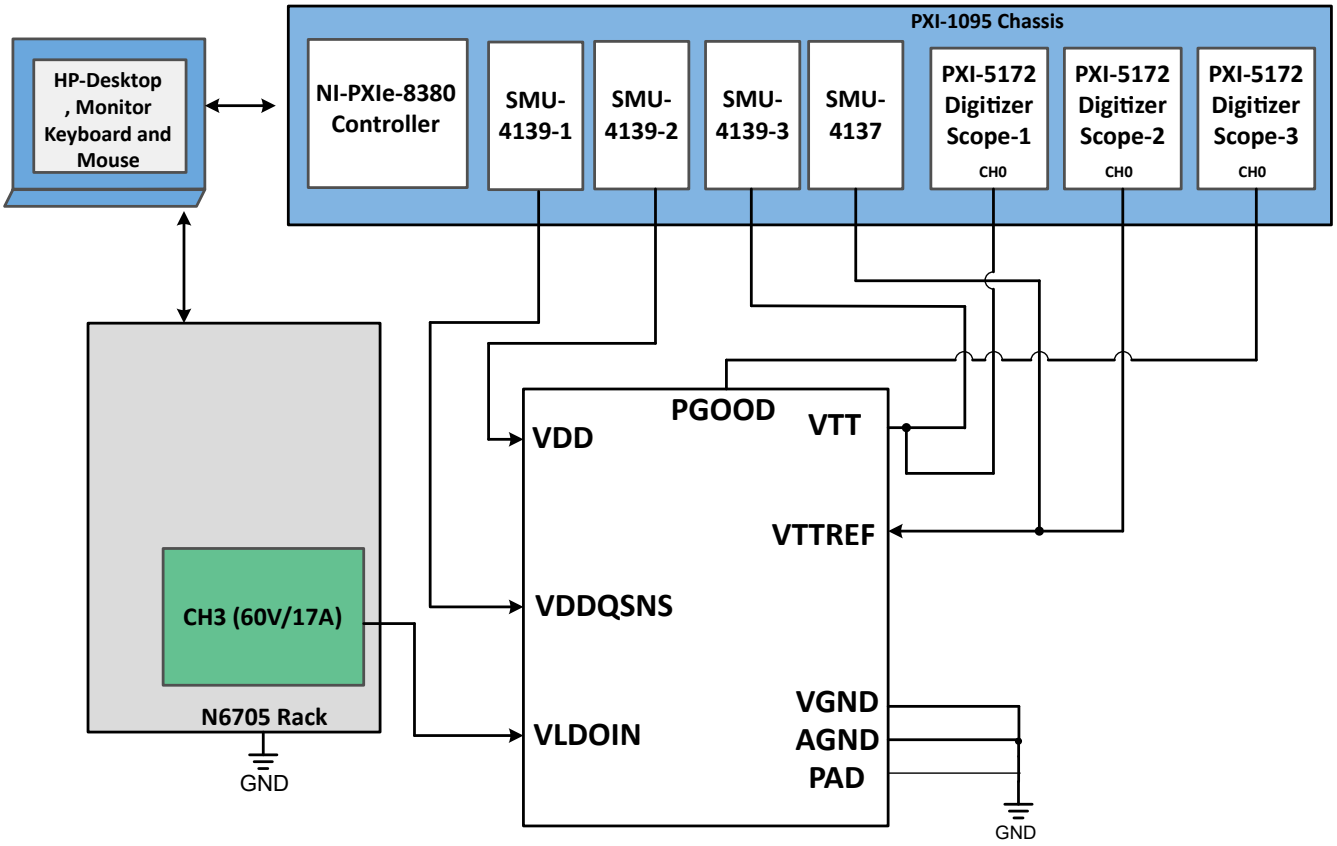
6 Test Set-up and Procedures

SEE testing was performed on a TPS7H3302-SEP device mounted on a prototype of the TPS7H3302 evaluation board. The board was powered to each of its DDR cases by providing voltages to V_{LDO}, V_{IN}, V_{DDQSNS}, and enabled by providing voltage to EN. An Agilent N6705C was used to provide power to V_{LDO}, a power All voltage rails were connected in a 4-wire configuration. The device was loaded with two NI-PXIe-4139 source meters, one to provide a load for the V_{TT}/V_O output and one to independently provide a load for V_{TTREF} output. The SEE events were monitored by using three NI-PXI 5172 Scope Cards.

All equipment was controlled and monitored using a custom-developed LabVIEW® program (PXIRadTest) running on a National Instruments™ NI-PXIe 8381 remote control module. Figure 6-1 shows a block diagram of the set-up used for SEE testing the TPS7H3302-SEP, and Table 6-1 shows the connections, limits and compliances used. The TPS7H3302-SEP was tested at room temperature and 125°C. For higher temperature tests, the device was heated using a Closed-Loop PID controlled heat gun (MISTRAL 6 System (120V, 2400W)). The die temperature was monitored during the testing using an IR camera prior to exposure to heavy ions.

Table 6-1. Equipment Set Used for the SEE Testing

PIN NAME	EQUIPMENT USED	CAPABILITY	COMPLIANCE	RANGE OF VALUES USED
V_{LDOIN}	Agilent™ N6705C (Ch 3)	17 A	100 mA	2.375 V to 3.5 V
V_{IN}	NI-PXIe-4139	3 A	5 A	1.2 V to 2.5 V
V_{DDQSNS}	NI-PXIe-4139	3 A	500 mA	1.2 V to 2.5 V
V_{TTREF}	NI-PXIe-4137	±3 A	Sink/Source	—
V_{TT}/V_O	NI-PXIe-4139	±3 A	Sink/Source	0.60 V to 1.25 V
Oscilloscope card (V_{TT}/V_O)	NI-PXIe 5172	100 MSPS	—	—
Oscilloscope card (V_{TTREF})	NI-PXIe 5172		—	—
Oscilloscope card (P_{GOOD})	NI-PXIe 5172		—	—



The V_{TT}/V_O output was used to trigger the oscilloscopes. The Agilent N6702A provided the precision power inputs and the Yokogawa GS610 and Keithley 2000 source meters provided active loading.

Figure 6-1. Block Diagram of Heavy-Ion SEE Test Set-Up With the TPS7H3302-SEP on a TPS7H3302 Evaluation Board

All boards used for SEE testing were fully checked for functionality and dry runs performed to ensure that the test system was stable under all bias and load conditions prior to being taken to the TAMU facility. During the heavy-ion testing, the LabVIEW control program powered up the TPS7H3302-SEP device and set the external sourcing and monitoring functions of the external equipment. After functionality and stability had been confirmed, the beam shutter was opened to expose the device to the heavy ion beam. The shutter remained open until the target fluence was achieved (determined by external detectors and counters).

During the irradiation the PXIe–5172 scope card monitored the P_{GOOD}, V_{TT}/V_O and V_{TTREF} outputs of the TPS7H3302-SEP. One scope card triggered off of V_{TT}/V_O when the signal exceeded a window of 1%, one scope card triggered off of V_{TTREF} when the signal exceeded a window of 1%, and the last scope card triggered on a negative edge 500mA below the nominal value of P_{GOOD}.

In addition to continuously monitoring the voltage levels of the five digital scope inputs, the currents into or out of the V_{DDQSNS}, V_{IN}, and V_{LDOIN} pins were also monitored during each test to enable the detection of the occurrence of an SEL event. No sudden increases in current were observed (outside of normal fluctuations) on any of the test runs which indicated that no SEL events occurred during any of the testing.

7 Results

7.1 SEL Results

All SEL characterizations were performed with forced hot air to maintain the device temperature at 125°C with the silver (Ag) heavy ion beam at an incident angle for a LET_{EFF} of 48MeV-cm^2/mg. A flux of 10^5 ions/cm^2-s was used for a total fluence of 10^7 ions/cm^2. Run duration to achieve this fluence was approximately 2 minutes. The current versus time data was obtained by current monitoring the V_{DDQSNS}, V_{LDOIN}, and V_{IN} pins for each run; representative data plots for these data are shown in Figure 7-1 for DDR1 modes (the plots looked similar for all DDR modes). No discontinuous increases in current were observed in any of the three monitored signals. No SEL events were observed for any of the DDR modes under the full range of load conditions. Table 7-1 summarizes the SEL results for all DDR modes.

I_{IN} is the current for VDD or I_{VDD}

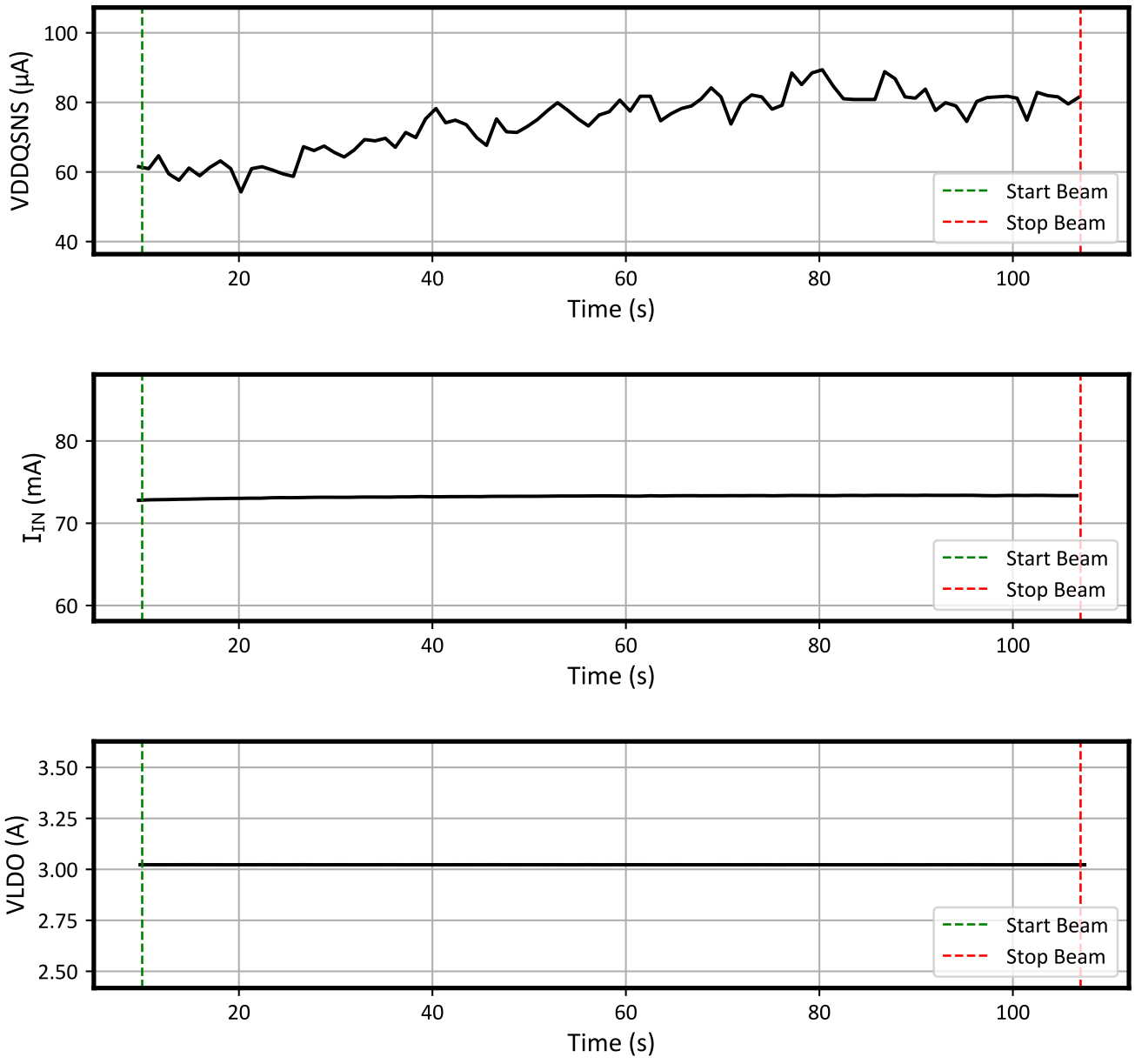


Figure 7-1. SEL Data for Sourcing 3A on V_{TT}, Sourcing 10mA on V_{TTREF}

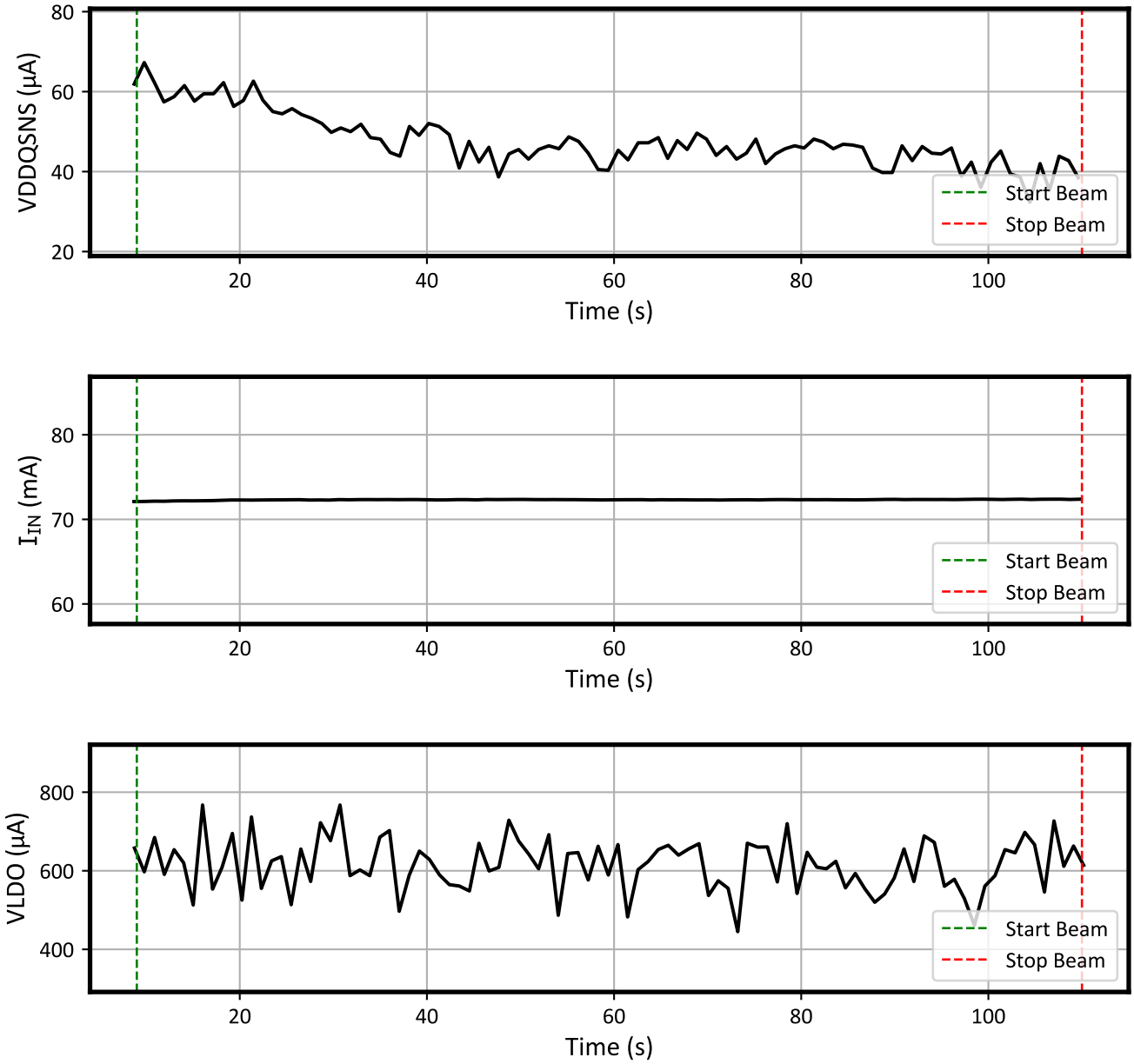


Figure 7-2. SEL Data for Sinking 3A on V_{TT}, Sourcing 10mA on V_{TTREF}

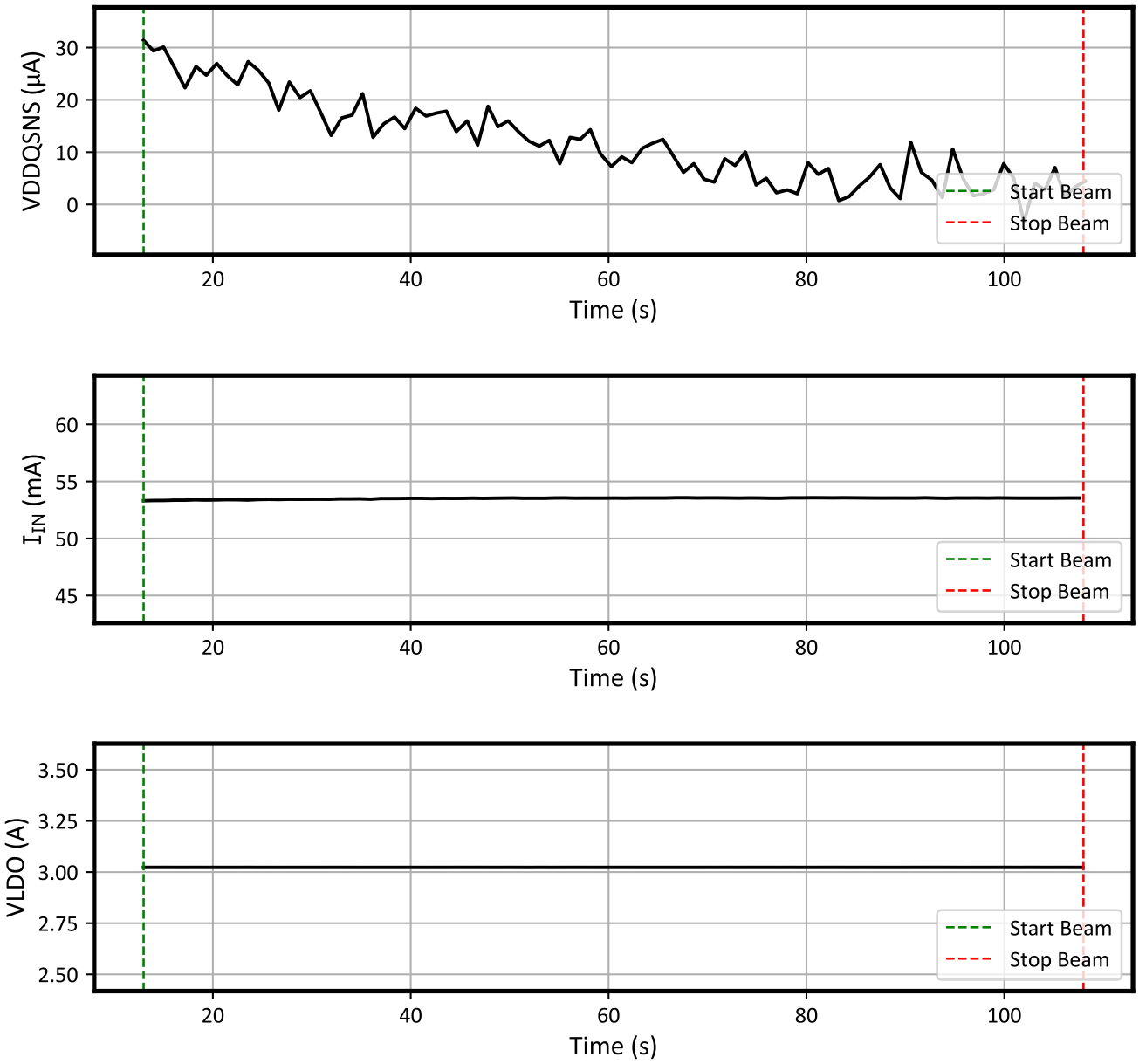


Figure 7-3. SEL Data for Sourcing 3A on V_{TT}, Sinking 10mA on V_{TTREF}

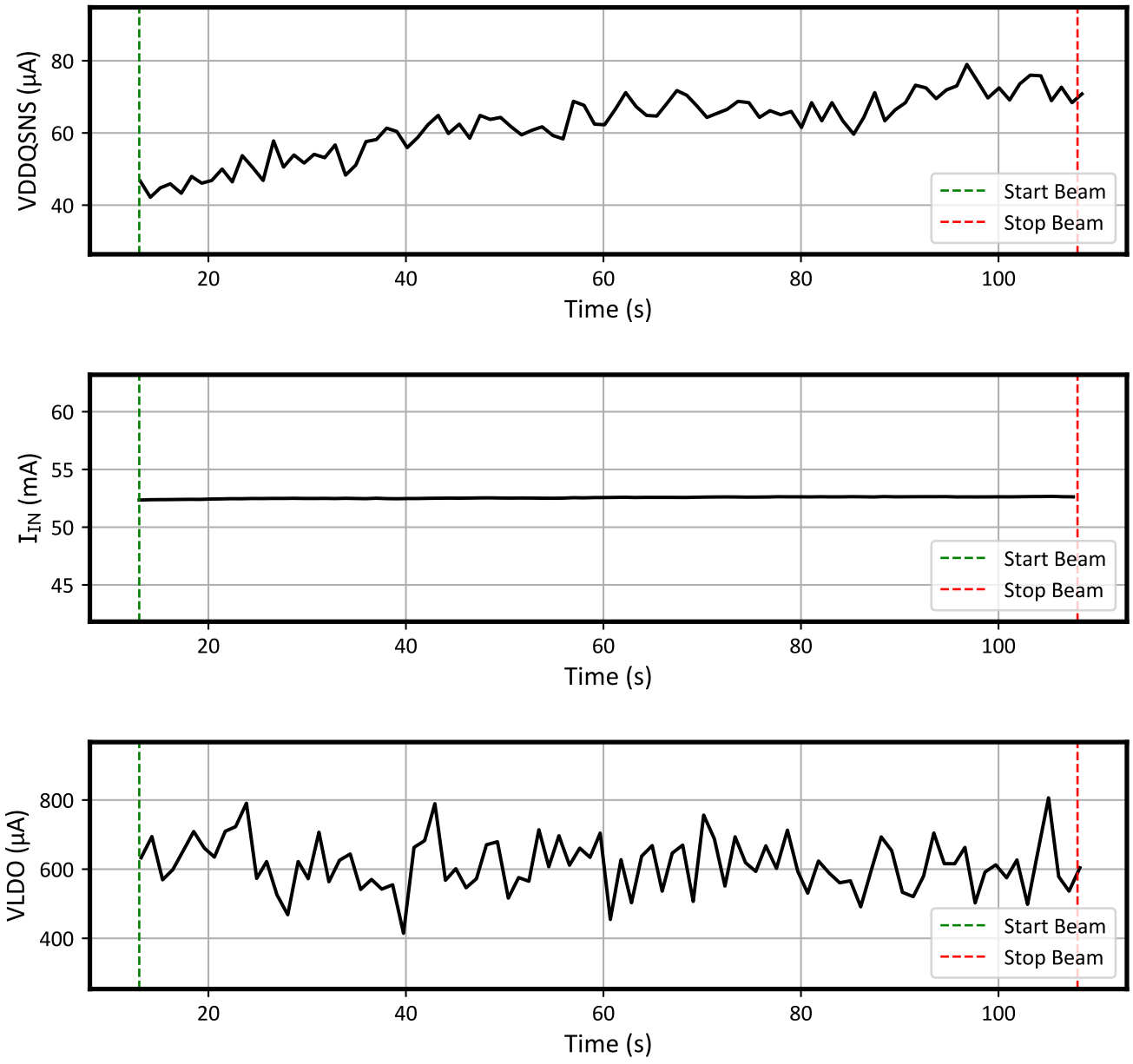


Figure 7-4. SEL Data for Sinking 3A on V_{TT}, Sinking 10mA on V_{TTREF}

Table 7-1. TPS7H3302-SEP SEL Results With T = 125°C and LET_{EFF} = 48 MeV-cm²/mg

DEVICE #	RUN #	LET_{EFF} (MeV-cm²/mg)	DDR MODE	V_{LDOIN} (V)	$V_{IN/VDD}$ (V)	V_{DDQSNS} (V)	VTT/V_O (V)	VTT/V_O LOAD (A)	V_{TTREF} LOAD (mA)	SEL?
1	1	48	DDR1	3.5	3.5	3.5	1.75	-3	–10	N
1	2	48	DDR1	3.5	3.5	3.5	1.75	-3	10	N
1	3	48	DDR1	3.5	3.5	3.5	1.75	3	10	N
1	4	48	DDR1	3.5	3.5	3.5	1.75	3	–10	N
2	5	48	DDR1	3.5	3.5	3.5	1.75	-3	–10	N
2	6	48	DDR1	3.5	3.5	3.5	1.75	3	–10	N
2	7	48	DDR1	3.5	3.5	3.5	1.75	-3	10	N
2	8	48	DDR1	3.5	3.5	3.5	1.75	3	10	N
3	9	48	DDR1	3.5	3.5	3.5	1.75	–3	–10	N
3	10	48	DDR1	3.5	3.5	3.5	1.75	3	–10	N
3	11	48	DDR1	3.5	3.5	3.5	1.75	-3	10	N
3	12	48	DDR1	3.5	3.5	3.5	1.75	3	10	N

No SEL events were observed under any of the test runs in any of the DDR modes over minimum and maximum load conditions, indicating that the TPS7H3302-SEP DDR termination regulator is *SEL-immune at T = 125°C and LET = 48MeV-cm²/mg*.

The upper-bound SEL cross section based on a 95% confidence interval (see *Appendix A* for discussion of confidence limits) for the TPS7H3302-SEP for each DDR mode is the same because the fluence for each test was identical and no SEL was observed in any DDR mode. Note that for each DDR mode the multiple tests over different load conditions were combined:

σ_{SEL} = 3.07 · 10^{-8} cm²/device for an LET = 48 MeV-cm²/mg and T = 125°C.

7.2 Single-Event-Burnout (SEB) and Single-Event-Gate-Rupture (SEGR)

During the SEB/SEGR characterization, the device was tested at around 25°C.

The species used for the SEB/SEGR testing was a Silver (^{109}Ag) with an angle-ofincidence of 0° for an LET_{EFF} = 48 MeV·cm² /mg (for more details refer to Section 5). The kinetic energy in the vacuum for ^{109}Ag is 1.634 GeV (15-MeV/ nucleon line). Flux of approximately 10^5 ions/cm² ·s and a fluence of approximately 10^7 ions/cm2 were used for the ten runs. Run duration to achieve this fluence was approximately 2 minutes. The three devices were powered up using the max device conditions for worst case destructive, with V_{IN}, V_{LDO}, and V_{DDQSNS} = 3.5V and a source and/or sink current of 0.5 or 1A on V_{TT} and a source/and/or sink current of 10mA on V_{TTREF}. The current of 0.5 or 1A was used to ensure the device could receive a load, but did not heat too much to invalidate the SEB run. The TPS7H3302-SEP was tested under enabled and disabled modes, the device was disabled by forcing 0V on the EN pin from a E36311A power supply. The PXIe-4139 were connected, even when the device was disabled, to help differentiate if an SET momentarily activated the device under the heavy-ion irradiation. During SEB/SEGR testing with the device "disabled", no V_{OUT} transient or input current events were observed. No SEB/SEGR events were observed during all fifteen runs, indicating that the TPS7H3302-SEP is SEB/SEGR-free up to LET_{EFF} = 48 MeV·cm² /mg and across the full electrical specifications. Table 7-2 shows the SEB/SEGR test conditions and results. Figure 7-2 shows a plot of the current vs time for run # 6 (Enabled) and Figure 7-3 for run # 7 (Disabled).

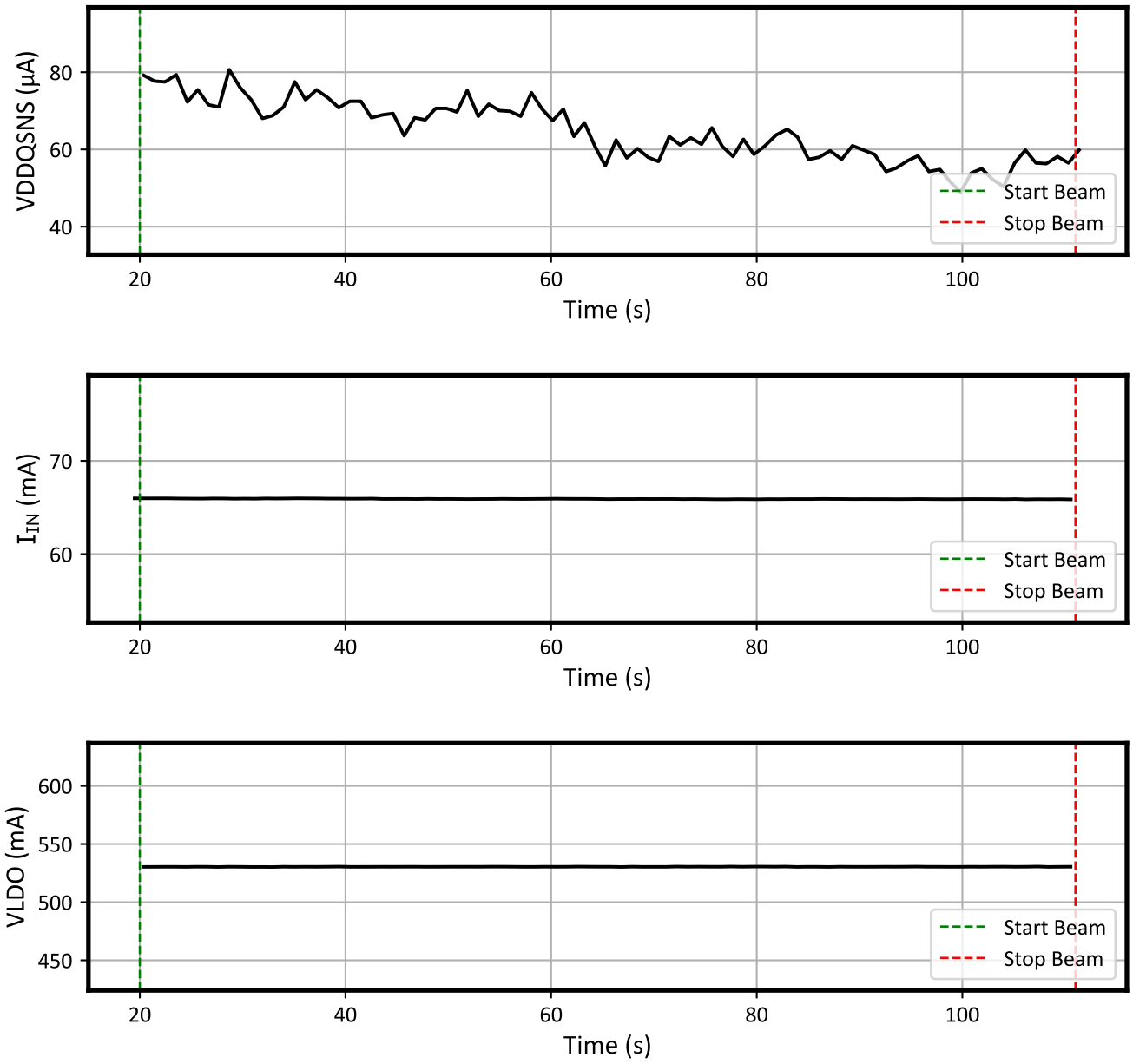


Figure 7-5. SEB-On Data for Sourcing 0.5A on V_{TT}, Sourcing 10mA on V_{TTREF}

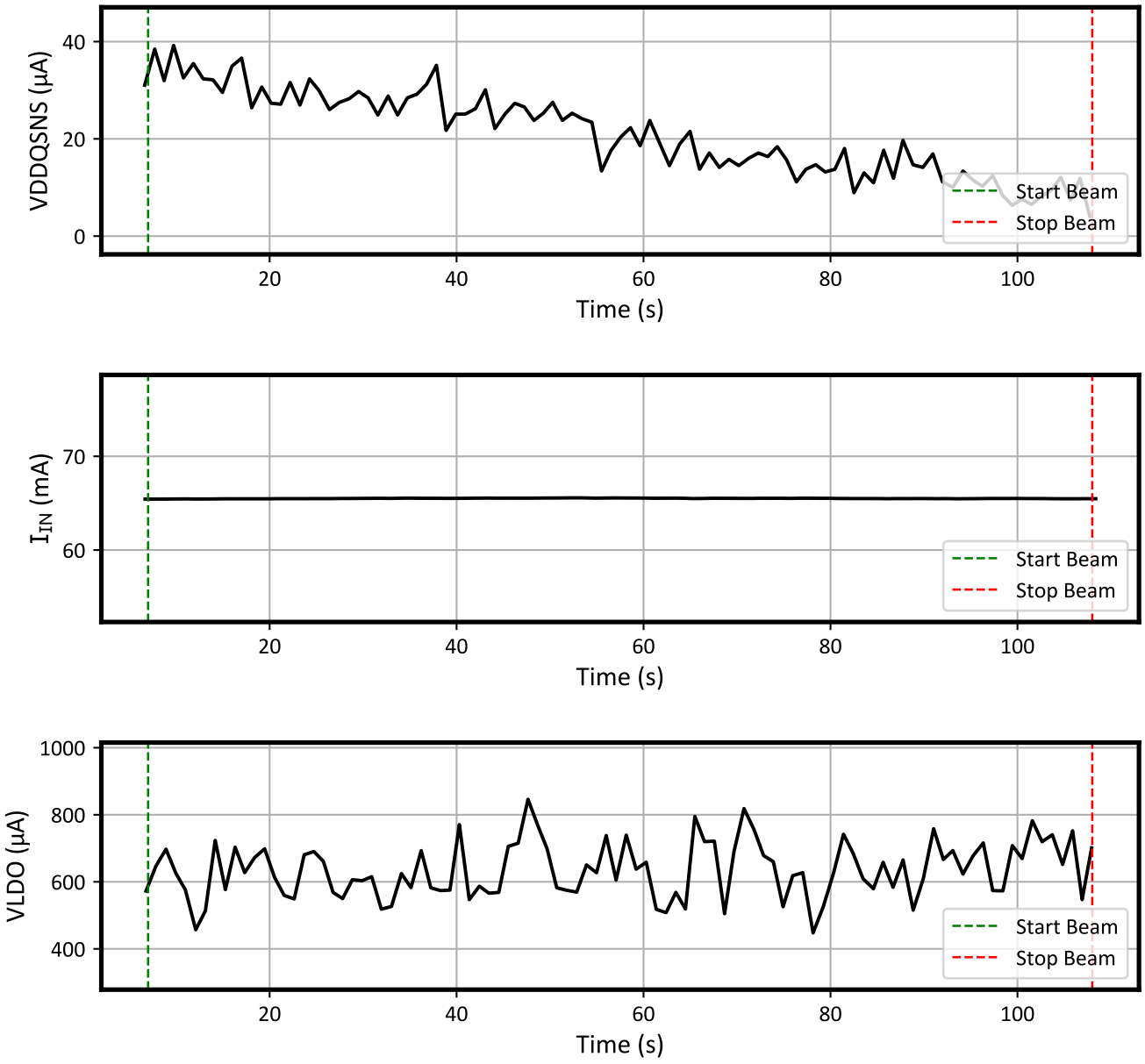


Figure 7-6. SEB-On Data for Sinking 0.5A on V_{TT}, Sourcing 10mA on V_{TTREF}

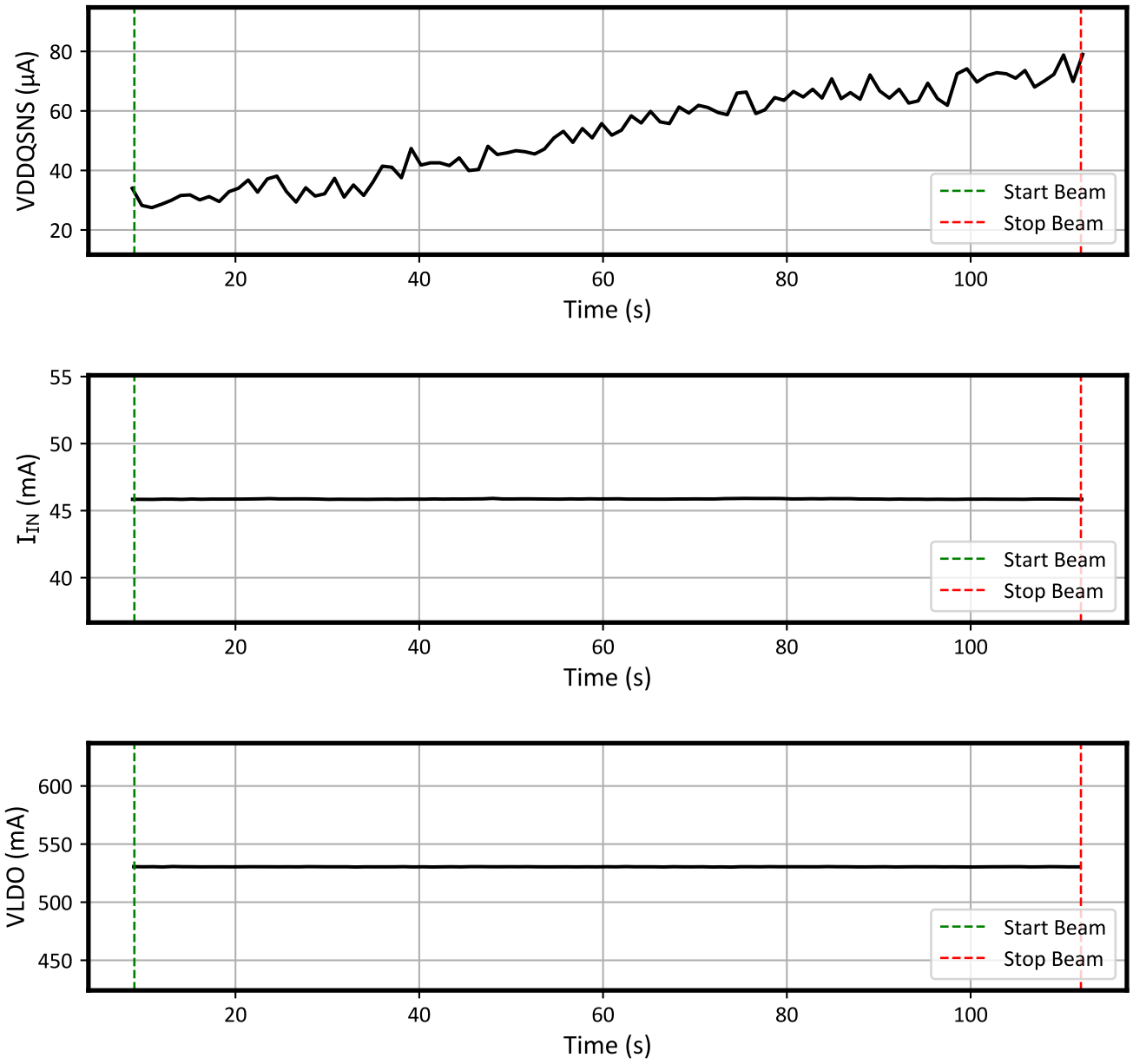


Figure 7-7. SEB-On Data for Sourcing 0.5A on V_{TT}, Sinking 10mA on V_{TTREF}

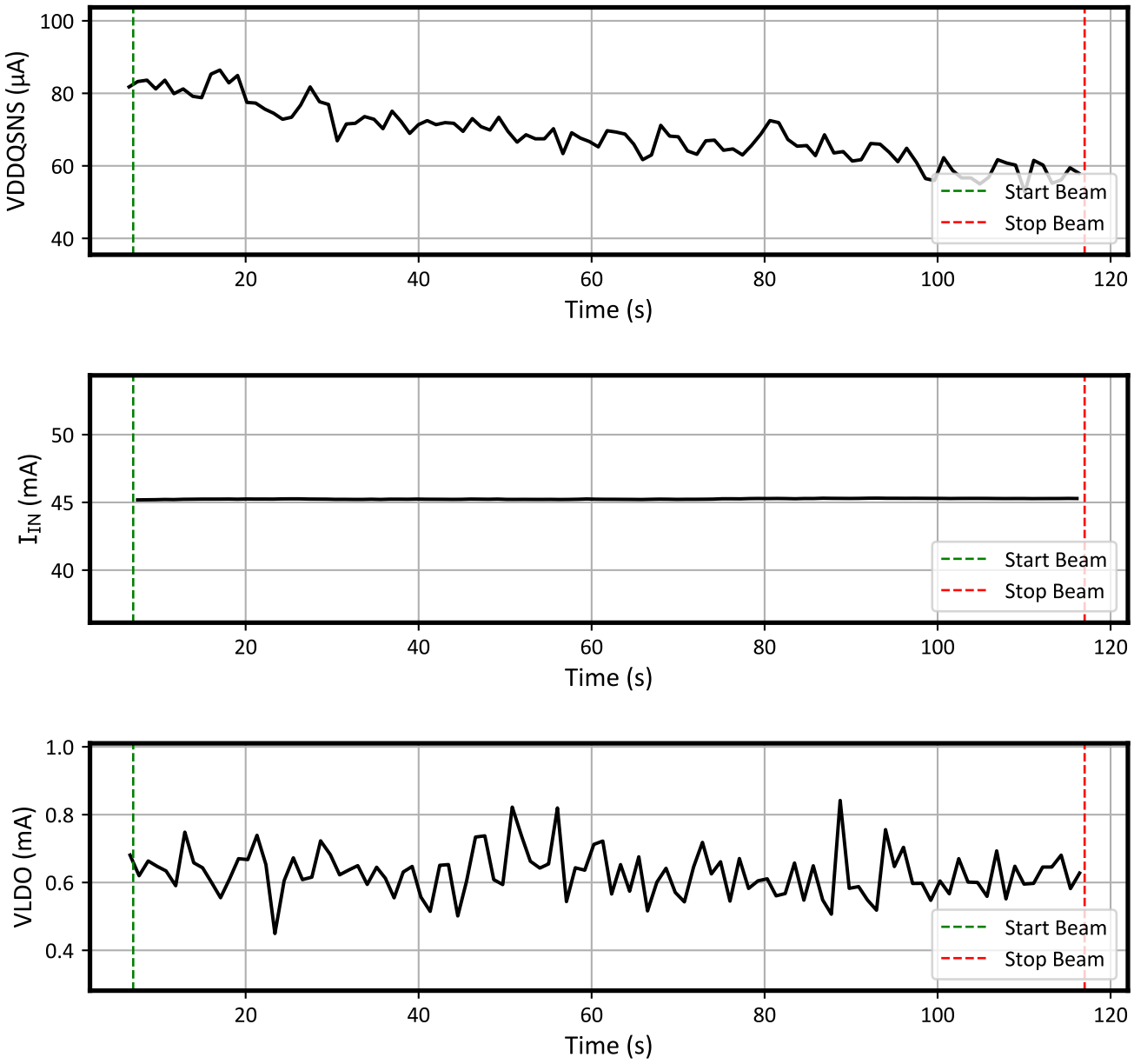


Figure 7-8. SEB-On Data for Sinking 0.5A on V_{TT}, Sinking 10mA on V_{TTREF}

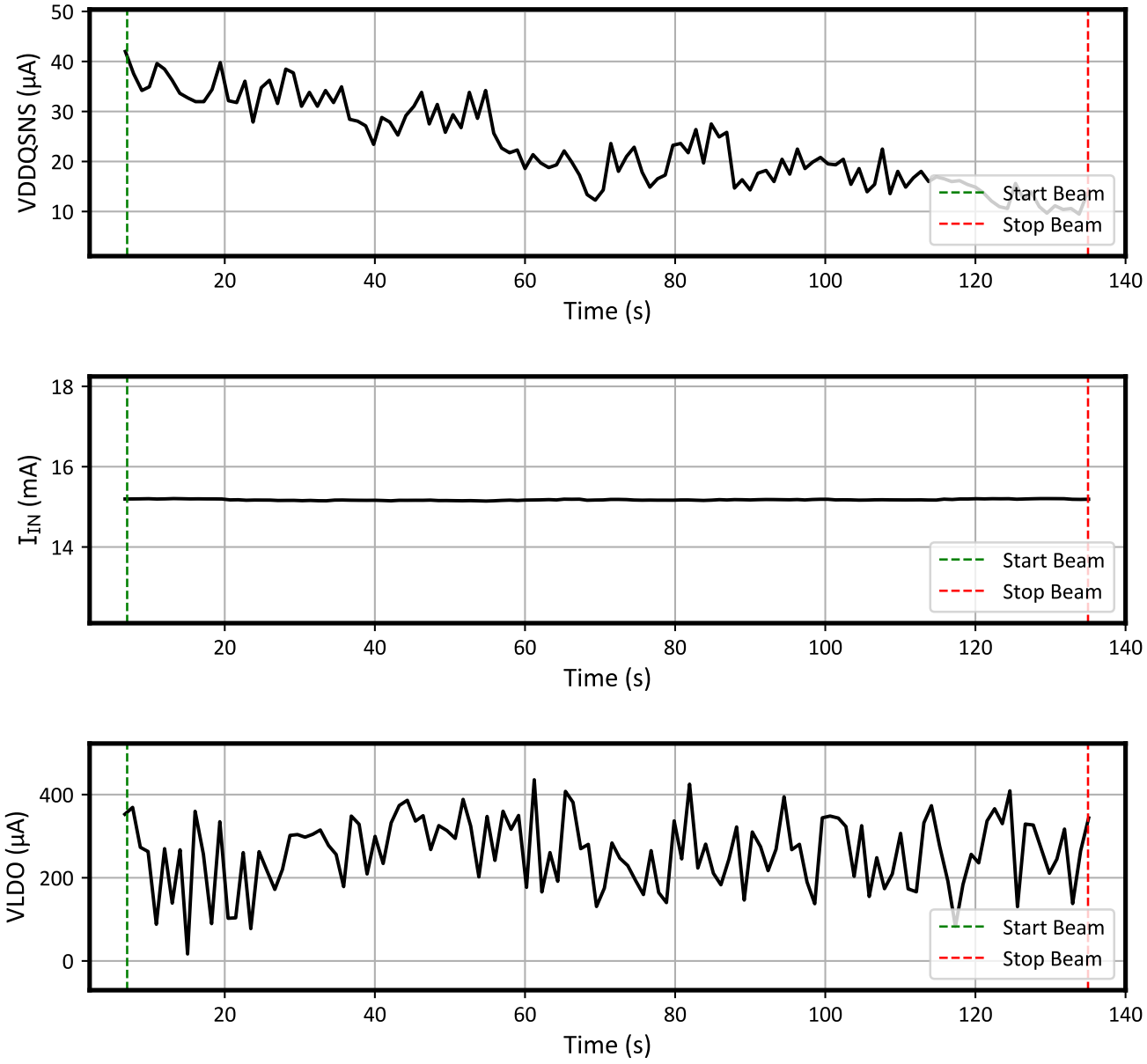


Figure 7-9. SEB-Off Data for Sinking 3A on V_{TT}, Sourcing 10mA on V_{TTREF}

Table 7-2. TPS7H3302-SEP SEB Results With T = 25°C and LET_{EFF} = 48 MeV-cm²/mg

Device #	Run #	LET_{EFF} (MeV·cm²/mg)	DDR Mode	V_{LDOIN} (V)	V_{IN}/V_{DD} (V)	V_{DDQSNS} (V)	V_{TT}/V_O (V)	V_{TT}/V_O LOAD (A)	V_{TTREF} LOAD (mA)	EN	SEB
1	13	48	DDR1	3.5	3.5	3.5	1.75	-1	-10	Y	N
1	14	48	DDR1	3.5	3.5	3.5	1.75	1	-10	Y	N
1	15	48	DDR1	3.5	3.5	3.5	1.75	0.5	10	Y	N
1	16	48	DDR1	3.5	3.5	3.5	1.75	.5	10	Y	N
1	17	48	DDR1	3.5	3.5	3.5	0	3	-10	N	N
2	18	48	DDR1	3.5	3.5	3.5	1.75	-.5	-10	Y	N
2	19	48	DDR1	3.5	3.5	3.5	1.75	.5	-10	Y	N
2	20	48	DDR1	3.5	3.5	3.5	1.75	-.5	10	Y	N
2	21	48	DDR1	3.5	3.5	3.5	1.75	.5	10	Y	N
2	22	48	DDR1	3.5	3.5	3.5	0	3	-10	N	N
3	23	48	DDR1	3.5	3.5	3.5	1.75	-.5	-10	Y	N
3	24	48	DDR1	3.5	3.5	3.5	1.75	.5	-10	Y	N
3	25	48	DDR1	3.5	3.5	3.5	1.75	-.5	10	Y	N
3	26	48	DDR1	3.5	3.5	3.5	1.75	.5	10	Y	N
3	27	48	DDR1	3.5	3.5	3.5	0	3	-10	N	N

7.3 SET and SEFI Results

The primary concern for DDR regulators like the TPS7H3302-SEP in a space environment is the occurrence of a SET that creates a transient difference exceeding ±40 mV (as per the JEDEC specification) between the nominal output (V_{TT}) and reference voltage (V_{TTREF}). Under nominal conditions, V_{TTREF} = ½ V_{TT}, where V_{TTREF} serves as a reference for memory read-write operations such that the sense amplifiers in the memories can reliably discriminate between a one and a zero data state.

Once it was determined that destructive events did not occur in the TPS7H3302-SEP, nor were any false P_{GOOD} signals (if the P_{GOOD} control circuits were sensitive it might have been possible for an ion event to generate a P_{GOOD} while the output was still valid). Thus voltage transients on the outputs induced by ions are the key concern. There are fundamentally two categories that need to be considered:

1. SET that causes a transient on output where V_{TT} – V_{TTREF} is less than ±40mV. This type of event is categorized as an SET and will NOT impact the downstream memory.
2. SET that causes a V_{TTREF} to exceed ±1% of its nominal value.

The TPS7H3302-SEP was completely SEE-free up to LET_{EFF} = 48 MeV-cm^2/mg. The regulator was also completely SEE-free up to LET_{EFF} = 48 MeV-cm^2/mg for all DDR modes.

The following are examples of captured waveforms that occurred during run #28. Note, the waveforms captured during this run were within JEDEC specifications for what is considred an SET, therefore these waveforms are there to only show how the signal reacted during the run, not showing actual SETs.

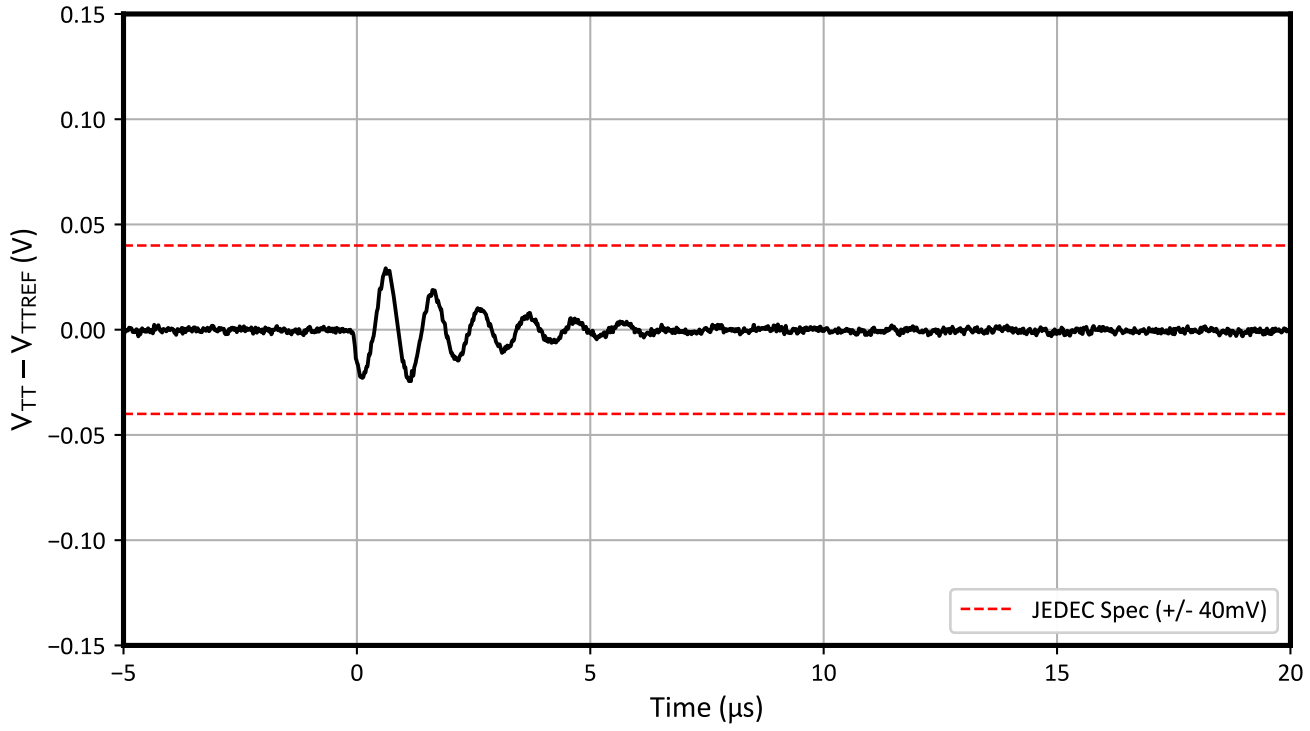


Figure 7-10. DDR1 V_{TT}-V_{TTREF} Difference is ≈ ±29 mV

7.3.1 DDR1 Mode

No SET or SEFI events of any kind were observed on any of the three TPS7H3302-SEP devices tested over 12 runs in the DDR1 mode over the full range of load conditions and a variety of input and output voltages and operating temperatures. The TPS7H3302-SEP operating in DDR1 mode is SEFI-free up to a LET_{EFF} = 48 MeV-cm^2/mg for fluences of up to 1 × 10^6 ions/cm^2. Table 9-1 shows a summary of the SET and SEFI tests.

Table 7-3. SET/SEFI Results for DDR1 Mode

DEVICE #	RUN #	LET_{EFF} (MeV-cm^2/mg)	FLUENCE (ions/cm^2)	V_{LDOIN} (V)	VDD(V)	V_{DDQSNS} (V)	VTT(V)	VTT LOAD (A)	V_{TTREF} LOAD (mA)	EVENTS ON VTT	EVENTS $V_{TT} - V_{TTREF} > 40$ mV	EVENTS ON P_{GOOD}
1	28	48	10^6	2.5	3	2.5	1.25	–1	–10	0	0	0
1	29	48	10^6	2.5	3	2.5	1.25	1	10	0	0	0
2	30	48	10^6	2.5	3	2.5	1.25	-1	-10	0	0	0
2	31	48	10^6	2.5	3	2.5	1.25	1	10	0	0	0
3	32	48	10^6	2.5	3	2.5	1.25	-1	-10	0	0	0
3	33	48	10^6	2.5	3	2.5	1.25	1	10	0	0	0

7.3.2 DDR2 Mode

No SET or SEFI events of any kind were observed on any of the three TPS7H3302-SEP devices tested over 12 runs in the DDR2 mode over the full range of load conditions and a variety of input and output voltages and operating temperatures. The TPS7H3302-SEP operating in DDR1 mode is SEFI-free up to a LET_{EFF} = 48 MeV-cm^2/mg for fluences of up to 1 × 10^6 ions/cm^2. Table 9-2 shows a summary of the SET and SEFI tests.

Table 7-4. SET/SEFI Results for DDR2 Mode

Device #	Run #	LET	Fluence	VLDOIN (V)	VDD (V)	VDDQSNS (V)	VTT (V)	VTT LOAD (A)	VTTREF LOAD (mA)	EVENTS ON VTTREF	EVENTS VTT-VTTREF ≥40mV	EVENTS ON PGOOD
1	34	48	10^6	1.8	3	1.8	0.9	-1	-10	0	0	0
1	35	48	10^6	1.8	3	1.8	0.9	1	10	0	0	0
2	36	48	10^6	1.8	3	1.8	0.9	-1	-10	0	0	0
2	37	48	10^6	1.8	3	1.8	0.9	1	10	0	0	0
3	38	48	10^6	1.8	3	1.8	0.9	-1	-10	0	0	0
3	39	48	10^6	1.8	3	1.8	0.9	1	10	0	0	0

7.3.3 DDR3 Mode

No SET or SEFI events of any kind were observed on any of the three TPS7H3302-SEP devices tested over 12 runs in the DDR3 mode over the full range of load conditions and a variety of input and output voltages and operating temperatures. The TPS7H3302-SEP operating in DDR1 mode is SEFI-free up to a LET_{EFF} = 48 MeV-cm^2/mg for fluences of up to 1 × 10^6 ions/cm^2. Table 9-3 shows a summary of the SET and SEFI tests.

Table 7-5. SET/SEFI Results for DDR3 Mode

Device #	Run #	LET	Fluence	VLDOIN (V)	VDD (V)	VDDQSNS (V)	VTT (V)	VTT LOAD (A)	VTTREF LOAD (mA)	EVENTS ON VTTREF	EVENTS VTT-VTTREF ≥40mV	EVENTS ON PGOOD
1	40	48	10^6	1.5	3	1.5	.75	-1	-10	0	0	0
1	41	48	10^6	1.5	3	1.5	.75	1	10	0	0	0
2	42	48	10^6	1.5	3	1.5	.75	-1	-10	0	0	0
2	43	48	10^6	1.5	3	1.5	.75	1	10	0	0	0
3	44	48	10^6	1.5	3	1.5	.75	-1	-10	0	0	0
3	45	48	10^6	1.5	3	1.5	.75	1	10	0	0	0

7.3.4 DDR4 Mode

No SET or SEFI events of any kind were observed on any of the three TPS7H3302-SEP devices tested over 12 runs in the DDR4 mode over the full range of load conditions and a variety of input and output voltages and operating temperatures. The TPS7H3302-SEP operating in DDR1 mode is SEFI-free up to a LET_{EFF} = 48 MeV-cm^2/mg for fluences of up to 1 × 10^6 ions/cm^2. Table 9-4 hows a summary of the SET and SEFI tests.

Table 7-6. SET/SEFI Results for DDR4

Device #	Run #	LET	Fluence	VLDOIN (V)	VDD (V)	VDDQSNS (V)	VTT (V)	VTT LOAD (A)	VTTREF LOAD (mA)	EVENTS VTTREF	EVENTS VTT-VTTREF ≥40mV	EVENTS ON PGOOD
1	46	48	10^6	1.2	3	1.2	.6	-1	-10	0	0	0
1	47	48	10^6	1.2	3	1.2	.6	1	10	0	0	0
2	48	48	10^6	1.2	3	1.2	.6	-1	-10	0	0	0
2	49	48	10^6	1.2	3	1.2	.6	1	10	0	0	0
3	50	48	10^6	1.2	3	1.2	.6	-1	-10	0	0	0
3	51	48	10^6	1.2	3	1.2	.6	1	10	0	0	0

8 Event Rate Calculations

A cross section for SET events was not calculated since, by definition, SET events were all smaller than the minimum event as specified by the JEDEC DDR specification, so SETs *have NO effect on the operation or reliability* of down-stream memory components.

Event rates were calculated for LEO(ISS) and GEO environments by combining CREME96 orbital integral flux estimations and simplified SEE cross-sections according to methods described in *Orbital Environment Estimations* section. We assume a minimum shielding configuration of 100 mils (2.54 mm) of aluminum, and "worst-week" solar activity (this is similar to a 99% upper bound for the environment). Using the 95% upper-bounds for the SEL and SEFI the event-rates of the TPS7H3302-SEP are tabulated in Table 8-1 and Table 8-3, respectively.

Table 8-1. SEL Event Rate Calculations for Worst-Week LEO and GEO Orbits

ORBIT TYPE	MODE	ONSET LET (MeV–cm^2/mg)	CREME96 INTEGRAL FLUX (/day–cm^2)	σ_{SAT} (cm^2)	EVENT RATE (/day)	EVENT RATE (FIT)	MTBE (years)
LEO(ISS)	All DDR	48	$4.50 \cdot 10^{-4}$	$3.07 \cdot 10^{-8}$	$1.38 \cdot 10^{-11}$	$5.77 \cdot 10^{-4}$	$1.98 \cdot 10^{8}$
GEO			$1.48 \cdot 10^{-3}$		$4.54 \cdot 10^{-11}$	$1.89 \cdot 10^{-3}$	$6.04 \cdot 10^{7}$

Table 8-2. SEB Event Rate Calculations for Worst-Week LEO and GEO Orbits

Orbit Type	MODE	ONSET LET (MeV-cm^2/mg)	CREME96 INTEGRAL FLUX(/day-cm^2)	σ_{SAT} (cm^2)	EVENT RATE (/day)	EVENT RATE (FIT)	MTBE (years)
LEO(ISS)	All DDR	48	$4.50 \cdot 10^{-4}$	$2.46 \cdot 10^{-8}$	$1.11 \cdot 10^{-11}$	$4.61 \cdot 10^{-4}$	$2.47 \cdot 10^{8}$
GEO			$1.48 \cdot 10^{-3}$		$3.63 \cdot 10^{-11}$	$1.51 \cdot 10^{-3}$	$7.55 \cdot 10^{7}$

Table 8-3. SEFI Event Rate Calculations for Worst-Week LEO and GEO Orbits

ORBIT TYPE	MODE	ONSET LET (MeV–cm^2/mg)	CREME96 INTEGRAL FLUX (/day–cm^2)	σ_{SAT} (cm^2)	EVENT RATE (/day)	EVENT RATE (FIT)	MTBE (years)
LEO(ISS)	All DDR	48	$4.50 \cdot 10^{-4}$	$1.54 \cdot 10^{-7}$	$6.92 \cdot 10^{-11}$	$2.88 \cdot 10^{-3}$	$3.96 \cdot 10^{7}$
GEO			$1.48 \cdot 10^{-3}$		$2.27 \cdot 10^{-10}$	$9.45 \cdot 10^{-3}$	$1.21 \cdot 10^{7}$

MTBE is the mean-time-between-events in years at the given event rates. These rates clearly demonstrate the SEE robustness of the TPS7H3302-SEP DDR Termination Regulator in two harshly conservative space environments. Customers using the TPS7H3302-SEP should only use the above estimations as a rough guide and we recommend that event rate calculations based on specific mission orbital and shielding parameters be performed to determine if the product will satisfy the reliability requirements for their specific mission.

9 Summary

The purpose of this study was to characterize the effect of heavy-ion irradiation on the single-event effect (SEE) performance of the TPS7H3302-SEP DDR termination regulator. Heavy-ions with LET_{EFF} of 48 MeV-cm^2/mg were used to irradiate three production devices in experiments with heavy-ion fluences ranging from 1×10^6 to 5×10^7 ions/cm^2 per run, over a variety of DDR modes, input and output voltage conditions, load conditions, and temperatures.

The results demonstrate that the TPS7H3302-SEP is SEE-free (no SEL, SET, or SEFI observed) under nearly all conditions up to LET_{EFF} = 48 MeV-cm^2/mg.

A Confidence Interval Calculations

For conventional products where hundreds of failures are seen during a single exposure, one can determine the average failure rate of parts being tested in a heavy-ion beam as a function of fluence with high degree of certainty and reasonably tight standard deviation, and thus have a good deal of confidence that the calculated cross section is accurate.

With radiation hardened parts however, determining the cross section becomes more difficult since often few, or even, no failures are observed during an entire exposure. Determining the cross section using an average failure rate with standard deviation is no longer a viable option, and the common practice of assuming a single error occurred at the conclusion of a null-result can end up in a greatly underestimated cross section.

In cases where observed failures are rare or non-existent, the use of confidence intervals and the chi-squared distribution is indicated. The Chi-Squared distribution is particularly well-suited for the determination of a reliability level when the failures occur at a constant rate. In the case of SEE testing, where the ion events are random in time and position within the irradiation area, one expects a failure rate that is independent of time (presuming that parametric shifts induced by the total ionizing dose do not affect the failure rate), and thus the use of chi-squared statistical techniques is valid (since events are rare an exponential or Poisson distribution is usually used).

In a typical SEE experiment, the device-under-test (DUT) is exposed to a known, fixed fluence (ions/cm^2) while the DUT is monitored for failures. This is analogous to fixed-time reliability testing and, more specifically, time-terminated testing, where the reliability test is terminated after a fixed amount of time whether or not a failure has occurred (in the case of SEE tests fluence is substituted for time and hence it is a fixed fluence test) ([17]). Calculating a confidence interval specifically provides a range of values which is likely to contain the parameter of interest (the actual number of failures/fluence). Confidence intervals are constructed at a specific confidence level. For example, a 95% confidence level implies that if a given number of units were sampled numerous times and a confidence interval estimated for each test, the resulting set of confidence intervals would bracket the true population parameter in about 95% of the cases.

In order to estimate the cross section from a null-result (no fails observed for a given fluence) with a confidence interval, we start with the standard reliability determination of lower-bound (minimum) mean-time-to-failure for fixed-time testing (an exponential distribution is assumed):

$$\mathrm{MTTF} = \frac{2nT}{\chi^2_{2(d+1);100\left(1-\frac{\alpha}{2}\right)}} \tag{1}$$

Where *MTTF* is the minimum (lower-bound) mean-time-to-failure, *n* is the number of units tested (presuming each unit is tested under identical conditions) and *T*, is the test time, and x^2 is the chi-square distribution evaluated at 100 (1 – σ / 2) confidence level and where d is the degrees-of-freedom (the number of failures observed). With slight modification for our purposes we invert the inequality and substitute *F* (fluence) in the place of *T*:

$$\mathrm{MFTF} = \frac{2nF}{\chi^2_{2(d+1);100\left(1-\frac{\alpha}{2}\right)}} \tag{2}$$

Where now *MFTF* is mean-fluence-to-failure and *F* is the test fluence, and as before, x^2 is the chi-square distribution evaluated at 100 (1 – σ / 2) confidence and where *d* is the degrees-of-freedom (the number of failures observed). The inverse relation between MTTF and failure rate is mirrored with the MFTF. Thus the upper-bound cross section is obtained by inverting the MFTF:

$$\sigma = \frac{\chi^2_{2(d+1);100\left(1-\frac{\alpha}{2}\right)}}{2nF} \tag{3}$$

Let's assume that all tests are terminated at a total fluence of 10^6 ions/cm^2. Let's also assume that we have a number of devices with very different performances that are tested under identical conditions. Assume a 95% confidence level (σ = 0.05). Note that as *d* increases from 0 events to 100 events the actual confidence interval becomes smaller, indicating that the range of values of the true value of the population parameter (in this case the cross section) is approaching the mean value + 1 standard deviation. This makes sense when one considers that as more events are observed the statistics are improved such that uncertainty in the actual device performance is reduced.

Table A-1. Experimental Example Calculation of Mean-Fluence-to-Failure (MFTF) and σ Using a 95% Confidence Interval

Degrees-of-Freedom (d)	2(d + 1)	χ^2 @ 95%	Calculated Cross Section (cm^2)		
			Upper-Bound @ 95% Confidence	Mean	Average + Standard Deviation
0	2	7.38	3.69E–06	0.00E+00	0.00E+00
1	4	11.14	5.57E–06	1.00E–06	2.00E–06
2	6	14.45	7.22E–06	2.00E–06	3.41E–06
3	8	17.53	8.77E–06	3.00E–06	4.73E–06
4	10	20.48	1.02E–05	4.00E–06	6.00E–06
5	12	23.34	1.17E–05	5.00E–06	7.24E–06
10	22	36.78	1.84E–05	1.00E–05	1.32E–05
50	102	131.84	6.59E–05	5.00E–05	5.71E–05
100	202	243.25	1.22E–04	1.00E–04	1.10E–04

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265