TEXAS INSTRUMENTS

Modular THS1206EVM

User's Guide

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Data Acquistion Products

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.3 to 5 VDC and the output voltage range of 0−5VDC.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation of the EVM. The Modular THS1206EVM is used to evaluate the 10/12-bit, 2−4 Channel, 6−8 MSPS, THS1206 family of parallel analog to digital converters. A complete circuit description, as well as schematic diagram and bill of materials are included.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1—EVM Overview
- ❏ Chapter 2—Analog and Digital Interface
- ❏ Chapter 3—Power Supplies
- ❏ Chapter 4—EVM Operation
- ❏ Chapter 5—EVM Bill of Materials and Schematic

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Data Sheets:	**Literature Number:**
THS10064	SLAS255
THS1007	SLAS286
THS10082	SLAS254
THS1009	SLAS287
THS1206	SLAS217
THS1207	SLAS284
THS12082	SLAS271
THS1209	SLAS288

Users Guides:	Literature Number:
5−6K Interface Board	SLAU104
DAP Signal Conditioning Board	SLAU105
Additional Resources:	**Literature Number:**
Op Amps for Everyone	SLOD006
Designing With the THS1206 High Speed Data Converter	SLAA094
Reading the Configuration Registers of the 10-Bit THS10064, THS1007, THS10082, and THS1009	SLAA143
Resetting Non-FIFO Variations of the 12-Bit THS1206	SLAA145

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Chapter 1

EVM Overview

This chapter provides a concise overview of the EVM.

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1.1 Features

- ❑ Full-featured evaluation board for the THS1206 family of high-speed, simultaneous sampling analog to digital converters
- ❑ Analog inputs can be configured as single-ended or differential
- ❑ Built-in reference
- ❑ High-speed parallel interface
- ❑ Compatible with the 5-6K Interface Card for use with a variety of DSP Starter Kits

1.2 Introduction

The THS1206 family consists of high-speed, low-power, 10- and 12-bit A/D converters that operate from independent 5 V Avdd and 3.0–5.25 V DVdd supplies. Independent buffer supply BVdd eliminates the need for level-shifting circuitry when the device is used with low voltage host controllers.

One common PWB can accommodate all eight devices of the THS1206 family of data converters. This includes 10- and 12-bit, two and four channel devices operating up to a maximum sampling rate of 8MSPS. The EVM layout shows the pin compatibility and upgrade path possibilities from the 10 bit, two channel THS10082 to the 12-bit four-channel THS1206.

Chapter 2

Analog and Digital Interface

This chapter provides a description of the analog and digital interfaces to the Modular THS1206EVM.

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2.1 Analog Interface

For maximum flexibility, the Modular THS1206EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient ten-pin dual row header/socket combination at J1. This header/socket provides access to the analog input pins of the ADC. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. The following table shows the pin out of the analog input connector, J1.

Pin Number	Signal	Description
J1.2	AINp	Non-inverting Input A – SE Channel 0
J1.4	AINm	Inverting input A – SE Channel 1
J1.6	BINp	Non-inverting input B – SE Channel 2
J1.8	BINm	Inverting input B – SE Channel 3
J1.10−J1.16	Unused	Pins are unused and should be left open for use with future amplifier and sensor input modules.
J1.18	REF(−)	External REFM source input (1.5 V NOM)
J1.20	REF(+)	External REFP source input (3.5 V NOM)
J1.15	REFOUT	Optional connection via W11. Provides external AFE circuitry with REFOUT bias voltage.
J1.1− J1.19 (odd)	AGND	Analog ground connections. Note J1.15 is used for REFOUT connections to external AFE circuitry.

The analog front-end (AFE) circuitry found on the EVM consists of a simple RC filter. When used in combination with the 5-6K interface card, the circuits found on both DAP signal conditioning boards (see SLAU105) provide the level shifting and amplifier configurations to realize single ended or differential mode operation of the analog to digital converter installed on the EVM.

2.2 Digital Interface

The Modular THS1206EVM is designed for easy interfacing to multiple control platforms. Jumper options are provided on the EVM to allow direct control over the state of chip select pins (/CS0 and CS1) as well as the /RD pin.

Jumper W4 controls the signal applied to the active low $\overline{CS0}$ pin. By completely removing the shunt jumper located at W4, the $\overline{CS0}$ pin is pulled low via a 10K resistor R10. Used in combination with U2, an SN74AHC138 address decoder, W4 allows the $\overline{CS0}$ signal to be controlled by one of three different addresses. Having the ability to select the address location of the ADC provides the possibility of *stacking* additional parallel ADC or DAC boards with the Modular THS1206EVM.

Jumpers W2 and W3 control signals applied to the $\overline{RD}$ and CS1 pins of the data converter. Closing the jumpers allows the signals to be applied via the parallel control connector J2. Opening the jumpers provides a logic high signal through pull up resistors R6 and R7.

2.2.1 Parallel Control

Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient ten-pin dual row header/socket combination at J2. This header/socket provides access to the digital control pins of the EVM. Consult Samtec at www.samtec.com or 1-800-SAMTEC-9 for a variety of mating connector options.

Pin Number	Signal	Description
J2.1	DC_CSa	Daughter card chip select – active low signal used to access the EVM
J2.3	$\overline{WR}$	DSP write strobe – active low signal used to initiate a conversion
J2.5	$\overline{RD}$	DSP read strobe – active low signal used to access parallel data
J2.7	EVM_A0	EVM address line 0 – used in conjunction with U2 to control $\overline{CS0}$
J2.9	EVM_A1	EVM address line 1 – used in conjunction with U2 to control $\overline{CS0}$
J2.11	EVM_A2	EVM address line 2 – used in conjunction with U2 to control $\overline{CS0}$
J2.13	EVM_A3	EVM address line 3 – used in conjunction with U2 to control $\overline{CS0}$
J2.15	EVM_A4	EVM address line 4 – not used
J2.17	TOUT	DSP timer input – optional CONVCLK or CONVST source
J2.19	INT	DSP interrupt input – connects to the ADC DATA_AV pin

2.2.2 Parallel Data

The Modular THS1206EVM uses Samtec part numbers SSW-116-22-F-D-VS-K and TSM-116-01-T-DV-P to provide a convenient 16-pin dual row header/socket combination at J3. This header/socket combination provides access to the parallel data pins of the THS1206. Data line D0 is connected to J3 pin 1. Data lines 1−11 are located on pins 3−31 respectively. Even-numbered pins (2 through 32) are connected to digital ground.

2.2.3 Two-Channel Device Options

When used with two channels devices, parallel data connector pin J3.25 is connected to the OVRFL signal found on the ADC. This is accommodated by shorting pin 2−3 of jumper W8. This allows the user to observe the FIFO over flow condition of the ADC directly through the host processor data bus.

The hardware reset pin ($\overline{\text{RST}}$) found on two channels devices can be activated by a distinct address location via U2 and EVM_A0 through EVM_A3 located on the parallel control connector J2. Reset is activated by driving all four address lines high. Reset is an asynchronous function that restores the configuration registers to their default states, and resets the FIFO read and write pointers.

Chapter 3

Power Supplies

This chapter describes the power supplies reguired to operate the Modular THS1206EVM.

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3.1 Requirements

The Modular THS1206EVM board requires 5 V dc for the analog section of the ADC. The digital supply (DVdd) and buffer supply (BVdd) can range from 3 V to 5.25 V. Since the EVM is designed to work with the 5-6K interface board, JP1 provides direct connection to the common power bus described in document number SLAU104. Jumpers W9 and W10 should be closed; jumper W6 provides BVdd options of 5.0 V or 3.3 V.

The following table shows the pin out of JP1:

Signal	Pin Number		Signal
Unused	1	2	Unused
+5VA	3	4	Unused
DGND	5	6	AGND
Unused	7	8	Unused
+3.3VD	9	10	+5VD

Alternate power sources can be applied via various test points located on the EVM. Refer to the schematic at the end of this document for details. Removing jumpers W6, W9, and W10 allow the AVdd, DVdd and BVdd voltages to be applied from completely independent, variable dc sources.

Note: While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.

3.2 Reference Voltages

The Modular THS1206EVM is configured to use its internal reference through jumper W1 (see schematic for details). If an external reference is desired, remove the shunt jumper on W1 and apply the external reference source to the test point labeled REFIN.

External voltages can also be applied to the REFM and REFP test points if the device is configured to use the external voltage option, set in configuration register one (CR1).

Chapter 4

EVM Operation

The analog input swing is 2 Vpp, centered on a 2.5 V internal or external reference. The devices accept bipolar input ranges when a level shift circuit is used in the analog front-end circuitry. Refer to Section 12 of *Op Amps for Everyone* (SLOD006) for information on various circuit applications.

Once power is applied to the EVM, the analog input source can be connected directly to J1 (top or bottom side) or through optional amplifier and signal conditioning modules using the 5−6K interface board. The analog input level should not exceed 2.0 Vp-p. The analog input range is from REFM to REFP (2 Vpp) centered at 2.5 V.

The digital control signals can be applied directly to J2 (top or bottom side). The Modular THS1206EVM can also be connected directly to the 5−6K interface board for use with a variety of C5000™ DSP platform and C6000™ DSP platform starter kits (DSK). The parallel control and data connectors are designed to allow pattern generators and/or logic analyzers to be connected to the EVM using standard ribbon type cables on 0.1-inch centers.

No specific evaluation software is provided with this EVM. However, various code examples are available that show how to use this EVM with a variety of digital signal processors from Texas Instruments. Check the product folders or send e-mail to dataconvapps@list.ti.com for a listing of available code examples. The EVM Gerber files are available on request.

Chapter 5

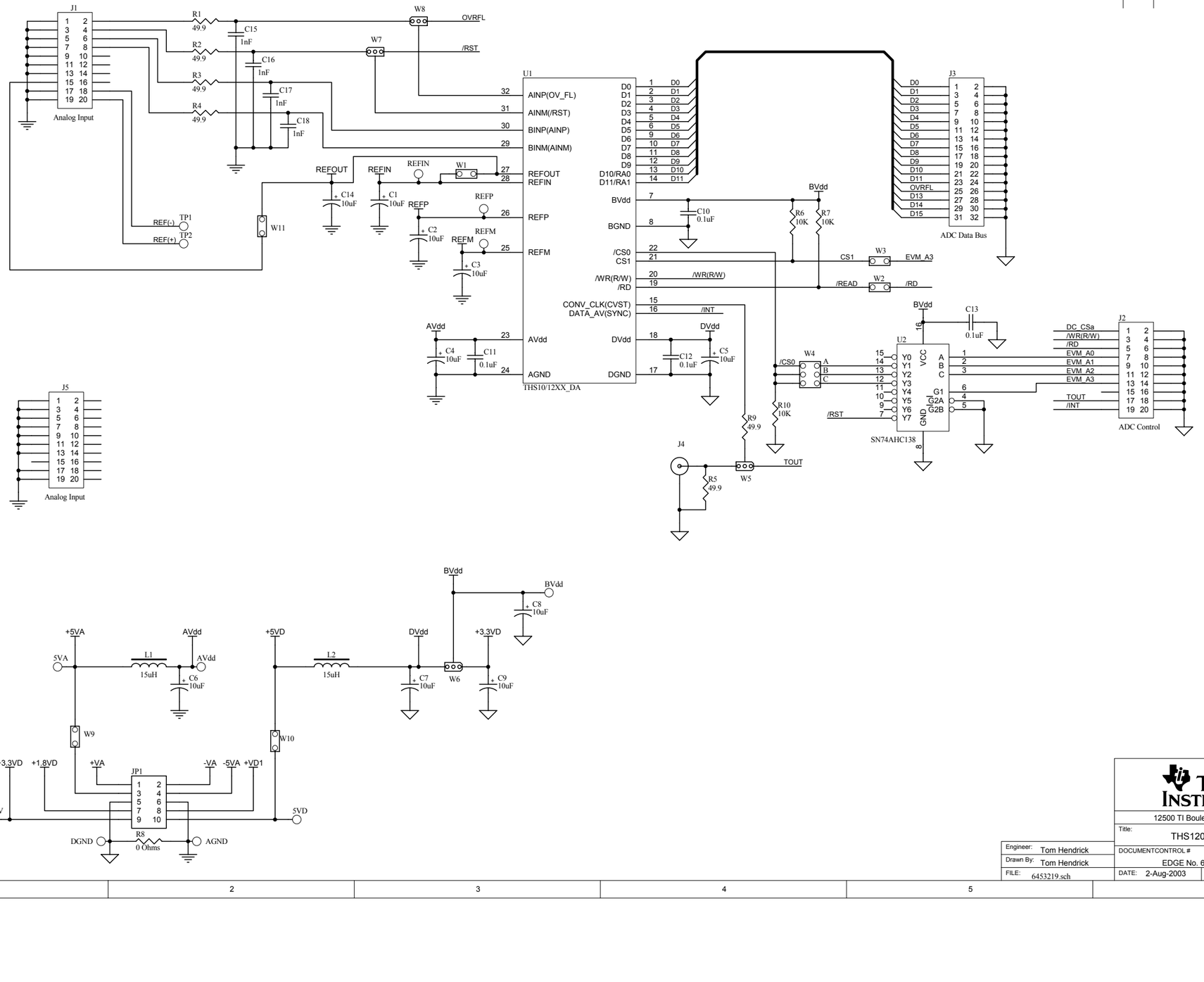
EVM Bill of Materials and Schematic

The following table contains a complete bill of materials for the Modular THS1206EVM. The schematic diagram is also provided for reference.

Designators	Description	Manufacturer	Mfg. Part Number
C1 C2 C3 C4 C5 C14	10 µF, A case, tantalum, 10 V	Panasonic	ECS-T1AY106R
C6 C7 C8 C9	10 µF, B case, tantalum, 20 V	Panasonic	ECS-T1DX106R
C10 C11 C12 C13	0.1 µF, 0805, ceramic, X7R, 50 V, 10%	Panasonic	ECJ-2YB1H104K
C15 C16 C17 C18	1 nF, 0805, ceramic, X7R, 50 V, 10%	Panasonic	ECJ-2VB1H102K
J1 J2 J5 (top side)	10 Pin, dual-row SMT header (20 positive)	Samtec	TSM-110-01-T-DV-P
J1 J2 J5 (bottom side)	10 Pin, dual-row SMT socket (20 positive)	Samtec	SSW-110-22-F-D-VS-K
J3 (top side)	16 Pin, dual-row SMT header (32 positive)	Samtec	TSM-116-01-T-DV-P
J3 (bottom side)	16 Pin, dual-row SMT socket (32 positive)	Samtec	SSW-116-22-F-D-V-K
J4	Not installed		
JP1 (top side)	5 Pin, dual-row, SMT header (10 positive)	Samtec	TSM-105-0-T-D-P
JP1 (bottom side)	5 Pin, dual-row, SMT socket (10 positive)	Samtec	SSW-105-22-F-D-VS-K
L1 L2	15 µH inductor, SMT, 1608 series	Inductors, Inc.	CTDS1608C-153
R6 R7 R10	10 KΩ, 0805, 5%, 0.1 W resistor	Yageo America	9C08052A1002JLHFT
R1 R2 R3 R4 R5	49.9 Ω, 0805, 1% 0.1 W resistor	Yageo America	9C08052A49R9FKHFT
R8	0 Ω, 0805, 0.1 W resistor	Yageo America	9C08052A0R00JLHFT
Various	Red test point loop	Keystone	5000
Various	Black test point loop	Keystone	5001
U1	THS1206	TI	See NOTE
U2	SN74AHC138	TI	SN74AHC138D
W1 W2 W3 W9 W10 W11	2 Pin , 0.1-inch header	Samtec	TSW-102-07-L-S
W4	3 Pin, dual-row, TH header (6 positive)	Samtec	TSW-103-07-L-D
W5 W6	3 Pin , 0.1-inch header	Samtec	TSW-103-07-L-S

Note: U1 may be replaced with THS1064CDA, THS1007CDA, THS10082CDA, THS1009CDA, THS1207CDA, THS12082CDA, or THS1209CDA as required.

Revision History		
REV	ECN Number	Approved
A	Initial Release	TH



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