Application Report
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Advanced Sequencing and Monitoring Using the UCD9081

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ABSTRACT

This application report describes how to design a custom sequencing and monitoring solution using the UCD9081. Hardware implementation details and use of the GUI are included. The application report, the UCD9081 data sheet, and the UCD9081EVM User's Guide provide information that can assist in the design and implementation of custom power supply sequencing solutions.

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1 Power System Monitoring and Sequencing with the UCD9081

The UCD9081 is a single, low-power (~3 mA at 3.3 V) integrated circuit in a 32-pin, quad-flatpack package (RHB) that monitors and sequences up to eight independent power supplies. The voltage at each rail and the status of each supply are reported to the user's system via the I²C™ bus. Each of the eight power-supply enables (ENx) and up to four general-purpose outputs (GPOx) can be configured to turn on in proper sequence based on a combination of user-defined parameters including:

- Elapsed time after a reset or sequence event
- Time delay after another power supply reaches regulation
- Voltage of another power supply

The power supply enables and GPOs can be configured to shut down in a controlled manner at specific times following a shutdown event.

An intuitive Windows™-based graphical user interface (GUI) provides a powerful tool for configuring the UCD9081. The UCD9081 GUI can communicate from a personal computer USB port to the UCD9081 through a USB-to-I2C interface adapter available from Texas Instruments. A connector with the UCD9081 clock, data pins, and ground on it is necessary to take advantage of this communication capability. An example is shown in the UCD9081EVM schematic of the UCD9081EVM user's guide (SLVU249). The GUI can then be used to configure the UCD9081 and to monitor operation of the sequencing system. Sequencing parameter files (*.par) developed using the EVM or on other designs can be loaded by the GUI as a starting point for a new design. After the final sequencing configuration is complete, the GUI or any other I²C™ master device can be used to configure the UCD9081. Alternatively, the GUI can build a standard Intel format *.hex file that a third-party device programmer can load into the UCD9081. Additional details can be found in the *Configuring the UCD9081* section of the data sheet (SLVS813) or in the *Programming the UCD9080* application report (SLUA441).

1.1 Power Supply Monitoring

The UCD9081 has eight voltage monitor inputs (MONx) that are multiplexed to a single, 10-bit, analog-to-digital converter (ADC). The ADC converts MONx inputs ranging from 0 volts to the ADC reference voltage. The ADC has an internal 2.5-V voltage reference or an external reference tied to V_{CC} can be used. The 2.5-V internal voltage reference has an accuracy of ±150 mV, which does not provide good enough accuracy for monitoring system voltages in most applications. If V_{CC} is used, then the reference voltage accuracy is as good as the accuracy of the external V_{CC}. Detailed specifications of the ADC total accuracy can be found in the data sheet.

The UCD9081 can monitor voltages higher than the reference voltage if a resistor divider network is used, so that the voltages at the MONx inputs are no larger than the reference voltage. The source impedance of the divider network must be kept below about 15 kΩ to ensure that the rise times on the internal MONx sample-and-hold capacitor are much faster than the ADC conversion time. The data sheet provides information about proper selection of the scaling resistors.

An I²C master can read the voltages from each MONx input. Each MONx input can be used as part of the sequencing criteria or to trigger system alarms and cause shutdowns.

1.2 Power Supply Sequencing

The MONx voltage monitoring inputs are directly linked to power supply enable pins (ENx) and can be configured through the GUI to control up to four general-purpose outputs (GPOx). During a sequencing event, each ENx pin can be configured to be either active low or active high and can be configured to assert based on a user-specified time delay following startup (**Time**), after a parent rail reaches regulation (**Parent (Reg)**) or after a parent rail achieves a specific voltage (**Parent (V)**). A rail also can be monitored without asserting the corresponding ENx pin (**None**). Even if **None** is selected for a rail, any configured Alarm Processing will be observed.

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1.3 Shutdown Sequencing

For many applications, rail shutdown order and timing is as important as startup order and timing. The UCD9081 can be configured through the GUI to shut down each rail and GPO based on shutdown delay times specified in milliseconds. The shutdown delay times define how long each rail or GPO waits after a shutdown command is generated before disabling the appropriate ENx pin or GPO.

1.4 Rail Errors

Once the ENx pins have been asserted, the UCD9081 compares the rail voltages on the MONx inputs to user settings for undervoltage (UV) and overvoltage (OV) conditions. UV and OV thresholds define the in-regulation boundaries for the rail. If the rail voltage is within the UV and OV settings, then the rail is in regulation.

Errors can occur at start-up if a rail does not achieve regulation within a user-specified **Max Time for Regulation (MTFR)**. Errors also can be flagged after regulation is achieved if a rail is outside of the UV and OV limits for longer than the user-specified **Out of Reg Time (OORW)** or **Glitch Width**. The UCD9081 can either record or **Ignore Glitch Alarms**. This choice has no impact on the monitoring or sequencing of a rail.

1.5 Alarm Processing

When a fault is detected, even on a nonsequenced rail, the UCD9081 provides a number of *Alarm Processing* options:

- **Ignore –** The UCD9081 takes no action when faults occur.
- **Log Only –** Faults are logged to on-chip memory, and no other action is taken.
- **Retry n Times –** The ENx pin is disabled for approximately 5 ms and then enabled again 0, 1, 2, 3, or 4 times to try and restore the power supply to regulation.
- **Retry Continuously –** The ENx pin is disabled for approximately 5 ms and then enabled again until the rail either reaches regulation or the system is turned off.
- **Sequence –** The configured shutdown sequence is ignored in this case. All rails and GPOs are immediately disabled, followed by initiation of a start-up sequence.

Alarm Processing options are not carried out when a dependent rail is disabled by a parent rail.

However, if any dependent rails have other rails or GPOs marked as dependents, those dependent rails or GPOs are sequenced off. Use Retry 0 Times and the appropriate dependencies to configure the UCD9081 to initiate a shutdown sequence in response to a fault on a specific rail.

1.6 Error Logging

The UCD9081 can log errors in two ways. All errors are stored in on-chip memory and retrieved over the I^2C bus. The error log includes a time stamp that shows the elapsed time since the UCD9081 was last reset, the rail number, the type of error, and the voltage measured on the rail at the time of the error.

The UCD9081 **Log Errors to Flash** feature allows the user to log errors on critical rails to flash memory for later review, even if power is lost. This provides a useful tool to help troubleshoot failure mechanisms. The Flash Error Log can be read and cleared by a master I^2C device using the procedure outlined in the data sheet.

1.7 Dependent Rails and GPOs

Any monitored voltage rail can shut down any other rail or GPO according to user-specified delay times if the monitored rail is shut down. A rail can be shut down if **Retry n Times** is unsuccessful at bringing it back into regulation, or if a parent rail forces it to shut down. A rail set to **Sequence** causes all rails and GPOs to shut down immediately. Although Alarm Processing options are ignored when a dependent rail is disabled by a parent rail, other rails or GPOs selected to shut down by the dependent rail do shut down. Cascaded dependencies and an example of dependent rail behavior are shown in Section 3.

1.8 Using Multiple UCD9081 ICs

For applications that require sequencing of more than eight voltage rails, multiple UCD9081 integrated circuits (IC) can be used, either independently but connected to a single I^2C bus or by cascading devices. When using multiple, independently configured UCD9081 ICs in a design, each device is given a unique I^2C address. The UCD9081 supports up to 16 I^2C addresses. The GUI can be used to communicate independently with each device. An example of how to cascade multiple devices is given in Section 3.

2 GUI Operation

The UCD9081 can be configured and monitored via I^2C using a Windows-based GUI. The GUI can be used with the UCD9081EVM or with a user's design to configure all available options, such as sequencing and shutdown order, over/undervoltage limits and timing, logging of rail errors to flash memory, and other configurable features. It also can be used to monitor the system power by reporting current readings of voltage and error conditions on all the rails.

A detailed description of how to use the GUI with the UCD9081EVM is given in the UCD9081EVM user's guide (SLVU249).

2.1 UCD9081 GUI Main Window

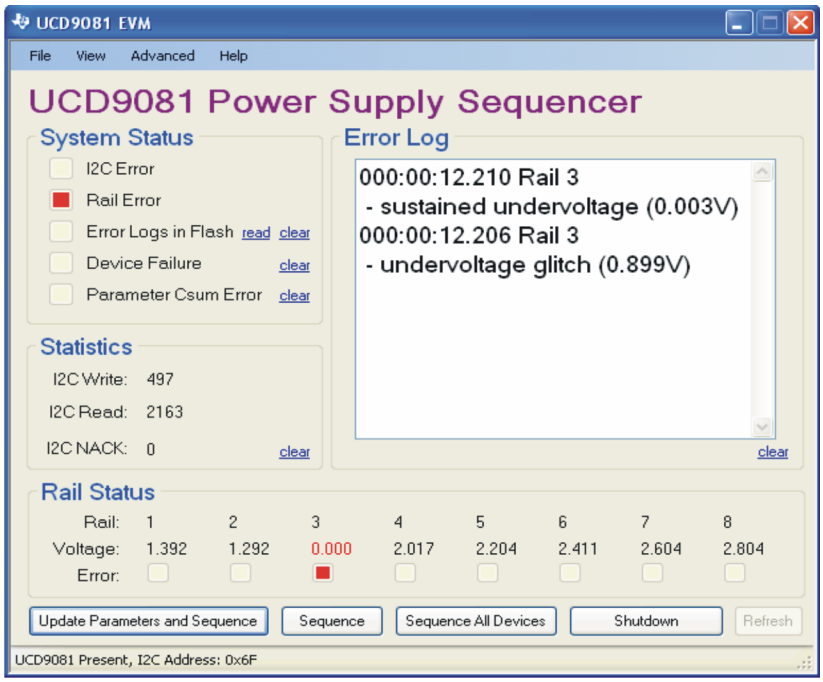


Figure 1. UCD9081 GUI Main Window

The GUI main window, shown in Figure 1, displays the current status and voltage of each rail. The main window menu functions provide access for the user to input the start-up and shutdown configurations. The GUI main window has the following areas:

- **System Status** – shows device errors including **I2C Error, Rail Error, Device Failure, and Parameter Csum** (Checksum) **Error**. A filled red box (Figure 1) indicates an error. The clear buttons to the right of each error provide a means to reset the errors.
  - **I2C Error –** communication error between the GUI and the UCD9081.
  - **Rail Error –** one of the monitored rails has an UV, OV or Failed to Reach Regulation error.
  - **Error Logs in Flash –** indicates that errors have been stored in nonvolatile flash memory on the UCD9081.
  - **Device Failure –** the UCD9081 in question is unusable, typically because a value has been written to an improper memory location. In most cases, the UCD9081 will detect the error and repair the memory location.

  - **Parameter Csum Error –** indicates that the user-defined configuration parameters were incorrectly stored in the UCD9081. If the configuration file was generated using the GUI, then this error can only be due to an interruption in communication while the parameter file was being stored to the device. If the parameter file was created outside of the GUI, then this error can be due to a parameter file with an incorrect or nonexistent checksum. To proceed within the GUI, clear the error and click the Update Parameters and Sequence button again.

- **Statistics –** I^2C communication statistics. Shows number of GUI I^2C Writes, Reads, and NACKs (Not Acknowledged) events. A NACK represents an I^2C communication problem. Multiple NACKs indicate a problem with the I^2C bus.
- **Rail Status –** Shows rail error status and monitored voltage of each rail. The voltage applied to the MONx inputs cannot exceed the ADC reference voltage. However, voltages higher than the reference can be monitored by using resistors to reduce the MONx voltage. Actual external resistor values that are used in the design can be entered in the Rail Configuration window shown in Figure 9. The GUI uses the resistor values to scale the displayed voltages to match the actual rail voltages. The **Pull-up** and **Pull-down** resistor values for a rail must be set to 0.00 if the rail voltage is applied directly to the MONx input.
  - **Update Parameters and Sequence button –** Updates buffer-stored GUI information input by the user in the Rail Configuration, System Configuration, GPO Configuration or User Data windows to device program flash memory and initiates a device sequence. This process takes less than a second.
  - **Sequence button –** Initiates a system sequence to a single device using current sequencing parameters. This is accomplished by sending a sequence command (0x00) to the RESTART (0x2F) register over the I^2C bus.
  - **Sequence All Devices button –** Initiates a system sequence to all devices on the I^2C bus using current sequencing parameters.
  - **Shutdown button –** Shuts down all rails and GPOs according to the time delays specified in the system shutdown configuration by writing 0xC0 to the RESTART register.
  - **Refresh button –** Manually updates the measured voltages and errors of all monitored voltage rails if Auto Refresh is not selected under the File menu.

- **Error Log –** Contains error messages corresponding to errors flagged in System Status. Errors can be logged in on-chip memory in an eight-deep FIFO located in volatile memory and displayed in the GUI error log in black text, as shown in Figure 1. On-chip memory errors also can be read by an I^2C master device but are not retained in the UCD9081 after a power cycle. Errors read from on-chip memory by an I^2C master are removed from the FIFO, creating room to write additional errors.

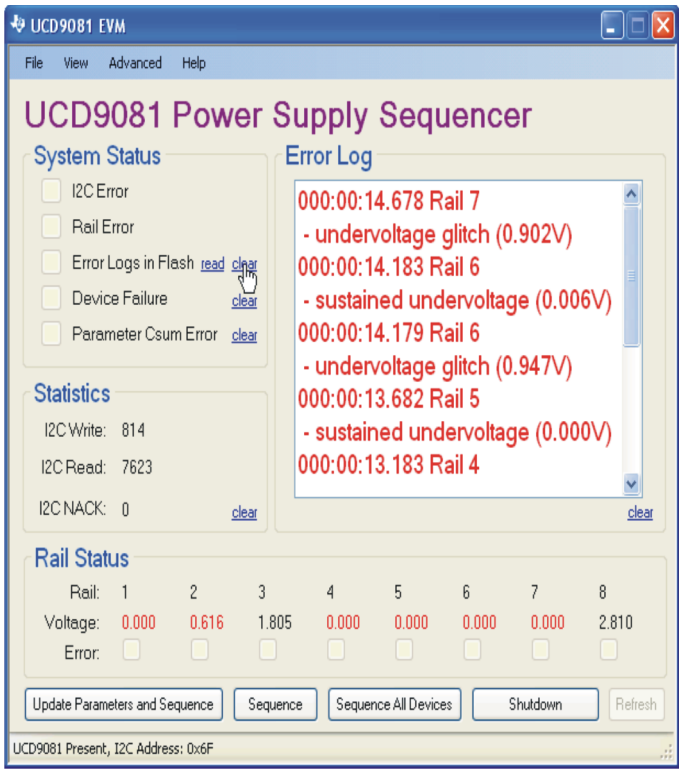


Figure 2. Clearing Errors Logged in Flash Memory

Errors are posted in the UCD9081 according to the configuration for a rail. If the user has specified **Ignore Glitches** for a rail, UV and OV events shorter than OORW are not posted to the error log. If the user has specified **Ignore** as the alarm response, no errors are posted to the error log for that rail. All other alarm responses result in the error condition being logged. Due to the unknown latency of the I^2C master extracting data from the FIFO, the UCD9081 only posts to the FIFO if it has room to write. If this FIFO is full and cannot be written to, the monitoring operation is unaffected.

The second method of error logging provides a way for users to store errors in nonvolatile or flash memory and to review the errors after power has been removed from the UCD9081. Similar to errors logged in on-chip memory, faults are logged for all rails that have the appropriate alarm processing options selected. In this case, errors are posted to both the on-chip memory FIFO and the Flash Error Log. The UCD9081 is capable of recording up to eight entries in the Flash Error Log. Errors are only posted to the Flash Error Log if there is room to write. The monitoring operation is unaffected if the Flash Error Log is full and cannot be written to. The Flash Error Log can only be read following a device RESET.

An **Ignore Flash Error Log** checkbox is in the System Configuration window (Figure 7). If the box is left unchecked, the UCD9081 is held in RESET after a RESTART if entries are detected in the Flash Error Log. The device remains in RESET until the Error Log is read and cleared. If the box is checked, the UCD9081 restarts whether or not entries are in the Flash Error Log. In applications that require review of the Flash Error Log after a shutdown occurs on a critical rail, this box must not be left unchecked to ensure that the user is able to review the Flash Error Log data before it is cleared. For applications in which it is critical that the system try to restart whenever possible, check this box. Note that if the device starts without clearing the Flash Error Log, it might be full at start-up, leaving no room for new faults to be stored. A ***clear*** button to the right of the Error Logs in Flash indicator in the GUI main window can be used to empty the Flash Error Log (Figure 2).

- **Menu bar –** user can select *File, View, Advanced*, and *Help* menu items. *File* and *View* include the primary UCD9081 configuration parameters. Later sections of this application report contain detailed descriptions of each option.

2.2 File Menu Options

The **File** menu includes the following commands:

- **Load Configuration –** loads a previously saved parameter (*.par) file into the UCD9081. The *.par files contain custom user configurations saved in a proprietary TI format.

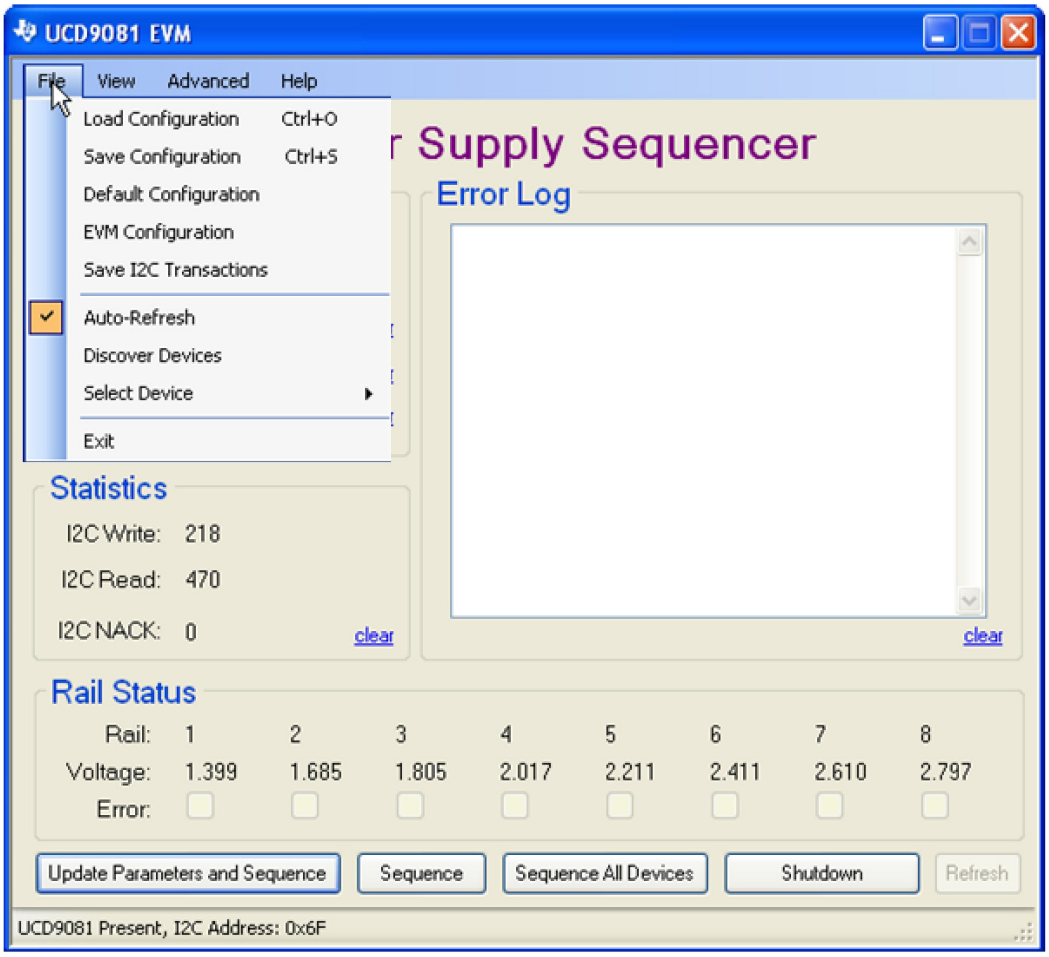


Figure 3. File Tab From Main Window Menu Bar

- **Save Configuration –** saves the current UCD9081 configuration to a user parameter (*.par) file. The parameter files can be loaded into the device by the user. This command can also generate a *.hex file, which can be used to configure the UCD9081 in production, independent of the GUI.

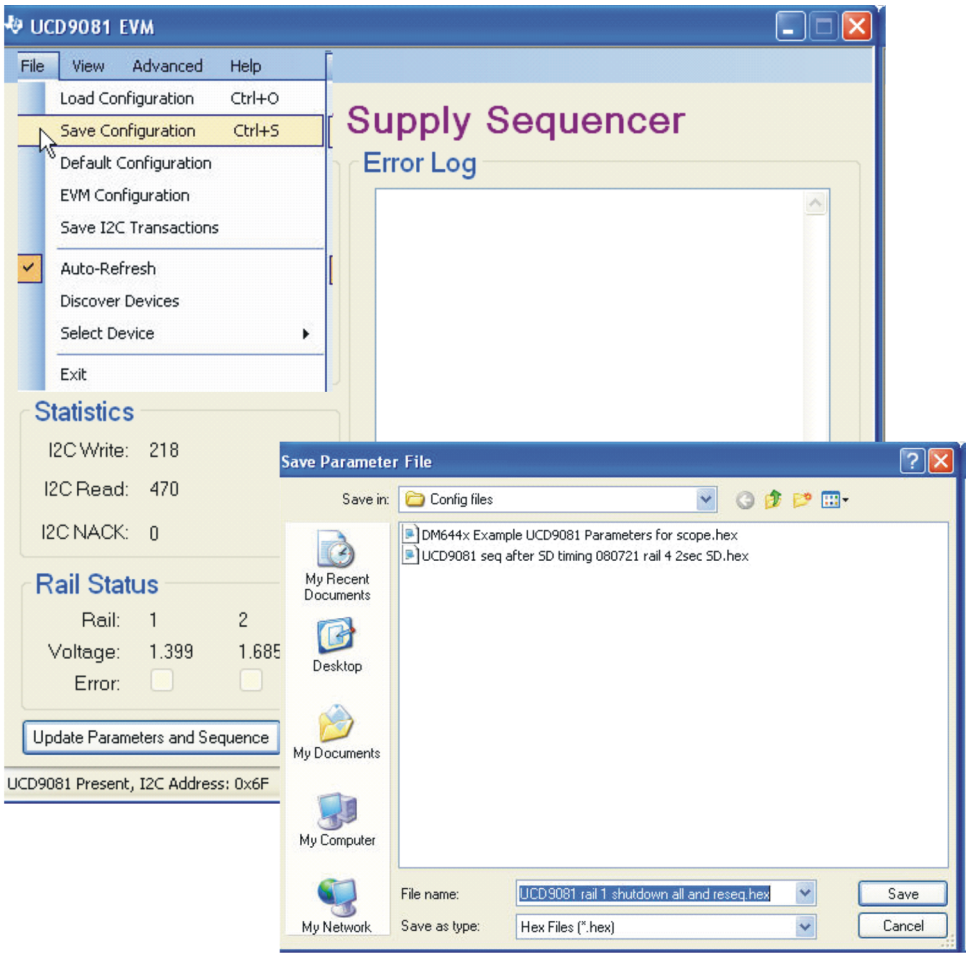


Figure 4. Save UCD9081 Parameters to Hexadecimal File

- **Default Configuration –** loads factory-provided parameters into the UCD9081. This is a null configuration that causes the device to do nothing at start-up.
- **EVM Configuration –** loads example parameters into the UCD9081 for use with EVM start-up and operation.
- **Save I2C Transactions –** generates an ASCII text file containing configuration-specific I^2C transactions.
- **Auto-Refresh –** refresh the window contents periodically. If not selected the window contents can be refreshed manually by clicking the Refresh button at the bottom of the main window. The Refresh button is unavailable when Auto-Refresh is selected.

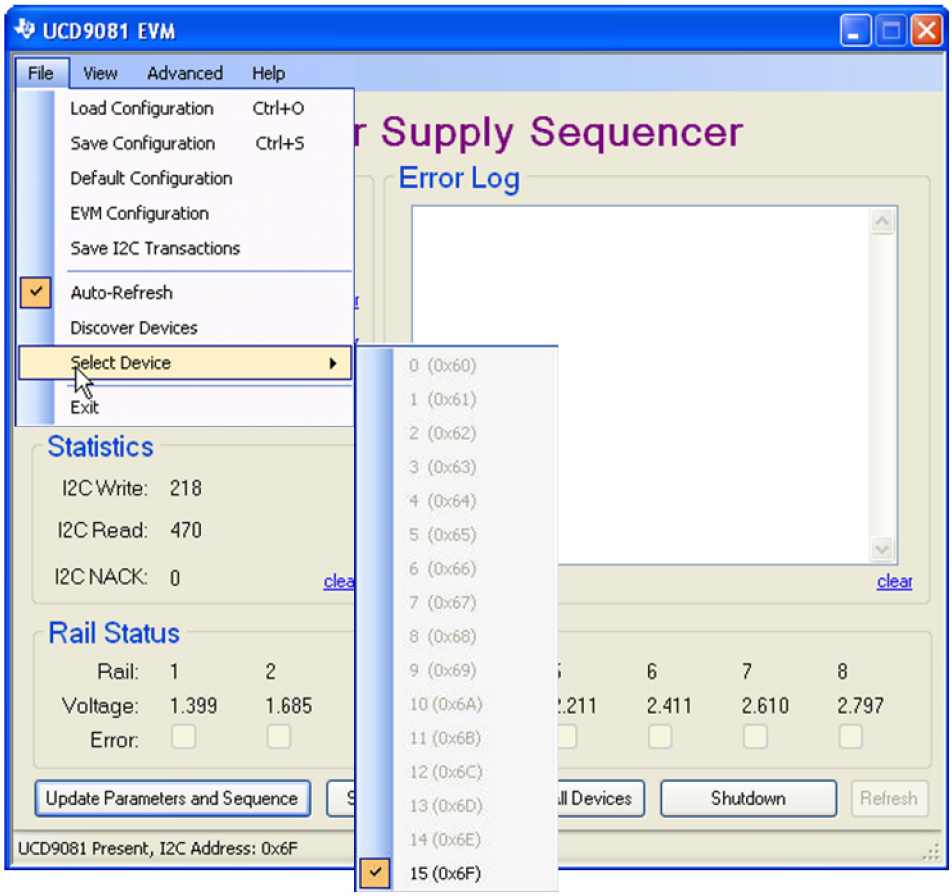


Figure 5. Select Device Option From File Menu Tab

- **Discover Devices –** discover all devices connected to the I^2C bus. The UCD9081 address is configurable by pulling inputs ADDR1, ADDR2, ADDR3, and ADDR4 (pins 25-28) high or low when power is applied to the device. The I^2C address is displayed at the bottom of the GUI main window.
- **Select Device –** if multiple devices are connected to the I^2C bus, this option allows the user to select which device is currently communicating with the GUI by selecting from a list of available addresses. Available devices are in **bold** and undetected addresses are grayed out.
- **Exit –** stop the GUI application.

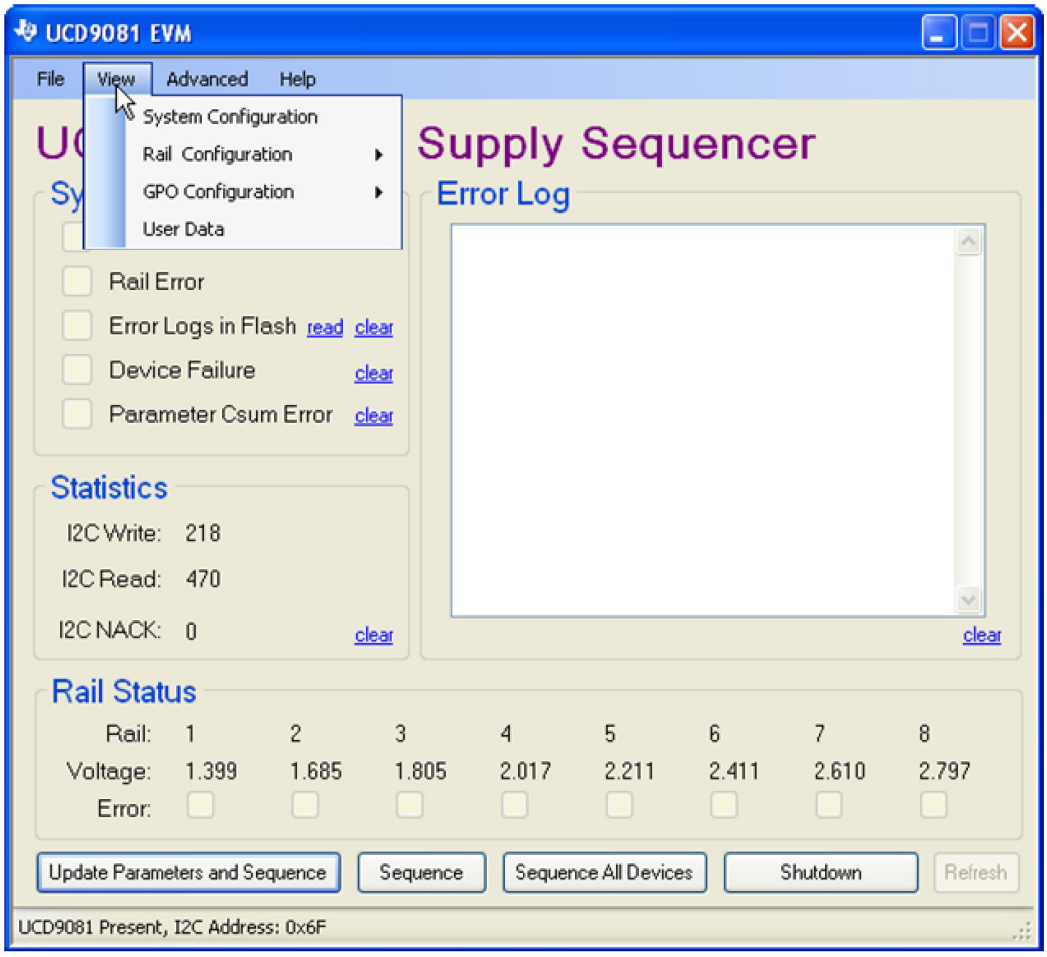


Figure 6. View Tab From Main Window Menu Bar

2.3 View Menu Options

The View menu shown in Figure 6 includes the following commands:

System Configuration:
The System Configuration window is shown in Figure 7 and includes the following configuration options:

- **Shutdown Delays –** user configuration of shutdown delays for each of the eight voltage rails and four GPOs. If a rail or GPO is marked for shutdown, then it does so according to the shutdown delays entered here. In the case of dependent rails shut down by parent rails, the delays are measured as the time between the event that marks a rail for shutdown and when the corresponding ENx pin is disabled. For example, if Rail 1 has Rail 2 specified as a dependency and Rail 1 is forced to shut down, the shutdown delay timer for Rail 2 starts when Rail 1 crosses its UV threshold (Rail 1 is considered off).

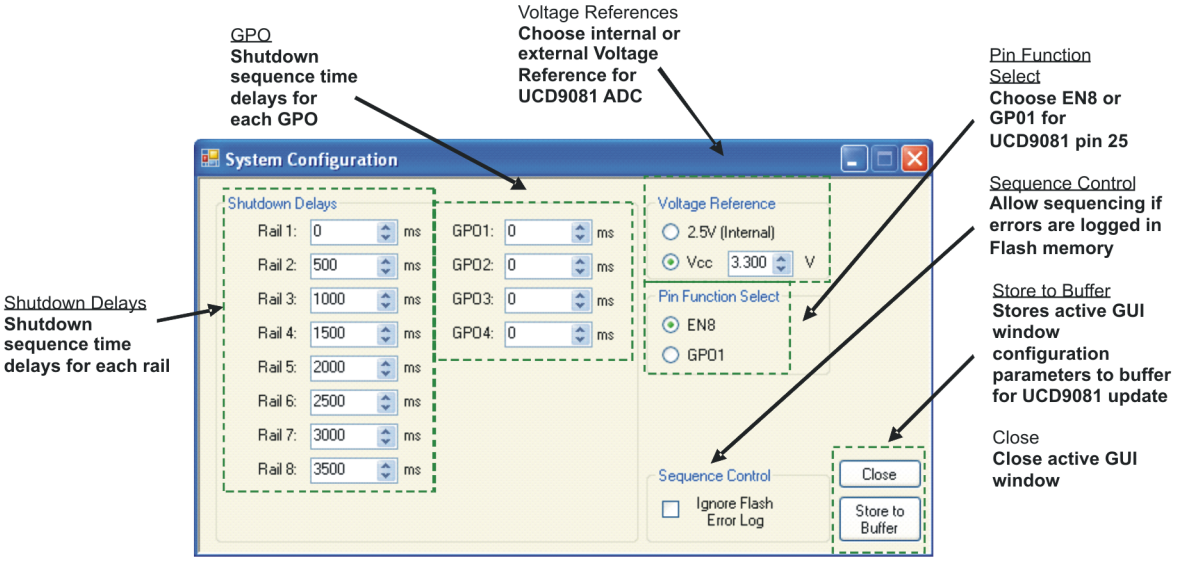


Figure 7. System Configuration Option From View Menu Tab

- **Voltage Reference –** user selection of internal 2.5V or external (V_{CC}) 3.3V Voltage Reference for the ADC. When V_{CC} is selected as the reference, the GUI provides an area for the actual V_{CC} voltage to be entered. For example, if the actual V_{CC} voltage measured at the device is 3.1 V, the GUI can use this to properly scale the displayed voltages.

NOTE: When the reference is changed and stored to the GUI buffer, the displayed rail voltages are incorrectly scaled, until the device parameters are updated using the Update Parameters and Sequence button in the GUI main window

- **Pin Function Select –** configures pin 25 as either EN8 or GPO1. The selected function disables configuration options for the other function.
- **Store to Buffer and Close buttons –** the Store to Buffer button saves the current window entries to a GUI buffer. The Update Parameters and Sequence button on the GUI main window can be used to resequence the EVM with the new configuration. The Close button closes the window. Any changes that are made without clicking the Store to Buffer button are not stored in the device when Update Parameters and Sequence is chosen in the main window and are lost when the System Configuration window is closed.
- **Sequence Control –** when this box is left unchecked, the UCD9081 stays in RESET after start-up if entries are detected in the Flash Error Log. If the box is checked, the device starts up whether or not entries are detected in the Flash Error Log.

Rail Configuration:
The Rail Configuration drop-down menu is shown in Figure 8. All Rails simultaneously opens all eight rail configuration windows for comparison setup. A single Rail Configuration window is shown in Figure 9 and includes the following configuration options:

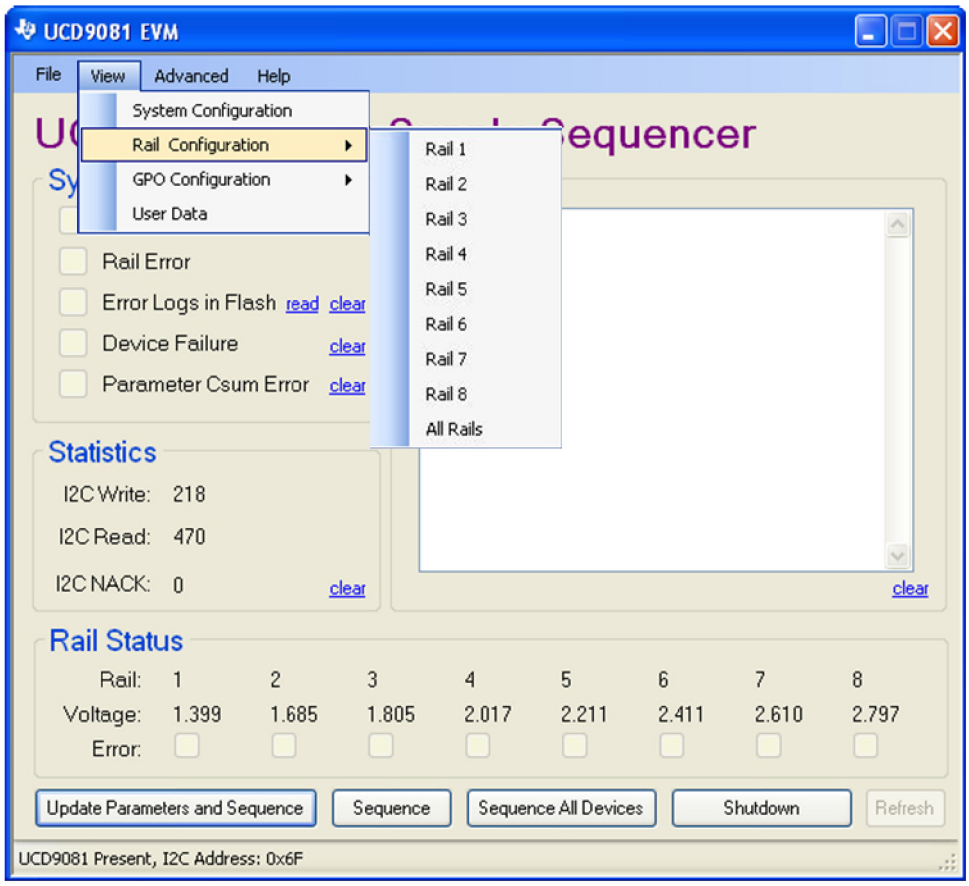


Figure 8. Rail Configuration Drop-Down From View Menu Tab

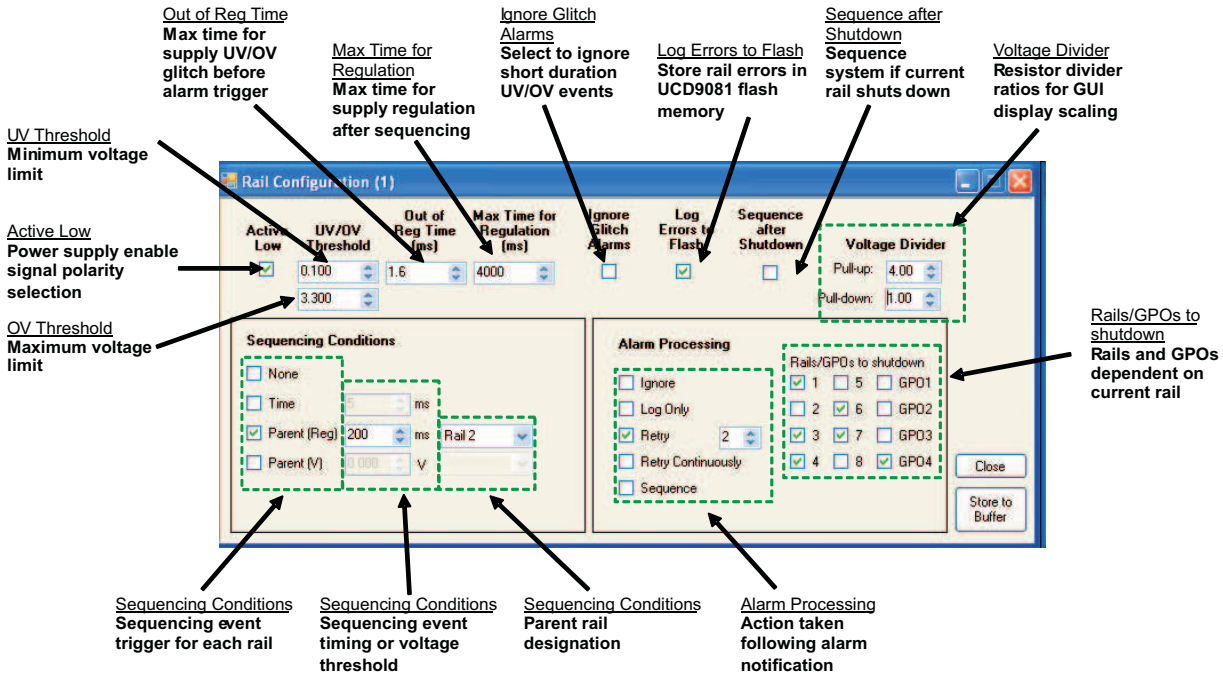


Figure 9. Rail Configuration Option From View Menu Tab

- **Sequencing Conditions Selections –** Voltage rail sequencing conditions are:
  - **None –** rail is not sequenced.
  - **Time –** time in milliseconds following a Start-up Sequence event before rail is enabled.
  - **Parent (Reg) –** time in milliseconds to delay after the parent rail achieves regulation before enabling the current rail.
  - **Parent (V) –** voltage the parent rail must reach before the current rail is enabled.
- **Alarm Actions –** The alarm actions are:
  - **Ignore –** take no action and do not log error.
  - **Log Only –** log any failures on this rail but take no other action, and keep rail enabled.
  - **Retry n Times –** continue to retry this rail for a configurable number of times (n = 0,1,2,3,4), then shut down according to the configured Rail and GPO Dependencies and the Shutdown Delays. If **Retry** is selected and the UCD9081 detects a fault, the following procedure takes place (Figure 10 and Figure 11):
    1. If n = 0, skip 2-5 and go to step 6.
    2. The faulty rail is disabled (~5 ms).
    3. The faulty rail is re-enabled.
    4. The rail remains enabled for the specified MTFR. If the rail properly achieves regulation, the rail remains enabled, and no further action is taken.
    5. If the rail does not properly achieve regulation, steps 2-4 are repeated (n–1) more times.
    6. If the error condition still exists after n retries, all rails and GPOs marked as dependents are sequenced off according to the delay times specified by the current system shutdown configuration.

  If any of the dependent rails have other rails or GPOs marked as dependents, those dependent rails or GPOs are also forced to shut down. Use **Retry 0 Times** and the appropriate dependencies to configure the UCD9081 to initiate a shutdown sequence in response to a rail error.

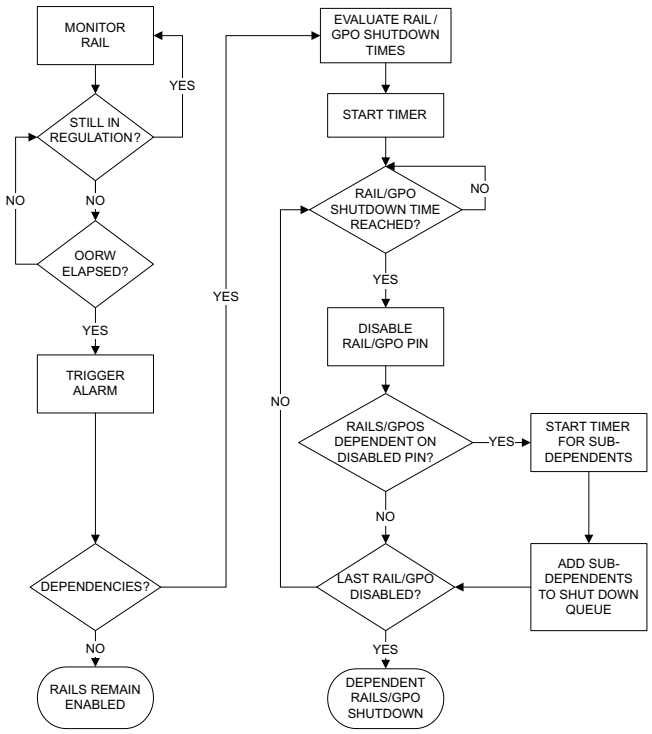


Figure 10. Flowchart for Retry 0 Times

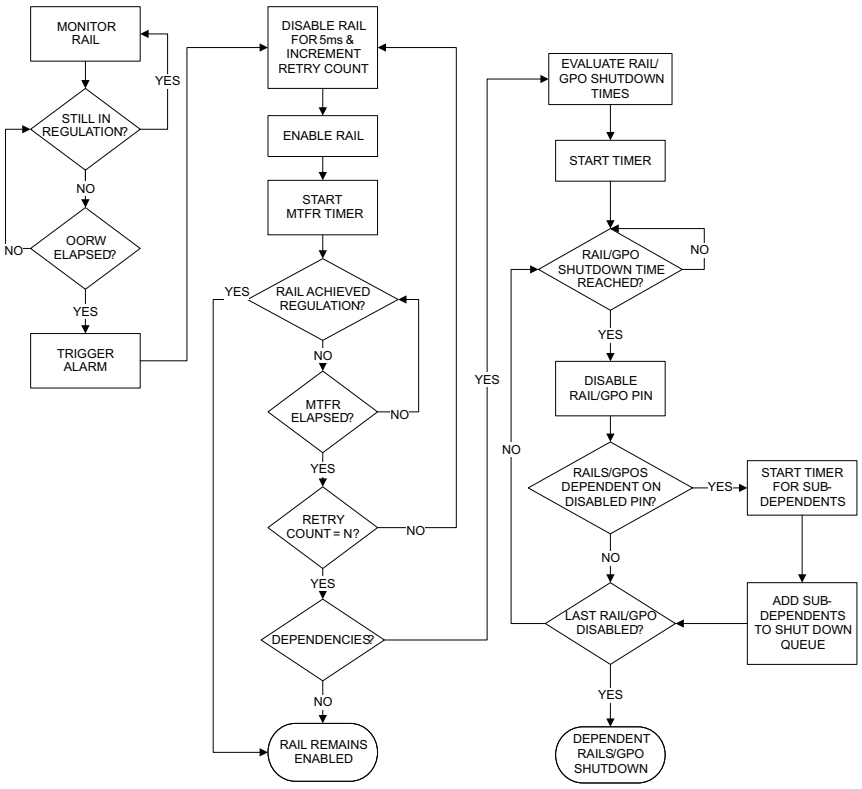


Figure 11. Flowchart for Retry n Times

- **Alarm Actions (continued)**
  - **Retry Continuously –** continue to retry this rail by disabling the rail (with ENx pin) and then re-enabling the rail. Repeat until the power supply rail alarm clears (Figure 12).
  - **Sequence –** shut down all rails and GPOs immediately (ignore shutdown time delays), and then sequence-on the system according to the current start-up sequence configuration.

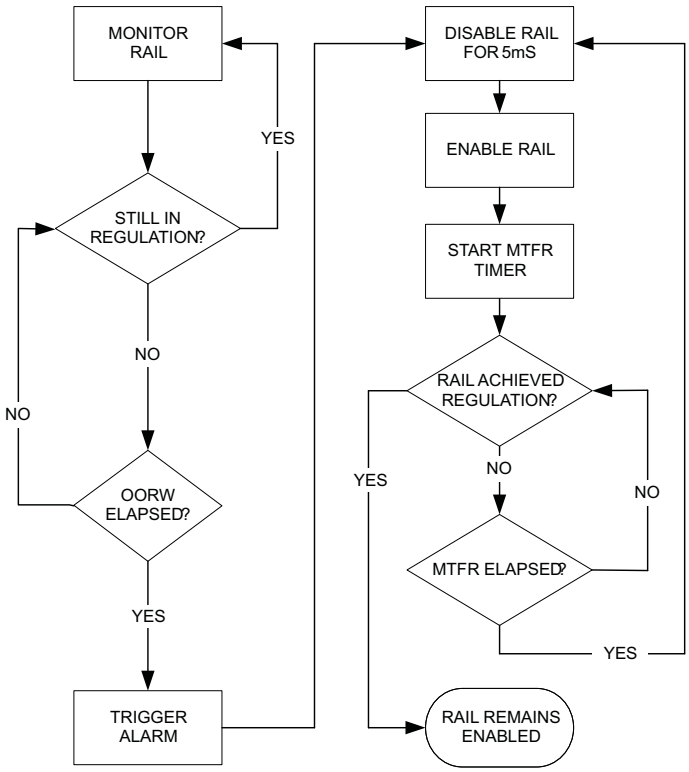


Figure 12. Flowchart for Retry Continuously

- **Rail and GPO Dependencies –** rails and GPOs can be marked as dependent on each other. This affects which rails and GPOs are shut down according to an alarm response. Delays specified in the system shutdown configuration and described in the preceding options are measured as the time between the event that marks a rail for shutdown and when the corresponding ENx pin is disabled. For example, if Rail 1 has Rail 2 specified as a dependency and Rail 1 is forced to shut down, the shutdown delay timer for Rail 2 starts when Rail 1 crosses its UV threshold (Rail 1 is considered off).

  If a voltage rail is disabled through a dependency on a parent rail, Alarm Processing options for the dependent rail including **Ignore**, **Log Only**, **Restart n Times**, **Restart Continuously**, and **Sequence** are not carried out. Because logging conventions are still followed, if **Ignore** is selected a shutdown caused by a parent rail is not recorded in the error log. **Sequence After Shutdown** is implemented if selected for a dependent rail that is disabled by a parent rail. **Sequence After Shutdown** is described in detail under the Rail Configuration section later in this document.
- **Active Low (Polarity) –** specify enable pin polarity.
- **UV/OV Threshold –** specify undervoltage and overvoltage trip points. Note that a UV value of zero causes the device to ignore any undervoltage conditions and that an OV value which is excessively high causes the device to ignore any overvoltage conditions.
- **Out of Reg Time (ms) –** specify the maximum amount of time (or glitch width) that the rail can be outside of the UV/OV range before an alarm is declared.
- **Max Time for Regulation (ms) –** specify the maximum amount of time a rail is allowed to achieve regulation (rail voltage must be within the UV/OV range) before an alarm is declared.
- **Ignore Glitch Alarms –** user can choose to not log glitches on a monitored rail
- **Log Errors to Flash –** log rail errors to nonvolatile memory for later evaluation.

- **Sequence after Shutdown–**specify UCD9081 ENx outputs to re-sequence the system as defined by the current sequencer configuration if the current rail is shut down. Sequence after Shutdown is an option that can be used with Retry n Times. **If this option is used with Retry n = 0, the following procedure takes place:**
  1. All rails and GPOs marked as dependents of the faulty rail are sequenced off according to the time delays specified in the system shutdown configuration.
  2. The GUI calculates the worst-case ENx or GPOx shutdown delay based on dependencies and delay timing.
  3. The UCD9081 waits until the time delay calculated by the GUI is satisfied.
  4. All remaining rails and GPOs are then shut down at the same time.
  5. UCD9081 RESET occurs according to the current start-up sequence configuration.

  If this option is used with Retry n =1,2,3,4, the following procedure takes place:

  1. The faulty rail is disabled for approximately 5 ms.
  2. The faulty rail is re-enabled.
  3. The rail remains enabled for the specified MTFR. If the rail achieves regulation, it remains enabled, and the UCD9081 continues monitoring as normal. No further action is taken.
  4. If the rail does not achieve regulation, steps 1-3 are repeated (n - 1) more times.
  5. If the error condition still exists after n retries, all rails and GPOs marked as dependents of the faulty rail are sequenced off according to the time delays specified in the system shutdown configuration.
  6. The GUI calculates the worst-case ENx or GPOx shutdown delay based on dependencies and delay timing.
  7. The UCD9081 waits until the time delay calculated by the GUI is satisfied.
  8. All remaining rails and GPOs are then shut down at the same time.
  9. UCD9081 RESET occurs according to the current start-up sequence configuration.

  Note that if a rail is specified to sequence after shutdown and is also marked as a dependent in the shutdown options of another rail, a fault on the parent rail could cause a sequence of the entire system. For example, if Rail 1 is configured to sequence after shutdown, and Rail 2 has Rail 1 selected as a dependent, then if Rail 2 is shut down, Rail 1 shuts down and the system follows the appropriate sequence after shutdown procedure.
- **Voltage Divider –** specify the external voltage divider resistor values that have been used in the design to attenuate the maximum voltage of a high voltage rail to V_{ref} (2.5 V or 3.3 V) at the MONx pin. The GUI uses these values to properly scale and display the voltages received through the UCD9081 monitors. If no external resistor divider is used, enter zero ohms for both resistor values to cause the divider ratio to be evaluated as unity (no scaling).

GPO Configuration:

The GUI GPO drop-down menu is shown in Figure 13. **All GPOs** simultaneously opens all GPO configuration forms for comparison setup. A single GPO Configuration window is shown in Figure 14 and includes the following configuration options:

- **Active Low –** specifies GPO pin polarity
- **Sequence after Shutdown –** UCD9081 GPOs can be marked to re-sequence the system as defined by the current sequencer configuration if the GPO is specified as dependent on a rail that shuts down.
- **Sequencing Conditions Selections –** GPO sequencing conditions are:
  - **None –** GPO is unsequenced.
  - **Time –** time in milliseconds following a Sequence event before GPO is enabled.
  - **Parent (Reg) –** time in milliseconds to delay after the parent rail achieves regulation before enabling this GPO.
- **User Data –** user can enter data to be uploaded to the device, such as customer-specific identification.

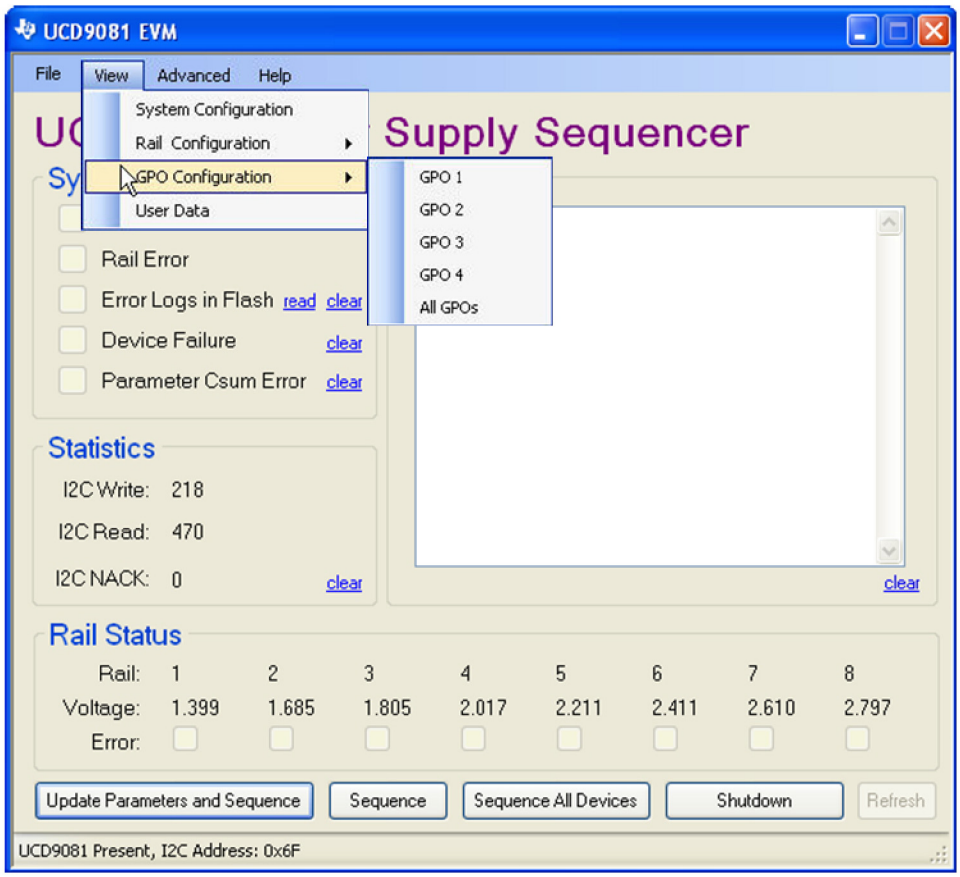


Figure 13. GPO Configuration Drop-down From View Menu Tab

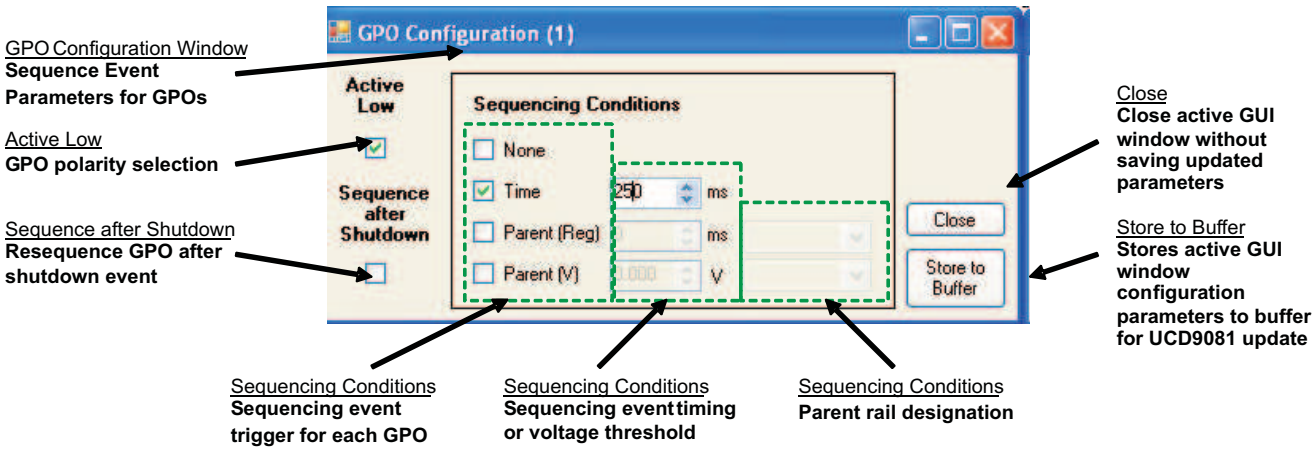


Figure 14. GPO Configuration Option From View Menu Tab

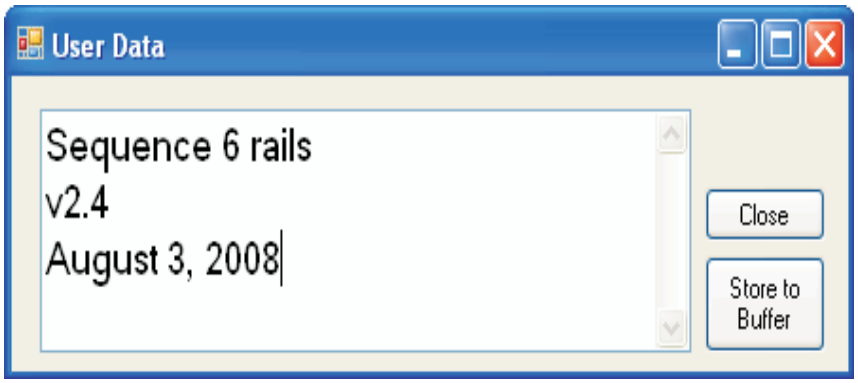
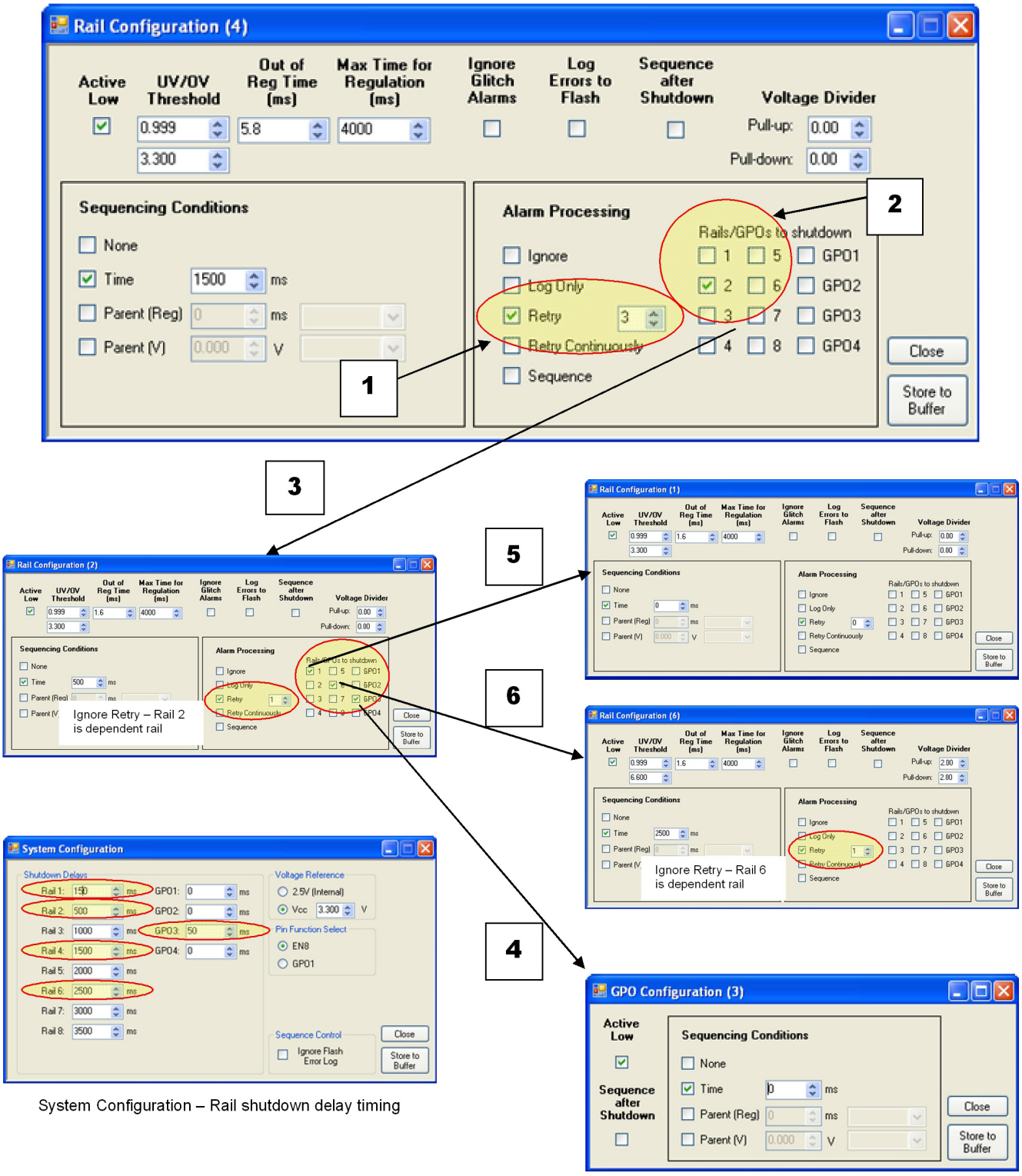


Figure 15. Store User Data to the UCD9081

3 Dependent Rails and GPOs, Error Logging, and Cascading Multiple Devices

3.1 Dependent Rails and GPOs

Alarm Processing options (**Ignore, Log Only, Restart n Times, Restart Continuously**) are not carried out for a dependent rail if that rail is disabled through a dependency on a parent rail. Because logging conventions are still followed, if **Ignore** is selected, a shutdown caused by a parent rail is not recorded in the error log. **Sequence After Shutdown** is implemented if selected for a dependent rail that is disabled by a parent rail. **Sequence After Shutdown** is described in detail under the Rail Configuration section later in this document.



System Configuration – Rail shutdown delay timing

Figure 16. Example of Dependent Rail Configuration and Processing

Although Alarm Processing options are ignored when a dependent rail is disabled by a parent rail, other rails or GPOs selected to shut down by the dependent rail are disabled. Figure 16 shows an example with Rail 2 as a dependent of Rail 4. In this configuration, if Rail 4 experiences a sustained UV or OV condition longer than 5.8 ms (**Out of Reg Time**), then Rail 4 retries three times as described in the **Retry n Times** section. If Rail 4 does not achieve regulation after the third try, then Rail 2 is shut down according to the time delay in the System Configuration window. According to the Rail 2 Alarm Processing configuration, it retries one time if an error is on the rail. However, because Rail 2 is shut down due to its dependency on Rail 4 and not because of an error on Rail 2 itself, it does not retry at all. Rail 2 is configured to shut down Rail 1, Rail 6, and GPO3, and those outputs are disabled on the shutdown of Rail 2. Rail 1, Rail 6, and GPO3 are not configured to shut down other rails so the cascaded shutdown stops at this point.

To summarize, if Rail 4 registers a sustained error:

1. Rail 4 tries to restart three times.
2. If Rail 4 does not achieve regulation after the third try, Rail 2 shuts down 500 ms after Rail 4 shuts down.
3. Rail 2 does not try to restart.
4. GPO3 shuts down 50 ms after Rail 2 shuts down.
5. Rail 1 shuts down 150 ms after Rail 2 shuts down.
6. Rail 6 shuts down 2500 ms after Rail 2 shuts down.

If a voltage rail is configured to **Retry n Times** with dependent rails that are disabled if regulation is not achieved, and the Alarm Processing options for that rail are changed, the previous dependencies remain checked but grayed out. If the voltage rail with the grayed-out checked dependencies is forced to shut down by a parent rail, then the dependent rails are also shut down. For example, in Figure 17, if Rail 5 is disabled by a parent rail, then Rail 4, Rail 7, and GPO2 are also disabled. If the user does not want such cascaded dependencies to take effect, then the grayed-out dependencies can be cleared by doing the following:

1. Select **Retry.**
2. Uncheck the boxes.
3. Re-select the required alarm processing option.
4. Click the **Store to Buffer** button.

Select **Update Parameters and Sequence** at the GUI main window.

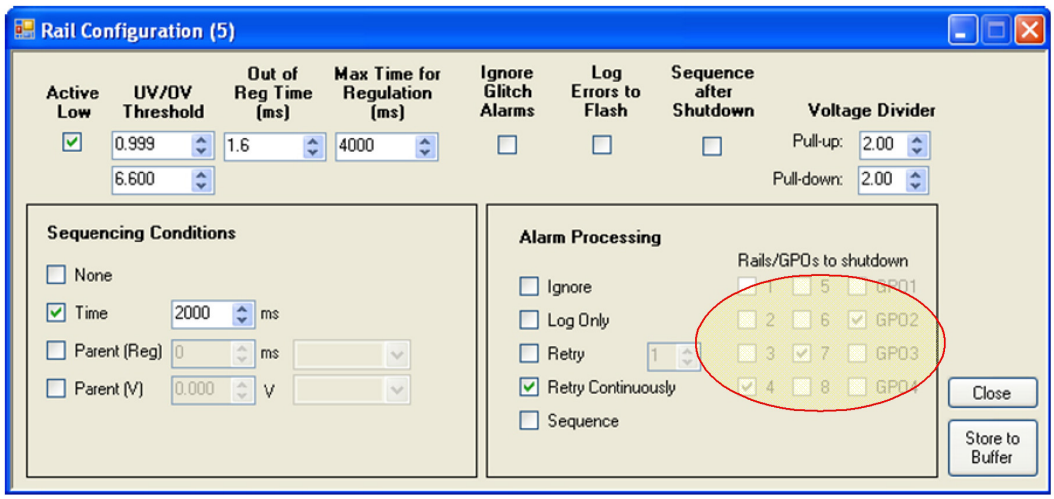


Figure 17. Grayed Out Dependent Rails

3.2 Using Multiple UCD9081 ICs

For applications that require sequencing of more than eight voltage rails, multiple UCD9081 ICs can be used, either independently but connected to a single I^2C bus or by cascading devices. To use multiple, independently configured UCD9081 ICs in a design, each device is given a unique I^2C address. The UCD9081 supports 16 addresses (0x60h - 0x6Fh). The GUI can find up to 16 devices on a single I^2C bus and can be used to communicate independently with each device. Interdependencies between voltage rails controlled by separate devices can be implemented in a number of ways.

UCD9081 ICs can be cascaded by using an ENx pin as either the RESET line or as a voltage rail input for the next device. Figure 18 shows one example of how multiple UCD9081 ICs can be cascaded. GP02 of the master device is configured to assert based on the status of one of the eight rails monitored by the master device. Assertion of GP02 brings MON8 of the slave device into regulation. The slave device is configured so that when MON8 is in regulation, the remaining rails sequence according to the user-specified configuration. When the master GP02 is disabled, the slave device shuts down, again as specified by the user.

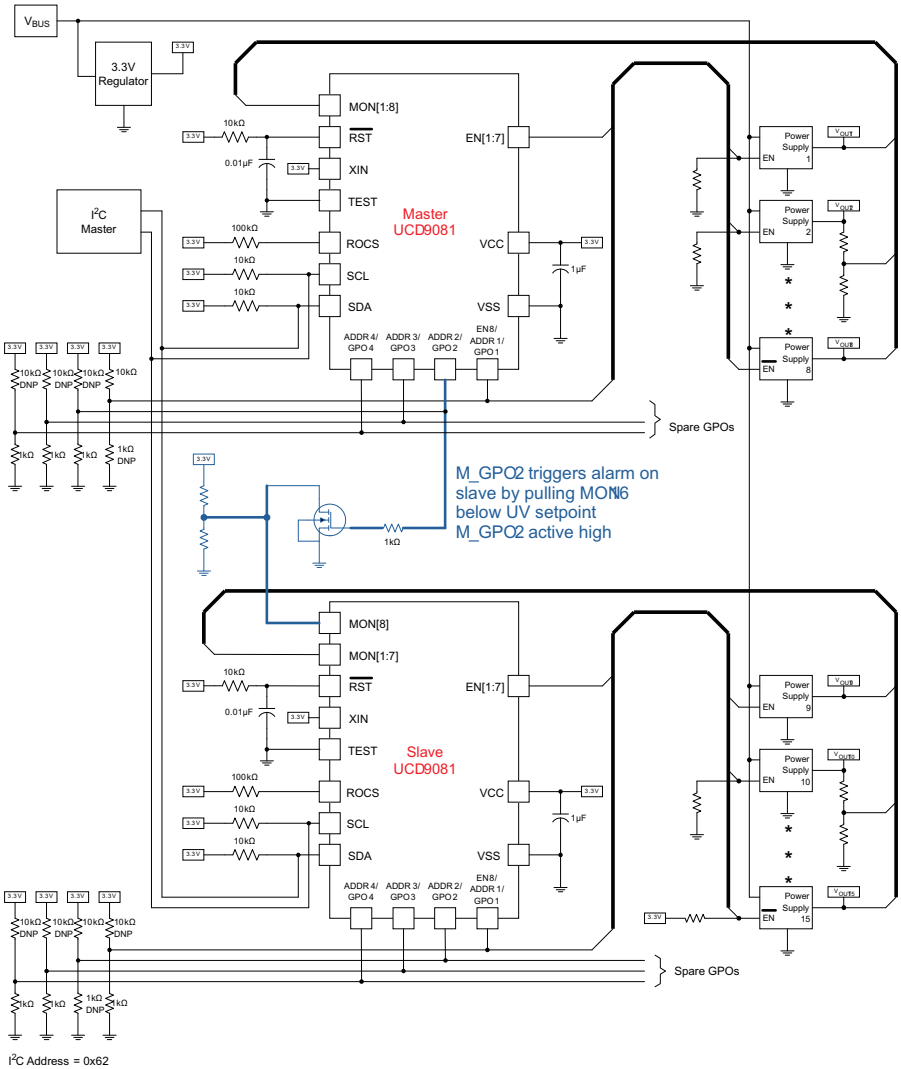


Figure 18. Option for Cascading Multiple UCD9081 ICs

3.3 Error Logging

In addition to taking action in response to errors on specified rails, the UCD9081 can log errors in two

ways. Unless a rail is configured to **Ignore** faults, all faults are stored in on-chip memory and can be read by an I²C master device, including the UCD9081 GUI (Figure 19), over the I²C bus. The user can choose to ignore Glitch Alarms or to log them for any rail. The error log includes a time stamp showing elapsed time since the UCD9081 was last reset, the rail number, the type of error, and the voltage measured on the rail at the time of the error.

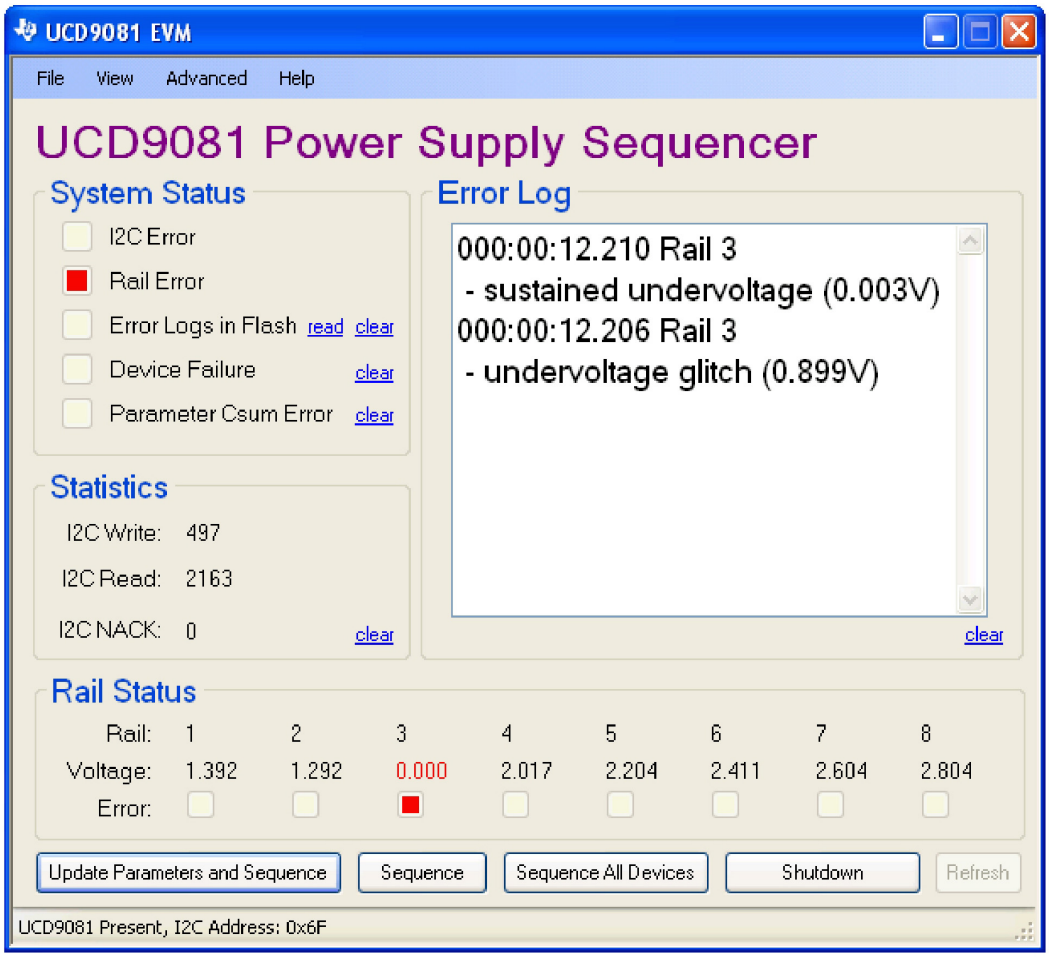


Figure 19. Error Log

The UCD9081 recognizes and can log five different types of rail errors. Glitches can only be logged and cannot initiate additional Alarm Processing.

1. **undervoltage glitch –** monitored rail voltage drops below the UV threshold and returns to regulation before the Out of Reg Time limit is reached.
2. **overvoltage glitch –** monitored rail voltage increases above the OV threshold and returns to regulation before the Out of Reg Time limit is reached.
3. **sustained undervoltage –** monitored rail voltage drops below the UV threshold and stays for longer than Out of Reg Time limit.
4. **sustained overvoltage –** monitored rail voltage increases above the OV threshold and stays for longer than Out of Reg Time limit.
5. **failed to start –** voltage rail was enabled and failed to settle between the UV and OV thresholds within Max Time for Regulation

The **Log Errors to Flash** feature is a tool to help troubleshoot failure mechanisms. Errors on critical rails can be logged to flash memory for later review even if power is lost to the UCD9081, but only critical rails should be logged. While errors are being logged, system monitoring is disabled for the 1.5 ms it takes to write to flash. The first eight error entries are kept. Once the Flash Error Log is full, no new entries can be added until the log is cleared. If a rail is set to **Retry Continuously** and to **Log Errors to Flash**, the Flash Error Log can quickly fill up if that rail fails and then tries unsuccessfully to restart. Logging errors to flash requires 5 mA for 1.5 ms at a minimum V_{cc} of 3.0 V. To log critical rail errors to flash during a system shutdown, a large capacitor can be used on V_{cc} to hold the device on. To size the capacitor, the shutdown timing of the critical rails and the loading and energy storage on V_{cc} must be considered in addition to the UCD9081 current, timing, and minimum voltage requirements.

If error logs exist in flash memory, the UCD9081 can be configured to hold the device in RESET following a power cycle or reset event and not allow it to restart and sequence. While the device is in RESET, it checks for any nonzero values in the Flash Error Log. If nonzero values are found, the device stays in RESET until the user reads and clears the error log via I^2C. If a user wants failures on critical rails to be stored for troubleshooting purposes, then selecting this mode ensures that errors logged in flash memory are not overwritten until the flash memory is read.

Alternatively, the UCD9081 can be configured to sequence if entries are in the Flash Error Log by setting a check box in the System Configuration window (Figure 7). If entries are in the Flash Error Log, and the system is configured to allow sequencing, any new entries append to any existing entries. After a device reset or power cycle, the error log time stamp returns to 000:00:00.000. The time stamp for any errors appended to the Flash Error Log indicates the time elapsed since the last RESET. If the Flash Error Log is already full at RESET and is not cleared, then no new entries are appended to the log. Selecting the second mode does log errors but also allows a system to sequence and attempt to restart if errors are caused by a power glitch on the system input voltage or by some event other than a power supply failure that is monitored and controlled by the UCD9081.

Once the device is operating, the Flash Error Log can be cleared by a master I^2C device using the procedure outlined in the data sheet. The **clear** button next to **Error Logs in Flash** in the GUI Main Window also clears the Flash Error Log. Performing this action does not reset the device. The **read** button displays the Flash Error Log in the GUI Main Window Error Log. Flash errors are shown in red text and on-chip memory errors are in black.

4 Example Sequencing Design

Figure 20 shows the basic pieces required to configure the UCD9081 via I^2C using a Windows-based GUI. The GUI can configure all available options such as sequencing and shutdown order, over/undervoltage limits and timing, logging of rail errors to flash memory, and other configurable features of the UCD9081. Once the configuration for the device is set to the user's requirements, the GUI can convert the *.par GUI file into a *.hex file. The UCD9081 can be configured by a host processor or with a third-party device programmer using the *.hex file. As previously mentioned, the GUI can monitor the operation of the sequencer by reporting current readings of voltage and error conditions on all the rails.

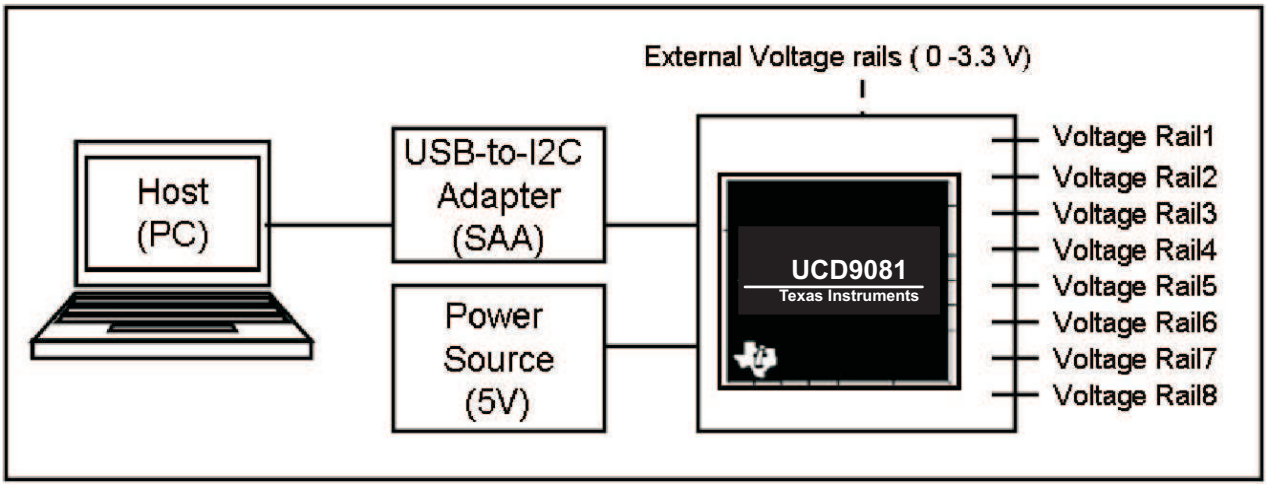


Figure 20. Using the GUI to Communicate With the UCD9081 in a User's Application

Once the dependencies and sequencing and shutdown timings for each of the system voltage rails and GPOs have been established by the designer, the voltage rails and GPOs can be mapped to match the UCD9081 GUI naming convention as shown in Table 1.

Table 1. Map User-Defined Voltage Rails to GUI Rail Naming Convention

User Designation	UCD9081 GUI	Sequence-On Parameters	Sequence-Off Parameters	Active H or L	Dependent Outputs	Logging
3.3V_MAIN	Rail 1	First rail started – start at 0 ms	Last rail shutdown (180 ms)	L	All active voltage rails. All active GPOs	Ignore Glitch Alarms Log errors to FLASH
1V	Rail 2	Start 50 ms after 1.8V (Rail 3) reaches regulation	First rail shutdown (10 ms)	H	None	Log errors to FLASH
1.8V	Rail 3	Start 10 ms after 2.5V (Rail 4) reaches regulation	Second rail shutdown (20 ms)	H	None	None
2.5V	Rail 4	Start 10 ms after 3.3V_MAIN (Rail 1) reaches regulation	Fourth rail shutdown (150 ms)	L	Rail 2, 3, 4, 5, GPO2	Log errors to FLASH
2.5V_I/O	Rail 5	Start 100 ms after 2.5V (Rail 4) reaches regulation	Third rail shutdown (120 ms)	H	None	None
Not used	Rail 6					
Not used	Rail 7					
3.3V_9081 (V_{CC})	Rail 8	Monitor only	Monitor only		None	Log errors to FLASH
LED_SEQ_DONE_1	GPO2	Start after last rail reaches regulation (2.5V_I/O, Rail 5)	Shut down first	H	None	None
Not used	GPO3					
Not used	GPO4					

To establish start-up dependencies and timing, start from the GUI main window menu bar and select **View → Rail Configuration → All Rails** (Figure 21). Configuration is done using the GUI naming convention. Therefore, keeping track of how the system rails and outputs correspond to the GUI rails and outputs helps reduce confusion. For this sequencing example, Table 1 also lists the Rail and GPO dependencies.

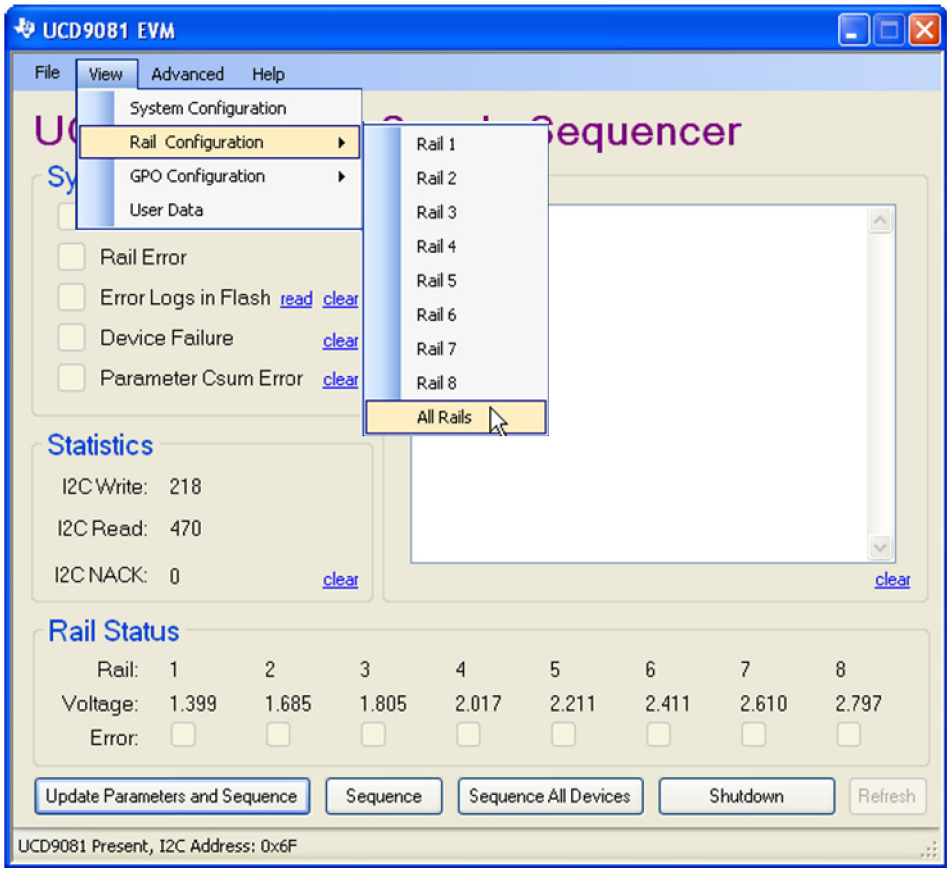


Figure 21. Select All Rails From Rail Configuration Drop-Down Menu

Choose **Rail Configuration (8)**, and make the following selections (Figure 22). Then repeat for each rail used in the design based on the required system operation.

Configure Rail 8 (3.3V_9081):

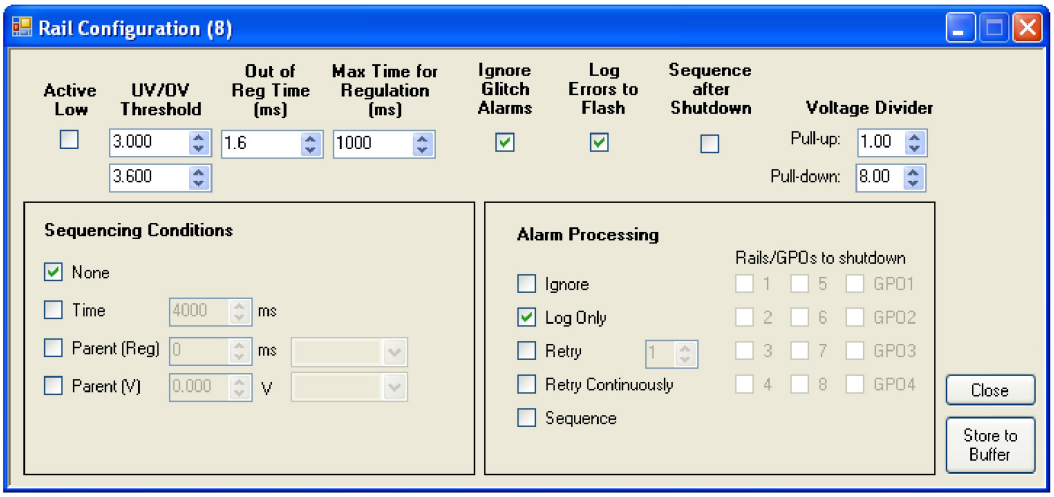


Figure 22. Example – Configure Rail 8

Rail Configuration (8) – Monitor UCD9081 Supply Voltage (3.3V_9081)	
Set EN8 High – not connected	**Active Low –** Unchecked
Voltage Regulation between 3.000 V and 3.600 V	**UV threshold –** 3.000 **OV threshold –** 3.600
Maximum Glitch width = 1.6 ms	**Out of Reg Time (ms) –** 1.6
Supply must be within regulation 1 second after enable	**Max Time for Regulation (ms) –** 1000
Power supply glitches are not logged to SRAM or FLASH	**Ignore Glitch Alarms –** Checked
Out of regulation errors are logged to FLASH	**Log Errors to Flash –** Checked
Do not resequence the system after a commanded shutdown of Rail 8	**Sequence after Shutdown –** Unchecked
Divide rail voltage so that Rail 8 max (3.6 V) = 3.2 V at ADC	**Voltage Divider Pullup –** 1.00 **Voltage Divider Pulldown –** 8.00
Monitor Rail 8 only – do not sequence	**Sequencing Conditions –** None
If Rail 8 voltage falls out of regulation log error to FLASH	**Alarm Processing –** Log Only
If Rail 8 is shut down, do not shut down any other rails or GPOs	**Rails/GPOs to shut down –** Check no boxes

Configure Rail 1 (3.3V_MAIN):

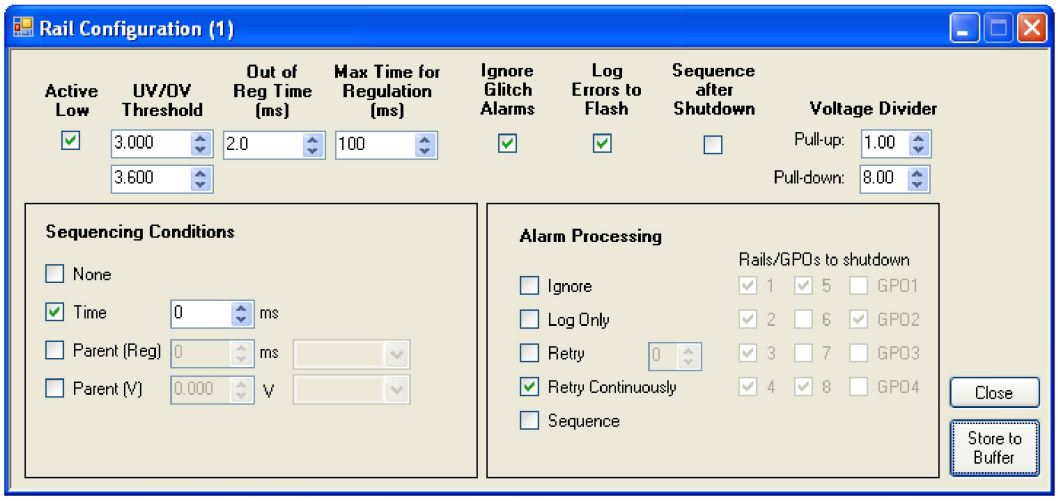


Figure 23. Example – Configure Rail 1

Rail Configuration (1) – Monitor and Sequence Input to All Other Supplies (3.3V_MAIN)	
EN1 Low turns on 3.3-V Power Supply to rest of system	**Active Low –** Checked
Voltage Regulation between 3.000 V and 3.600 V	**UV threshold –** 3.000 **OV threshold –** 3.600
Maximum Glitch width = 2 ms	**Out of Reg Time (ms) –** 2.0
Supply must be within regulation 100 ms after enable	**Max Time for Regulation (ms) –** 100
Power supply glitches are not logged to SRAM or FLASH	**Ignore Glitch Alarms –** Checked
Out of Regulation errors are logged to FLASH	**Log Errors to Flash –** Checked
Do not resequence the system after a commanded shutdown of Rail 1	**Sequence after Shutdown –** Unchecked
Divide rail voltage so that Rail 1 max (3.6 V) = 3.2 V at ADC	**Voltage Divider Pullup –** 1.00 **Voltage Divider Pulldown –** 8.00
Enable rail immediately by setting EN1 low	**Sequencing Conditions –** Time 0 ms
If Rail 1 voltage falls out of regulation disable EN1 and then Retry until regulation is achieved or system is turned off	**Alarm Processing –** Retry Continuously
If Rail 1 is shut down by a parent rail, also turn off Enables for all other active rails and GPO2	**Rails/GPOs to shut down –** Check Rails 1, 2, 3, 4, 5, 8, GPO2

Configure Rail 2 (1V):

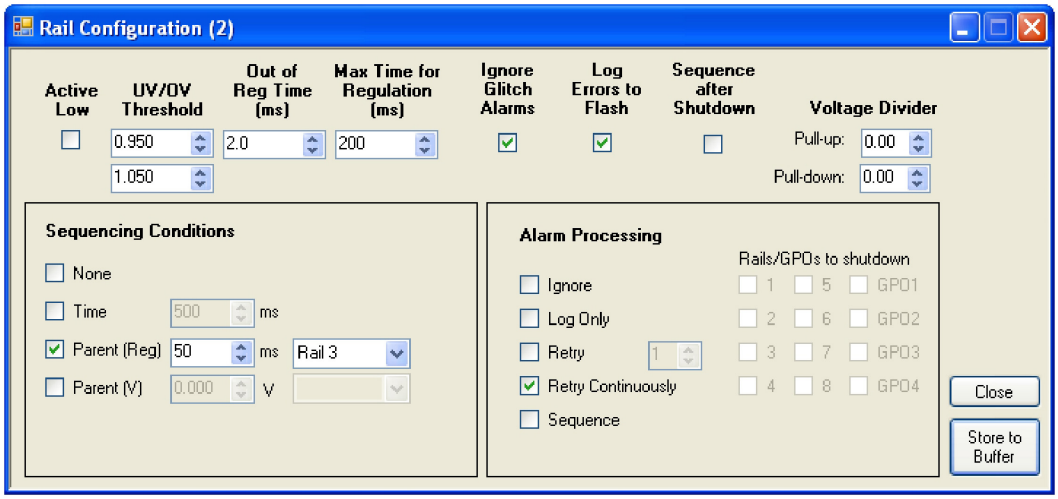


Figure 24. Example – Configure Rail 2

Rail Configuration (2) – Monitor and Sequence 1V Supply	
EN2 High turns on 1-V power supply	**Active Low –** Unchecked
Voltage Regulation between 0.950 V and 1.050 V	**UV threshold –** 0.950 **OV threshold –** 1.050
Maximum Glitch width = 2 ms	**Out of Reg Time (ms) –** 2.0
Supply must be within Regulation 200 ms after enable	**Max Time for Regulation (ms) –** 200
Power supply glitches are not logged to SRAM or FLASH	**Ignore Glitch Alarms –** Checked
Out of Regulation errors are logged to FLASH	**Log Errors to Flash –** Checked
Do not resequence the system after a commanded shutdown of Rail 2	**Sequence after Shutdown –** Unchecked
Measure rail voltage directly with ADC	**Voltage Divider Pullup –** 0.00 **Voltage Divider Pulldown –** 0.00
Enable rail 50 ms after Rail 3 achieves regulation by setting EN2 high	**Sequencing Conditions –** Parent (Reg) 50 ms, Rail 3
If Rail 2 voltage falls out of regulation, disable EN2 and then retry until regulation is achieved or system is turned off	**Alarm Processing –** Retry Continuously
If Rail 2 is shut down, do not shut down any other rails or GPOs	**Rails/GPOs to shut down –** Check no boxes

Configure Rail 3 (1.8V):

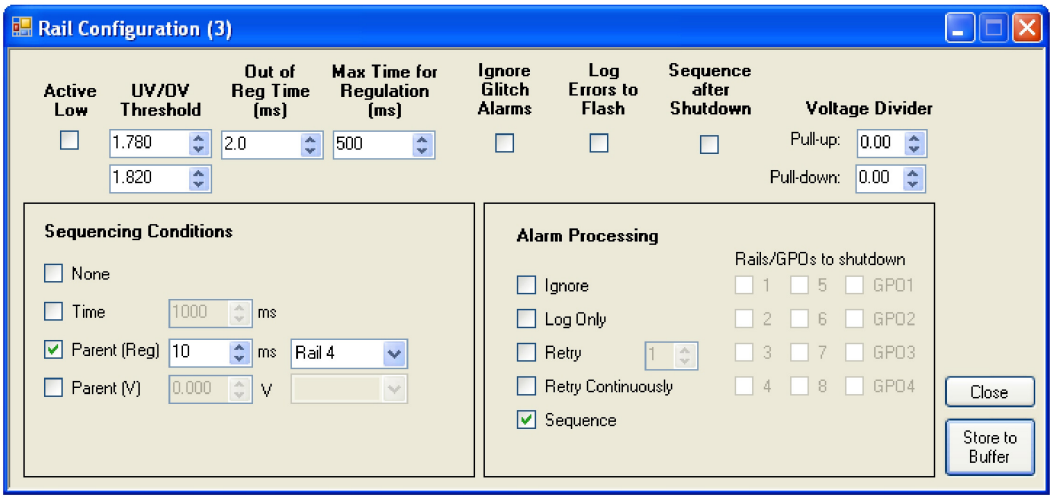


Figure 25. Example – Configure Rail 3

Rail Configuration (3) – Monitor and Sequence 1.8V Supply	
EN3 High turns on 1.8-V power supply	**Active Low –** Unchecked
Voltage Regulation between 1.780 V and 1.820 V	**UV threshold –** 1.780 **OV threshold –** 1.820
Maximum Glitch width = 2 ms	**Out of Reg Time (ms) –** 2.0
Supply must be within regulation 500 ms after enable	**Max Time for Regulation (ms) –** 500
Power supply glitches are logged to SRAM	**Ignore Glitch Alarms –** Unchecked
Out of regulation errors are not logged to FLASH	**Log Errors to Flash –** Unchecked
Do not resequence the system after a commanded shutdown of Rail 3	**Sequence after Shutdown –** Unchecked
Measure rail voltage directly with ADC	**Voltage Divider Pull-up –** 0.00 **Voltage Divider Pull-down –** 0.00
Enable rail 10msec after Rail 4 achieves regulation by setting EN3 high	**Sequencing Conditions –** Parent (Reg) 10ms, Rail 4
If Rail 3 voltage falls out of regulation then RESET device – immediately disable all outputs and then sequence rails based on configured parameters	**Alarm Processing –** Sequence
If Rail 3 is shut down, do not shut down any other Rails or GPOs	**Rails/GPOs to shut down –** Check no boxes

Configure Rail 4 (2.5V):

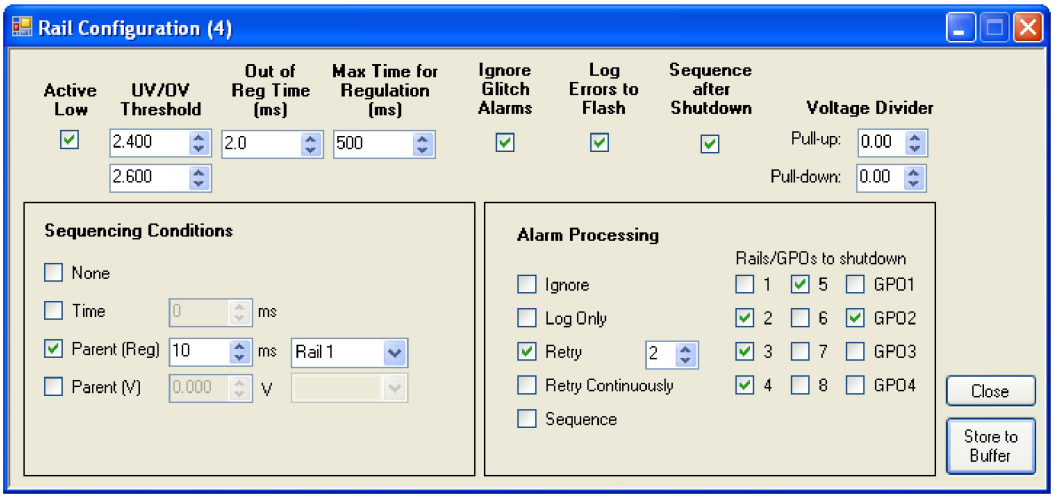


Figure 26. Example – Configure Rail 4

Rail Configuration (4) – Monitor and Sequence 2.5V Supply	
EN4 Low turns on 2.5-V power supply	**Active Low –** Checked
Voltage regulation between 2.400 V and 2.600 V	**UV threshold –** 2.400 **OV threshold –** 2.600
Maximum Glitch width = 2.0msec	**Out of Reg Time (ms) –** 2
Supply must be within Regulation 500 ms after enable	**Max Time for Regulation (ms) –** 500
Power supply glitches are not logged to SRAM or FLASH	**Ignore Glitch Alarms –** Checked
Out of regulation errors are logged to FLASH	**Log Errors to Flash –** Checked
Sequence the system after a commanded shutdown of Rail 4	**Sequence after Shutdown –** Checked
Measure rail voltage directly with ADC	**Voltage Divider Pullup –** 0.00 **Voltage Divider Pulldown –** 0.00
Enable rail 10 ms after Rail 1 achieves regulation by setting EN4 low	**Sequencing Conditions –** Parent (Reg) 10 ms, Rail 1
If Rail 4 voltage falls out of regulation, then attempt to restart Rail 4 two times using EN4 as described in **Retry n Times**	**Alarm Processing –** Retry 2
If Rail 4 is disabled by a parent rail or after 2 Retry attempts, turn off Enables for Rails 2, 3, 4, 5 and GPO2	**Rails/GPOs to shut down –** Check Rails 2, 3, 4, 5, GPO2

Configure Rail 5 (2.5V_I/O):

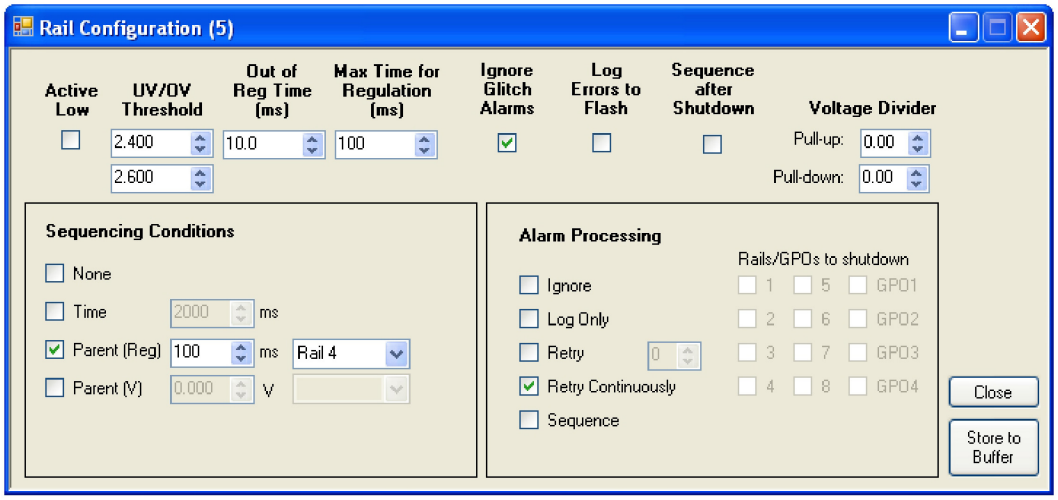


Figure 27. Example – Configure Rail 5

Rail Configuration (5) – Monitor and Sequence 2.5V_I/O Supply	
EN5 High turns on 2.5-V power supply	**Active Low –** Unchecked
Voltage regulation between 2.400 V and 2.600 V	**UV threshold –** 2.400 **OV threshold –** 2.600
Maximum Glitch width = 10 ms	**Out of Reg Time (ms) –** 10
Supply must be within regulation 100msec after enable	**Max Time for Regulation (ms) –** 100
Power supply glitches are not logged to SRAM or FLASH	**Ignore Glitch Alarms –** Checked
Out of regulation errors are not logged to FLASH	**Log Errors to Flash –** Unchecked
Do not sequence the system after a commanded shutdown of Rail 5	**Sequence after Shutdown –** Unchecked
Measure rail voltage directly with ADC	**Voltage Divider Pullup –** 0.00 **Voltage Divider Pulldown –** 0.00
Enable rail 100 ms after Rail 4 achieves regulation by setting EN5 high	**Sequencing Conditions –** Parent (Reg) 100 ms, Rail 4
If Rail 5 voltage falls out of regulation disable EN5 and then Retry until Regulation is achieved or system is turned off	**Alarm Processing –** Retry Continuously
If Rail 5 is shut down, do not shut down any other rails or GPOs	**Rails/GPOs to shut down –** Check no boxes

Configure GPO2 (LED_SEQ_DONE_1):

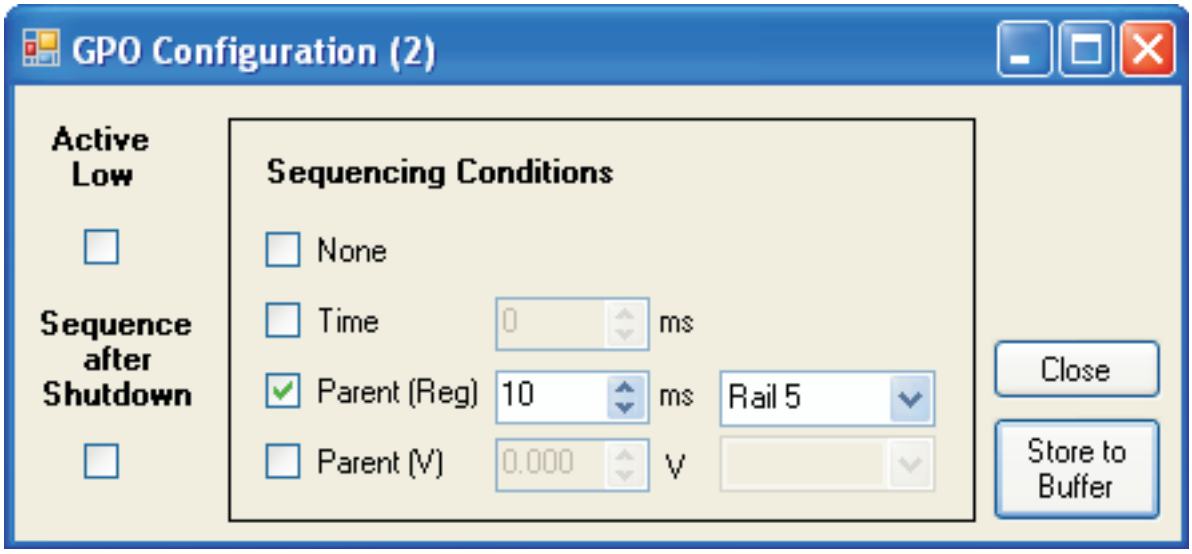


Figure 28. Example – Configure GPO2

GPO Configuration (2) – Sequence LED_SEQ_DONE_1	
GPO2 High turns on indicator LED	**Active Low –** Unchecked
Do not sequence the system after a commanded shutdown of GPO2	**Sequence after Shutdown –** Unchecked
Turn on LED 10 ms after Rail 5 achieves regulation by setting GPO2 high	**Sequencing Conditions –** Parent (Reg) 100 ms, Rail 5

Sequence-off timing for all rails and GPOs are set in a single window. From the GUI main window menu bar, select **View → System Configuration**. Figure 29 shows the settings for this example:

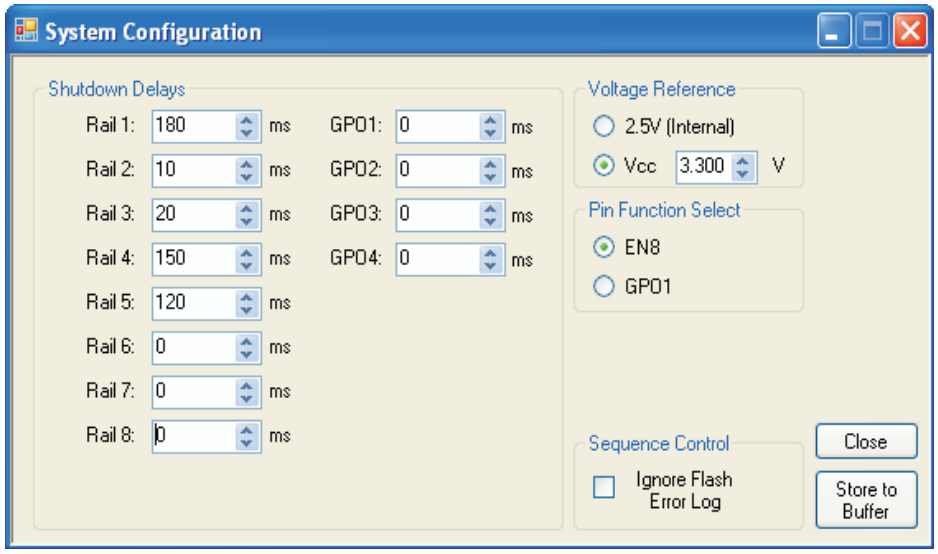


Figure 29. Example – Configure Shutdown Delays for All Rails

5 Enabling and Disabling Individual Rails and GPOs Over the I²C bus

The I²C bus can be used to toggle individual UCD9081 Enables and GPOs, a capability that allows a single rail or GPO to be turned off or on without a failure present or without sequencing the device. An ENx or GPO can be set to 0 or 1 over the I²C bus by writing to the 2-byte GPIOVAL register. Each byte of GPIOVAL is accessible. The address of the low byte (GPIOVALL) is 0x1Ah and the high byte (GPIOVALH) is at 0x1Bh (Table 2). By writing to the register, any individual or group of ENx or GPOx pins can be set. Table 3 maps the GPIOVAL register to the UCD9081 ENx and GPOx pin names. To toggle a single or group of rails or GPOs:

1. Read GPIOVALL or GPIOVALH (returned in HEX format)
2. Invert the bit(s) for the rails or GPOs to be toggled
3. Write the new value to GPIOVALL or GPIOVALH

To toggle EN4 from 0 to 1 starting with the values given in Table 3, reading GPIOVALH returns 0x55h. Inverting bit 11 and writing 0x5Dh back to GPIOVALH toggles EN4.

Table 2. Rail Enable and GPO Register Information

REGISTER NAME	ADDRESS	ACCESS	ADJUSTMENT AFTER ACCESS
GPIOVALL	0x1Ah	rw	+0 (0x1Ah)
GPIOVALH	0x1Bh	rw	+0 (0x1Bh)

Table 3. GPIOVAL Control Bit Definition for ENx and GPOx

	GPIOVALH (0x1Bh)								GPIOVALl (0x1Ah)						
ENx/GPOx	**EN8**	**EN7**	**EN6**	**EN5**	**EN4**	**EN3**	**EN2**	**EN1**				**GPO4**	**GPO3**	**GPO2**	**EN8/GPO1**
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
VALUE 0=logic low 1=logic high	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0

Texas Instruments provides a generic GUI for sending and receiving I²C commands over the USB adapter and is useful for testing of this feature. To download and install the USB-to-I²C GUI, go to http://focus.ti.com/docs/toolsw/folders/print/usb-to-gpio.html, click on Support Software and download sllc288.zip, titled *Reference GUIs and Libraries for Eval and Usage of the USB Interface Adapter*. Open the *.zip file and extract USB Interface Adapter GUI-v1.10.zip. If a Texas Instruments USB Interface Adapter is being used, also extract USB Interface Adapter Driver.zip to install the required drivers.

Texas Instruments also includes an SMBus & SAA Debug Tool with the Fusion Digital Power GUI installation (Figure 30). Using the Fusion SMBus and SAA Debug Tool (http://focus.ti.com/docs/toolsw/folders/print/fusion_digital_power_designer.html), registers in the UCD9081 can be read or written to by entering the Device Address in decimal or hex format. For example, if the EVM jumpers are set to “F” then the device address is “6Fh” or "111d". The device address can be found at the bottom of the UCD9081 GUI when it is connected to an EVM or other active device. The device address is entered into the "Target" field at the top of the GUI. Before reading or writing with the GUI, click on the SAA Settings button and make sure that the "100kHz" button under "Bus Speed" is checked and that "Disabled" button under "PEC (Packet Error Checking)" is checked.

To write to the device use the "Write Data" box:

- Check the "Write Byte" button
- Enter the register address (1B, for example) in hexadecimal format in the Cmd box
- Enter the value to be written in hexadecimal format in the Data box
- Click the "Send" button
- If successful "ACK" will appear under Status

To read from the device use the "Read Data" box:

- Check the "Read Byte" button
- Enter the register address (1B, for example) in hexadecimal format in the Cmd box
- Click the "Send" button

- The value stored in the register will be reported in hexadecimal format in the Data box
- If successful "ACK" will appear under Status

Figure 30 shows the value “BAh” being written to device address “111d” or “6Fh” and register address 0x1Bh. Referring to Table 2 and Table 3, EN8, EN6, EN5, EN4, and EN2 are being set to “1” and EN7, EN3 and EN1 are being set to “0”. Writing to register address 0x1Ah allows manipulation of the GPOs. EN8 is shown as two different bits within GPIOVAL. If EN8/GPO1 is configured as EN8, then it is controlled by bit 8 of GPIOVALH. If EN8/GPO1 is configured as GPO1, then it is controlled by bit 1 of GPIOVALL.

User-selected dependencies and alarm processing still apply when manipulating a single rail using I²C. Manually disabling a rail forces a failure on that rail if the rail voltage falls below the UV threshold for that rail. If the rail is configured to respond to a failure, then that response will be carried out.

For example, if Rail 1 is set for Retry Continuously or Retry n Times and n is not equal to 0, then if EN1 is disabled causing Rail 1 to fall out of regulation, EN1 will be reasserted by the UCD9081. To control a single rail without affecting the rest of the system, that rail must be configured so that no other rails or GPOs are shut down or Alarm Processing is set to Ignore, Log Only or Retry 0. If Retry 0 is selected, then Sequence After Shutdown cannot be selected because after the rail is disabled with no retries, then the UCD9081 will restart. Another way to prevent Alarm Processing or disabling dependent rails or GPOs is to set the UV threshold to 0V so that when the rail is disabled, no fault or error is flagged.

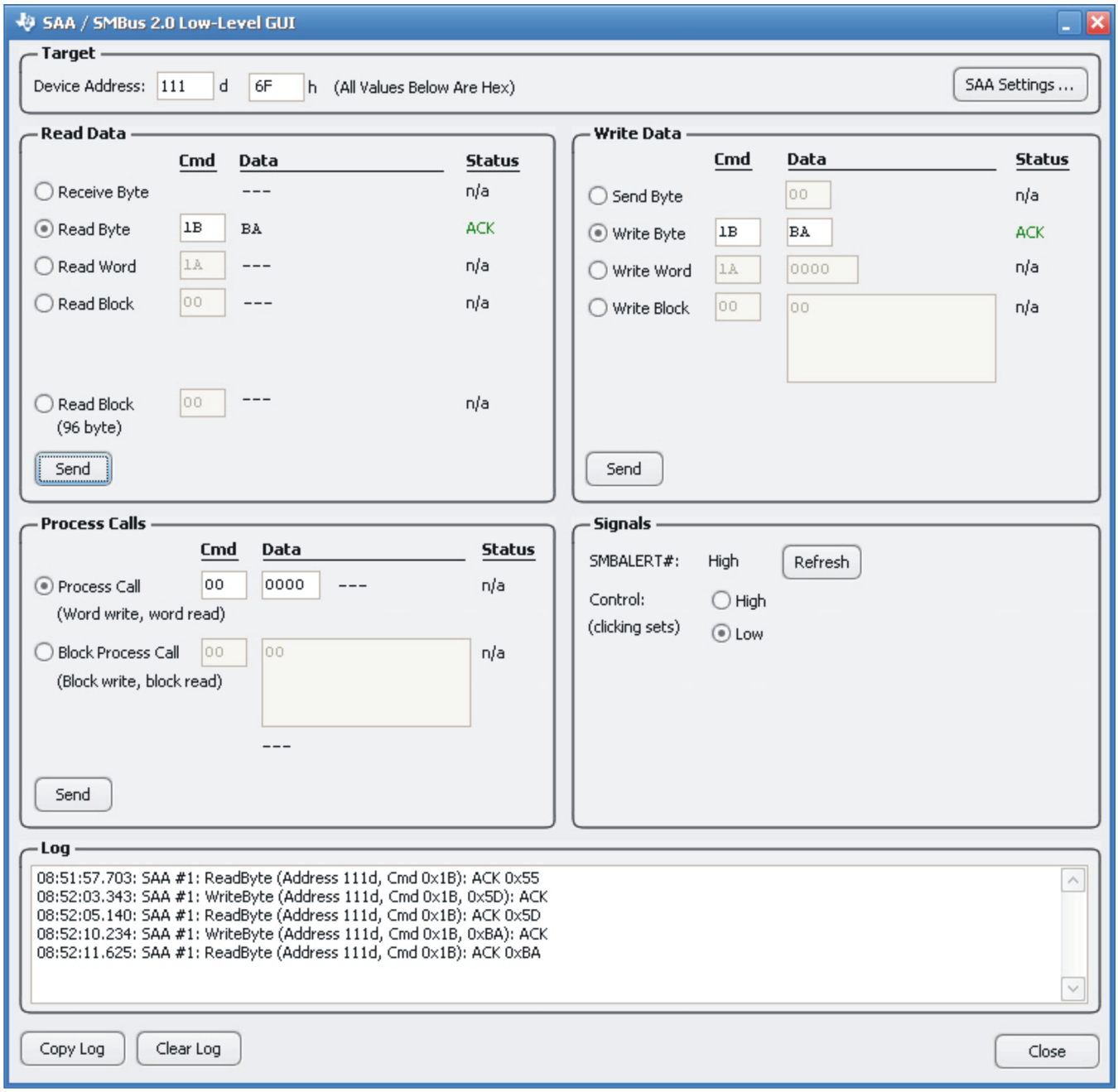


Figure 30. USB to I²C Adapter GUI for Manual Register Reads and Writes

6 System Design Considerations

The UCD9081 is a stand-alone device but it does require some supporting components, such as pullup resistors and decoupling capacitors. Also, some RESET timing and standard layout issues must be considered. Most of this information can be found in the UCD9081 data sheet (SLVS813).

The UCD9081 operates at a relatively low frequency (8 MHz maximum) and very low power. Although layout, routing, and decoupling requirements are not stringent, typical best practices are recommended. A 1-μF or larger decoupling capacitor must be provided as close to V_{CC} (pin 30) and V_{SS} (pin 1) as possible to minimize the loop area for high-frequency supply current into the device. Each ENx output must have a pullup or pulldown resistor that disables the power supply being controlled. When choosing the ENx resistors, see the UCD9081 data sheet for information relating to high- and low-level output voltage and current.

No-connect (NC) pins 4, 17, 20, and 31 and TEST pin 29 must all be tied to V_{SS}. NC pin 2 must be left open. All unused ENx and GPOx pins must be terminated with a pullup or pulldown resistor to force the outputs to a known state during operation. I^2C address inputs (ADDR) are read during RESET and must have weak pullup or pulldown resistors (1 kΩ to 10 kΩ) added so that a communication address can be established. Then, those four multiplexed pins can be used as GPOs during normal operation. I^2C inputs SCL and SDA must each have 10-kΩ pullups to V_{CC}.

The UCD9081 package has a 3.45-mm × 3.45-mm exposed thermal pad on the board side. It is recommended that the thermal pad be tied to V_{ss} to improve thermal performance and to potentially reduce EMI/EMC created by the device.

A digitally controlled oscillator (DCO) establishes the clock frequency for the device. Adding a 100-kΩ resistor from V_{CC} to ROSC (pin 32) reduces the DCO frequency temperature coefficient from about –5%/°C to about –0.1%/°C.

Power-on-Reset (POR), Brownout and Reset voltage and timing requirements are given in the UCD9081 data sheet. The duration of the RESET sequence is the same whether at power up or in response to the $\overline{RST}$ pin. During RESET, a checksum function runs to validate the user configuration memory contents. If the configuration parameters are invalid, the last known good parameters are loaded into the device. A checksum error extends RESET time to about 120 ms. To establish a copy of a valid configuration, RESET takes up to 120 ms when a new configuration is first loaded. During power up, the UCD9081 begins its RESET sequence within 2 ms after V_{CC} reaches between 1.78 V and 1.89 V. If the parameter configuration file has not been updated since the last RESET, then RESET lasts about 35 ms. If the parameter file is new, then RESET takes up to 120 ms to complete. Once V_{CC} is established, if the user wishes to generate a RESET after the UCD9081 is operational the $\overline{RST}$ pin must be held low for at least 2 μs. The UCD9081 does not respond to I^2C host requests during RESET. The RESET sequence is also described in the UCD9081 datasheet.

7 Links to Other Useful Documents

1. *UCD9081, 8-Channel Power Supply Sequencer and Monitor With Error Logging* data sheet (SLVS813)
2. *Programming the UCD9081* application report (SLUA441)
3. *Expanded System Monitoring Functions With UCD9080* application report (SLUA426)
4. *UCD9081 Power Supply Sequencer and Monitor EVM* user's guide (SLVU249)
5. *TI-Fusion-Digital-Power-Designer GUI* (SLVC118)
6. *USB Interface Adapter Evaluation Module User's Guide* (SLLU093)

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