TPS740xxDGKEVM-722 Evaluation Module

This user's guide describes the characteristics, operation, and use of the TPS74001DGKEVM-722 and TPS74012DGKEVM-722 evaluation modules (EVM). The TPS740xxDGKEVM-722 is a fully assembled and tested platform for evaluating the performance of the TPS740xx low-dropout voltage regulator in a power MSOP-8 package. The TPS740xx family is a set of wide bandwidth, very low-dropout, 1.5-A voltage regulators, ideal for powering microprocessors, with adjustable output voltages between 0.9 V and 4 V. TPS74001DGKEVM-722 EVM has an output voltage of 1.5 V, set by external resistors, whereas the TPS74012DGKEVM-722 has an output voltage of 1.2 V, set by internal resistors and cannot be changed. This user's guide includes setup configuration instructions, a complete schematic diagram, bill of materials , and printed-circuit board layout drawings for the evaluation module.

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1 Introduction

The TPS740xxDGKEVM-722 evaluation module helps designers evaluate the operation and performance of the TPS740xx low-voltage, low-dropout regulator in an 8-pin power MSOP-8 package. This particular EVM configuration contains a low-voltage, low-dropout (LDO), 1.5-A voltage regulator with dual input voltages with input voltage range of 1.2 V to 5.5 V and input V_{BIAS} range of 3 V to 5.5 V. Two TPS740xxDGK EVMs are available: one with an adjustable output voltage and one with a fixed voltage of 1.2 V. The output voltage of TPS74001DGKEVM is adjustable and is configured with external resistors, R_1 and R_2, to 1.5 V. The output voltage for this part can be adjusted to be between 0.9 V and 4 V. The output voltage of TPS74012DGKEVM is fixed to 1.2 V, set by resistors internal to the integrated circuit (IC), and cannot be modified. The TPS740xx is also available in a 5-pin Jr S-Pak package, which has its own orderable evaluation module, TPS74001DPTEVM-713 or TPS74012DPTEVM-713. The TPS740xx is ideal for powering microprocessors.

1.1 Features

- Small consumption current: 3 mA, maximum
- Input voltage ranges:
  - V_{IN}: 1.2 V to 5.5 V
  - V_{BIAS}: 3 V to 5.5 V
- Stable with any output capacitor ≥ 2.2 µF
- ±1% initial tolerance
- Maximum dropout voltage (V_{IN} - V_{OUT}) of 300 mV over temperature
- Ultrafast transient response
- Excellent line and load regulation
- Thermal shutdown and current-limit protection
- Logic-controlled shutdown option
- Junction temperature range of –40°C to 125°C

1.2 Orderable Options

- TPS74001DGKEVM-722: EVM output voltage configured to 1.5 V by external resistors and is adjustable to between 0.9 V and 4 V
- TPS74012DGKEVM-722: fixed EVM output voltage of 1.2 V, set by resistors internal to the IC

2 Schematic

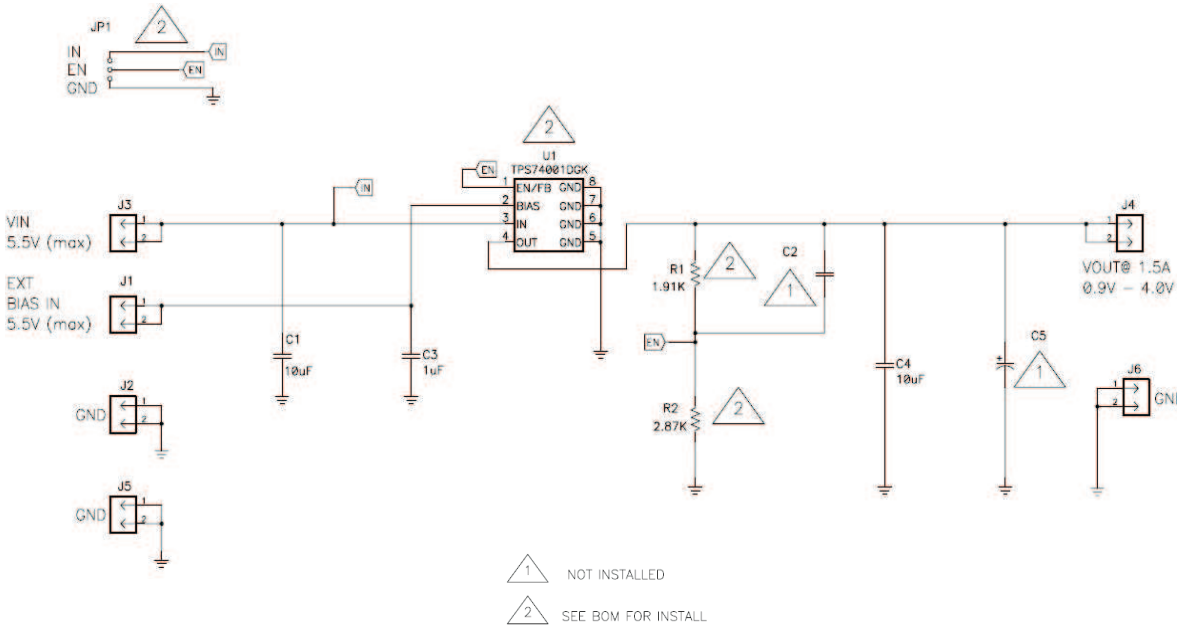

Figure 1. TPS74001DGK-722 Rev-A Schematic

3 Setup and Board Description

3.1 EVM Input/Output Connectors and Test Jumpers

Table 1. List of Input and Output Connectors

Connector	Label	Description
J1	BIAS	VBIAS input power supply connection: 3 V to 5.5 V. Used to power error amplifier, reference, and internal control circuits.
J2	GND	Return connection for V_{BIAS} input power supply.
J3	VIN	V_{IN} input power supply connection: 1.2 V to 5.5 V. Note: $V_{IN} \geq V_{OUT} + V_{DO}$ for proper operation
J4	VOUT	Regulated output voltage connection.
J5	GND	Return connection for V_{IN} input power supply.
J6	GND	Return connection for V_{OUT}.
JP1	IN/EN/GND	Ties EN pin to either V_{IN} (high) or GND (low). Used for TPS74012DGK only. Not used for TPS74001DGK. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.

3.2 Connection Setup

1. Connect power supply #1 to V_{IN} (J3) and its return connection to J5 as shown in Figure 2. V_{IN} must be at least 300 mV (or V_{DO}) greater than V_{OUT}, up to 5.5 V.
2. Connect power supply #2 to V_{BIAS} (J1) and its return connection to J2 as shown in Figure 2. V_{BIAS} must be between 3 V and 5.5 V.
3. An ammeter can be connected in series with either power supply to measure the supply current or bias current.
4. For TPS74012DGK (fixed voltage part), attach a jumper on JP1, shorting EN and V_{IN} (ties EN high).
5. If desired, a load can be connected at the output, J4 and J6.
6. Connect a voltmeter or an oscilloscope voltage probe across the output pins J4 and J6 to observe and measure the regulated output voltage.

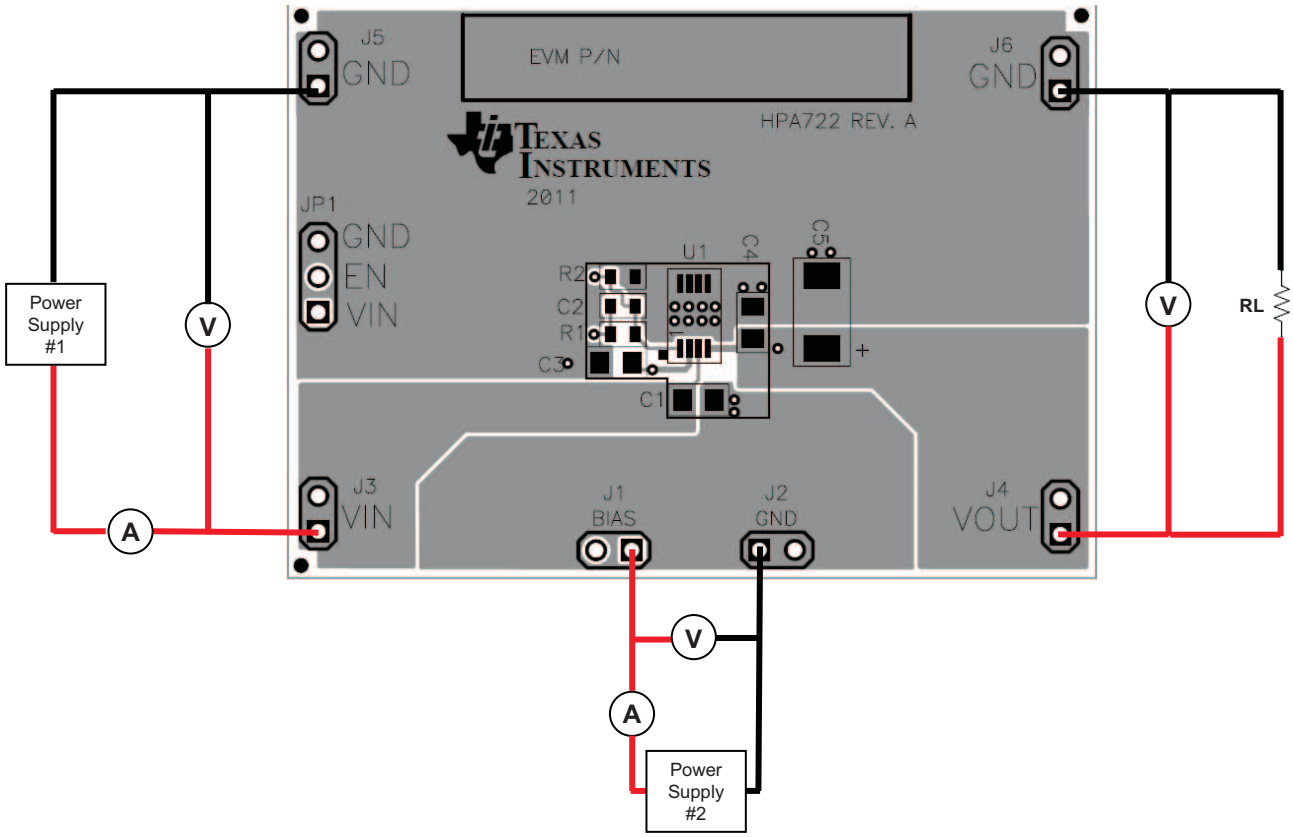

Figure 2. Quick-Start Connection Setup

4 Operation

This section provides information about the operation of the TPS740xxDGK EVM and expected outputs. The TPS740xx parts can support input voltages (V_{IN}) between 1.2 V and 5.5 V and output voltages (V_{OUT}) between 0.9 V and 4 V. A separate V_{BIAS} input supply (3 V to 5.5 V) powers the error amplifier, reference, and internal control circuits to allow for very low main input supply voltage. The TPS740xx requires only a small output ceramic capacitor of 2.2 µF (minimum) to ensure stability of the IC.

4.1 Adjustable Output Voltage

TPS74001DGK EVM comes configured for a 1.5-V output voltage. However, this output voltage can easily be modified to range between 0.9 V and 4 V by changing the values of the resistors R_1 and R_2 that form a voltage divider at the output of the IC. In order to achieve maximum accuracy, R_2 is recommended to be lower than 4.99 kΩ. Proper values for R_1 and R_2 for a desired V_{OUT} can be calculated using:

$$V_{OUT} = 0.9 \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Sample resistor values of common output voltages are shown in Table 2.

Table 2. Sample Resistor Values for Common Output Voltages for TPS74001DGK

R_1 [kΩ]	R_2 [kΩ]	VOUT [V]
Short	Open	0.9
0.562	5.11	1
0.75	4.53	1.05

Table 2. Sample Resistor Values for Common Output Voltages for TPS74001DGK (continued)

R_1 [kΩ]	R_2 [kΩ]	VOUT [V]
1.07	4.99	1.1
1.58	4.75	1.2
1.91	2.87	1.5
2.43	2.43	1.8
3.01	1.69	2.5
4.22	1.58	3.3
5.23	1.74	3.6

TPS74012DGKEVM is a fixed output voltage IC and cannot be modified. The output voltage is fixed at 1.2 V.

4.2 Transient Response

The TPS740xx is designed to have excellent transient response for most applications with a small amount of output capacitance. The TPS740xx is stable with a ceramic output capacitor as low as 2.2 µF. Additional output capacitance serve to reduce undershoot and overshoot at the output during a transient event.

Figure 3 is an example load transient response captured with V_{IN} = 3.5 V, V_{BIAS} = 5 V, Load = 1.2 A.

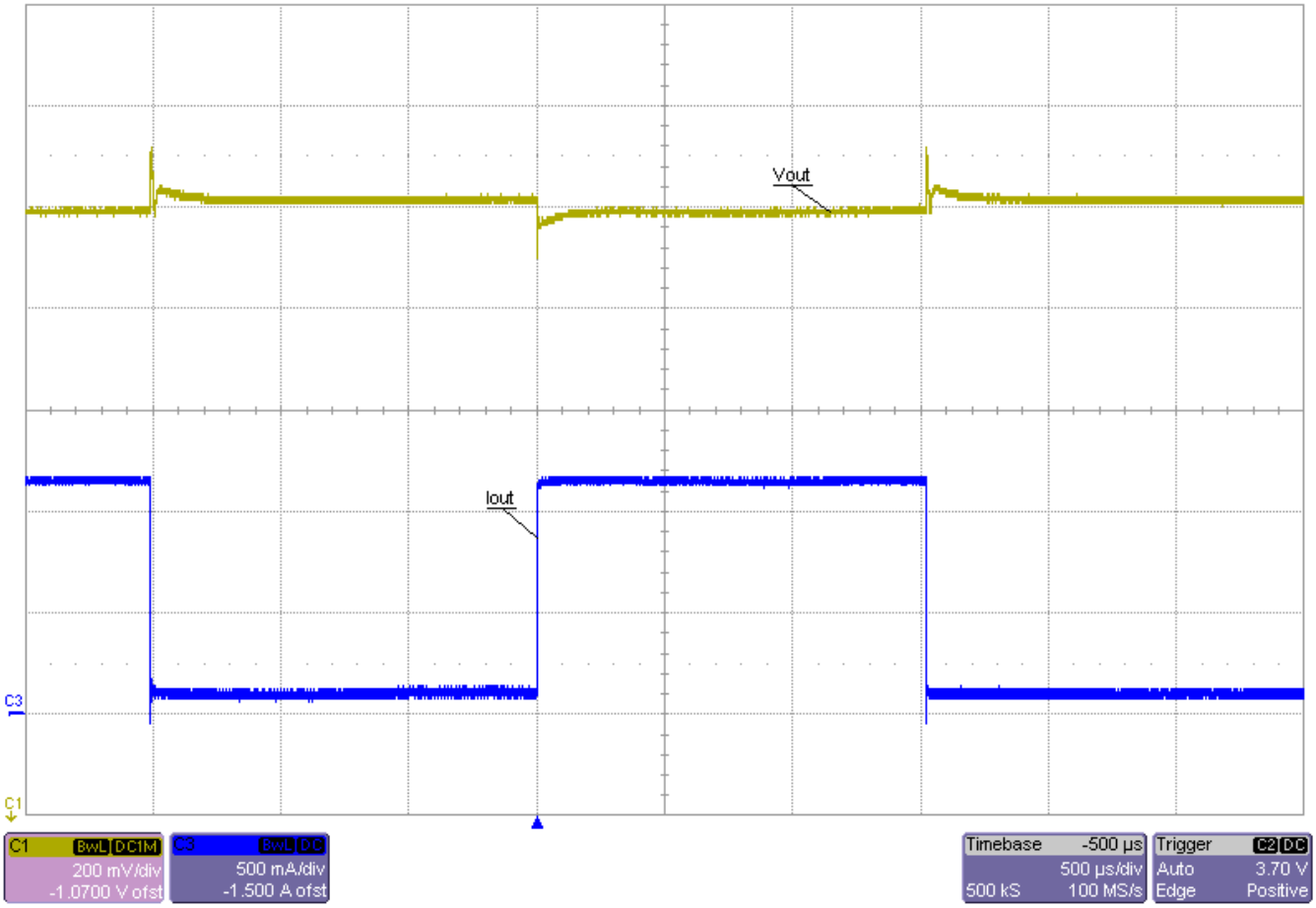

Figure 3. Transient Response of TPS74001DGKEVM With V_{IN} = 3.5 V, V_{BIAS} = 5 V, Load = 1.2 A

4.3 Dropout Voltage, V_{DO}

TPS740xxDGK offers very low dropout performance and allows the device to be used in place of a dc/dc converter and still achieve good efficiency. The V_{IN} dropout voltage, V_{IN}-V_{OUT}, for the TPS740xxDGK is specified to be a maximum of 300 mV at 1.5-A load for V_{BIAS} = V_{OUT} + 2 V. The V_{IN} dropout voltage decreases as V_{BIAS} increases.

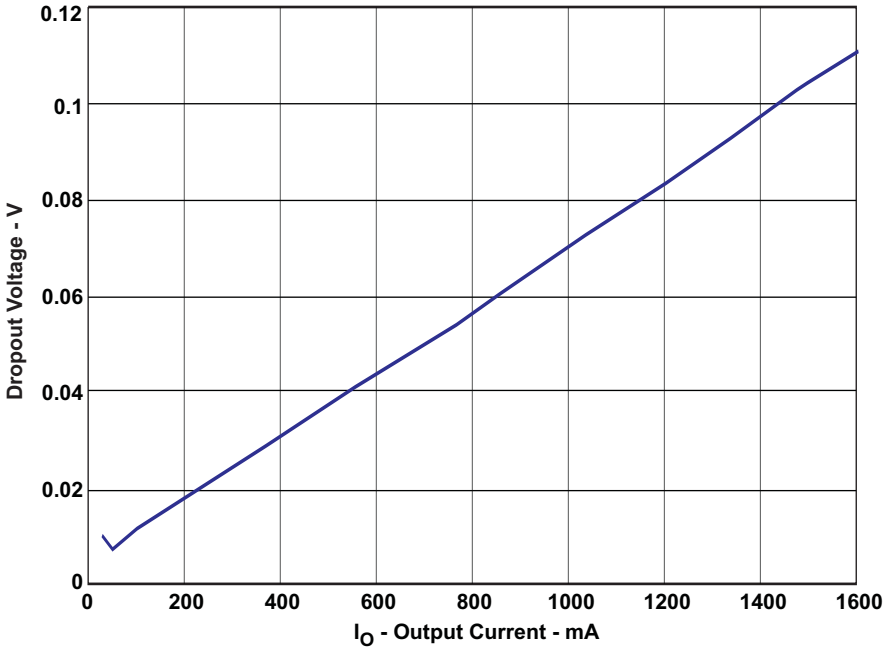

Figure 4. Dropout Voltage, V_{DO}, Measurement of TPS74001DGKEVM for V_{BIAS} = 5 V, V_{OUT} = 1.5 V

4.4 Enable/Shutdown, Fixed Voltage Version Only – TPS74012DGK

The EN pin is active high and enables the regulator. When V_{EN} is above 1.1 V, the regulator turns on. When V_{EN} is below 0.4 V, the regulator turns off. The enable circuitry has hysteresis and deglitching to help avoid on/off cycling as a result of small glitches in the V_{EN} signal. V_{EN} threshold is typically 0.8 V but varies slightly with temperature and process variations. See the TPS740xx data sheet for more information.

4.5 Internal Current Limit

TPS740xxDGK features an internal current-limit protection circuitry that is designed to protect against overload conditions. The current limit responds in approximately 10 µs to reduce the current during a short-circuit fault. The current-limit circuitry allows up to a maximum of 4 A before clamping the output current. The resulting V_{OUT} is 80% of V_{OUT}, nominal. See the TPS740xx data sheet for more information.

4.6 Thermal Protection

TPS740xxDGK comes with a thermal protection circuit that disables the output of the IC when the junction temperature rises to approximately 160°C. When the junction temperature cools down to approximately 140°C, the output circuitry is once again enabled. The thermal protection circuit may cycle on and off depending on the power dissipation, thermal resistance, and ambient temperature of the EVM. See the TPS740xx data sheet for more information.

5 Board Layout

This section provides the TPS740xxDGKEVM-722 printed-circuit board (PCB) layout and illustrations.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS740xxDGKEVM-722 PCBs.

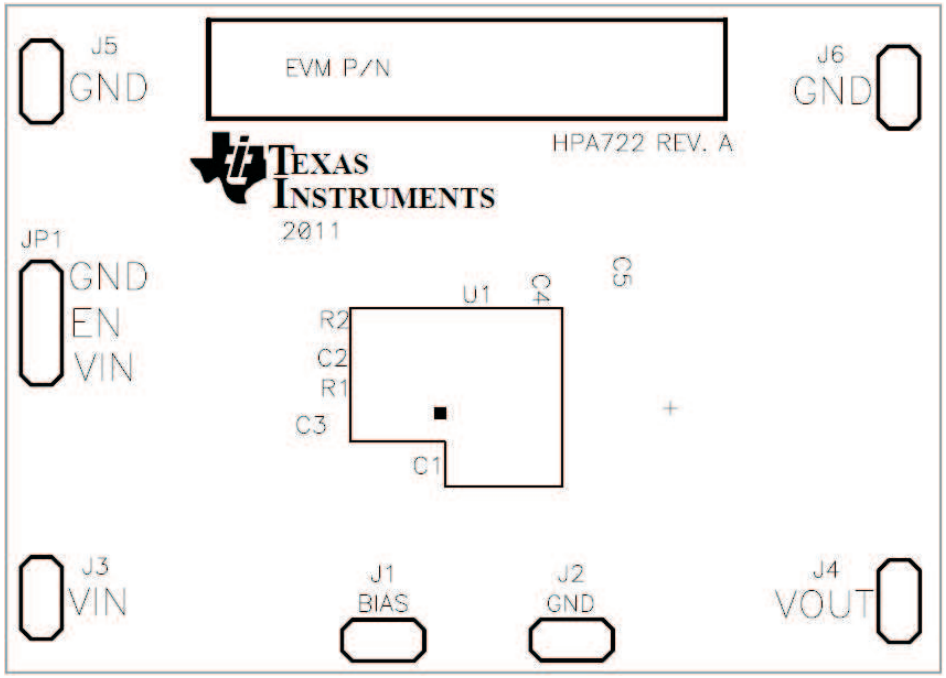

Figure 5. Silkscreen Layer

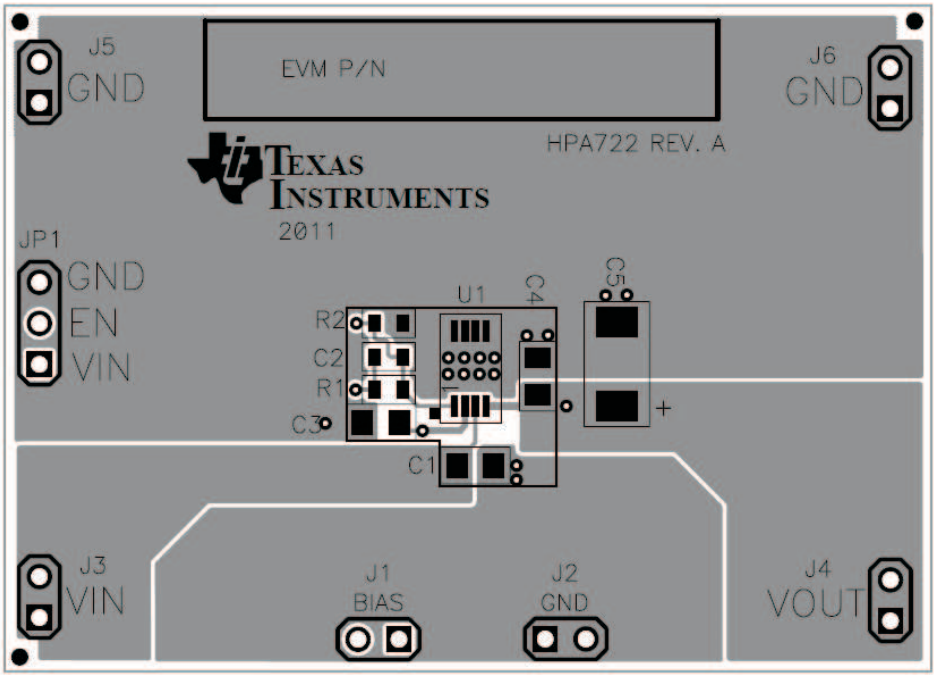

Figure 6. Assembly Layer

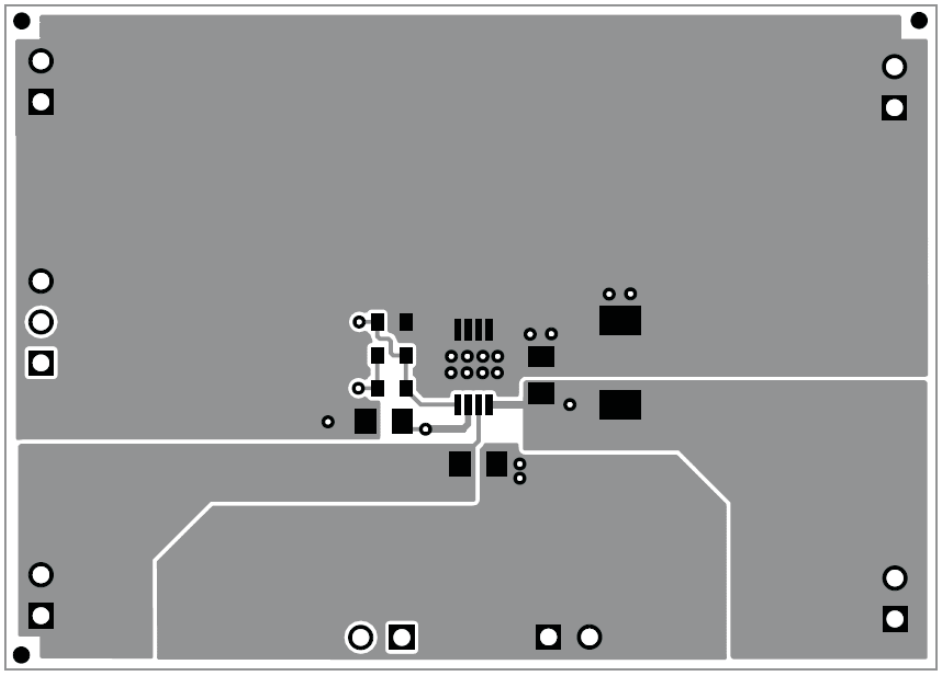

Figure 7. Top Layer Routing

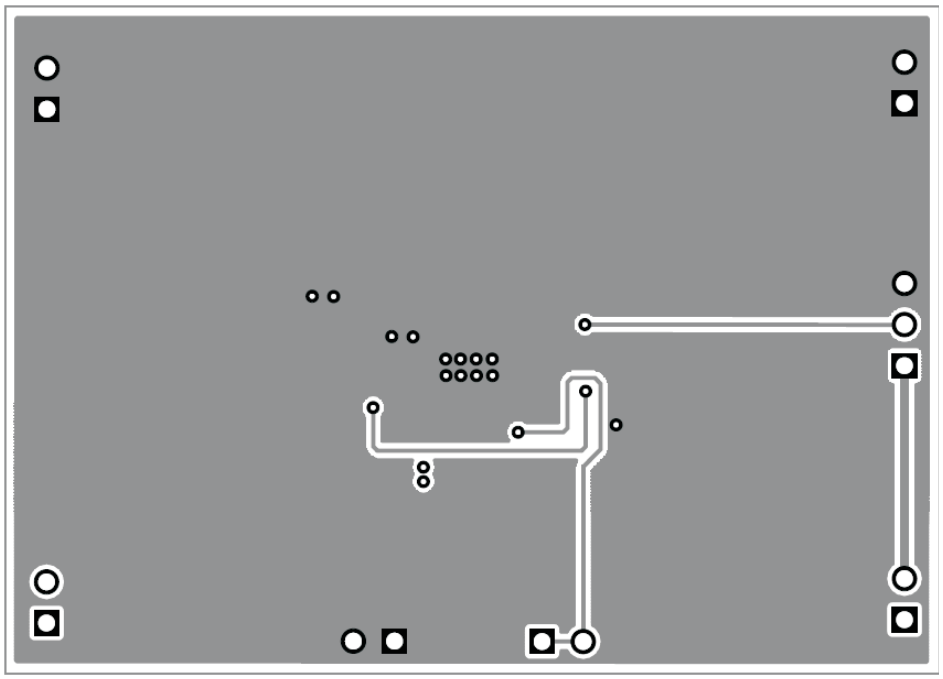

Figure 8. Bottom Layer Routing

6 Bill of Materials

Table 3. Bill of Materials

HPA722-001	HPA722-002						
Count	**Count**	**RefDes**	**Value**	**Description**	**Size**	**Part Number**	**MFR**
2	2	C1, C4	10 µF	Capacitor, Ceramic,10V, X5R 20%	0805	STD	STD
0	0	C2	DNI	Capacitor, Ceramic	0603	STD	STD
1	1	C3	1 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0805	STD	STD
0	0	C5	DNI	Capacitor, Ceramic	6032	STD	STD
6	6	J1, J2, J3, J4, J5, J6	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	1	JP1	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	0	R1	1.91K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	0	R2	2.87K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	0	U1	TPS74001DGK	IC, 1.5A Low Voltage LDO Regulator with Dual Input Voltages	MSOP	TPS74001DGK	TI
0	1	U1	TPS74012DGK	IC, 1.5A Low Voltage LDO Regulator with Dual Input Voltages	MSOP	TPS74012DGK	TI

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.
5. Install label after final wash. Text shall be 8 pt font. Text shall be per Table 4.

Table 4. Assembly Number and Corresponding Label Text

ASSEMBLY NUMBER	TEXT
HPA722-001	TPS74001DGKEVM-722
HPA722-002	TPS74012DGKEVM-722

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 1.2 V to 5.5 V and the output voltage range of 0.9 V to 4 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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