UCC27423-4-5-Q1 EVM User's Guide

This user's guide describes the UCC27423-4-5-Q1 evaluation module (EVM). This document contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

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1 Introduction

The UCC27423-4-5-Q1 EVM is a high-speed dual MOSFET evaluation module that provides a test platform for a quick and easy startup of the UCC2742x-Q1 driver. The EVM is powered by a single 4 V to 15 V external supply and features a comprehensive set of test points and jumpers. All of the devices have separate input and output lines and all devices share a common ground. Enable (ENBL) functions are provided to allow better control of the operation of the driver applications, driver signals of the devices can be enabled or disabled through the same enable pin.

1.1 Related Documentation

For more information on the UCC27423-Q1, UCC27424-Q1, and UCC27425-Q1 devices refer to *UCC2742x-Q1 Dual 4-A High-Speed Low-Side MOSFET Drivers With Enable*.

Table 1. EVM Compatible Devices

Part Number	Description	Package
UCC27323, *UCC27324*, *UCC27325*, *UCC37323*, *UCC37324*, *UCC37325*	Dual 4A Low-Side TTL/CMOS	This EVM is compatible with SOIC and MSOP-PowerPAD™ 8-pin packages.
UCC27324-Q1	Dual 4A Low-Side TTL/CMOS	
UCC27423, *UCC27424*, *UCC27425*	Dual 4A Low-Side TTL/CMOS with ENABLE	
UCC27523, *UCC27524*, *UCC27525*	Dual 5A Low-Side TTL/CMOS with ENABLE	
UCC27524A	Dual 5A Low-Side TTL/CMOS with ENABLE and Negative Input Capability	
UCC27524A-Q1	Dual 5A Low-Side TTL/CMOS with ENABLE and Negative Input Capability	
UCC27528	Dual 5A Low-Side CMOS with ENABLE	
UCC27528-Q1	Dual 5A Low-Side CMOS with ENABLE	
LM5110	Dual 3A-source 5A-sink Low-Side TTL with ENABLE and Negative Input Capability	
LM5111	Dual 3A-source 5A-sink Low-Side TTL	
LM5112	Single 3A-source 7A-sink Low-Side TTL with Split Supply	
TPS2811, *TPS2812*, *TPS2813*	Dual 2A Low-Side CMOS with Internal Regulator	
EMB1412	Single 3A-source 7A-sink Low-Side CMOS/TTL with Split Supply	

1.2 UCC2742x-Q1 Applications

The UCC2742x-Q1 family of devices can be used in the following applications:

- Switch Mode Power Supplies
- DC-DC Converters
- Motor Controllers
- Class D Switching Amplifiers

2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the UCC27423-4-5-Q1 EVM schematic, bill of materials (BOM), and layout.

2.1 UCC27423-4-5-Q1 EVM Schematic

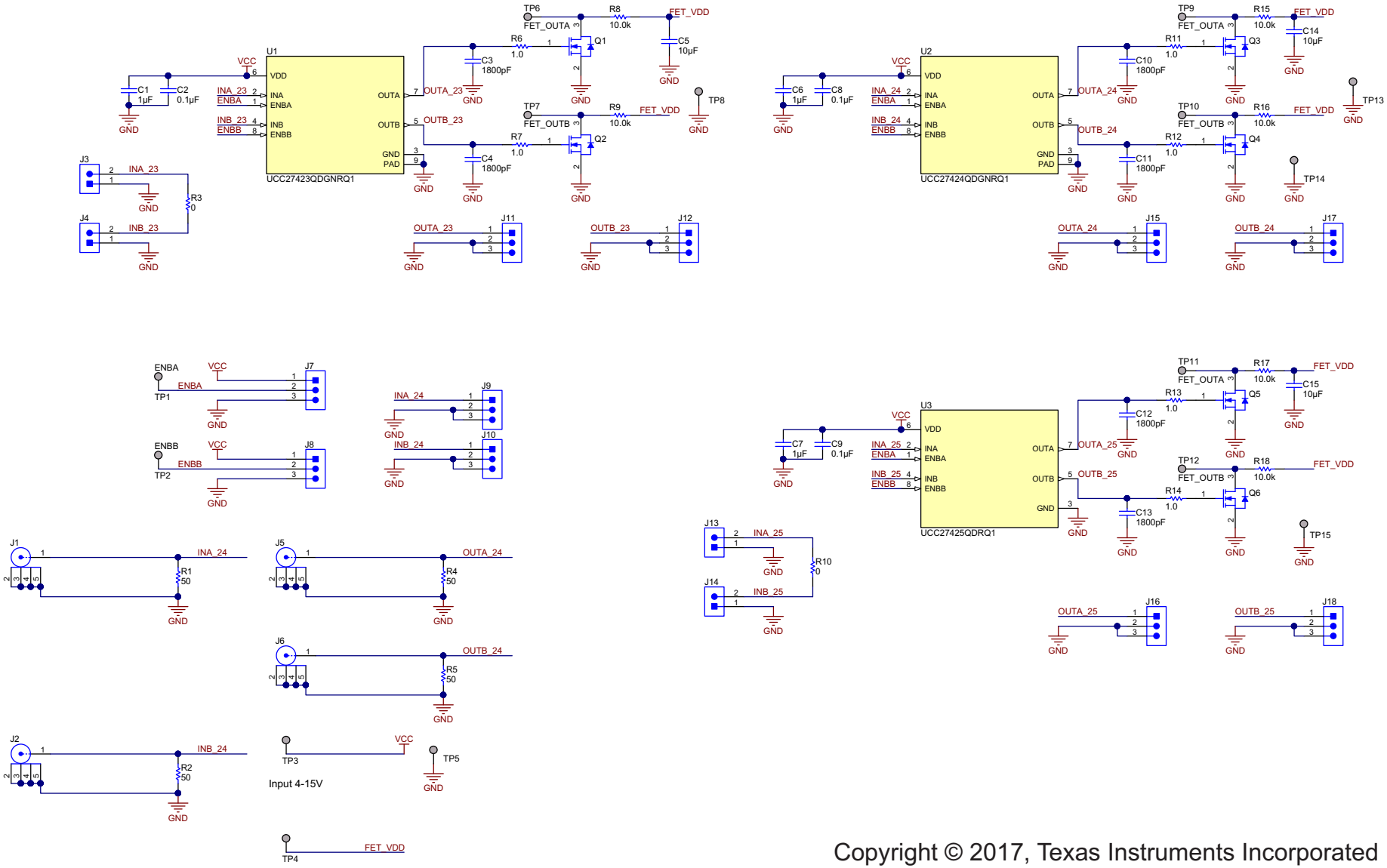


Figure 1. UCC27423-4-5-Q1 EVM Schematic

2.2 UCC27423-4-5-Q1 EVM Bill of Materials

Table 2. BOM

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
PCB1	1		Printed Circuit Board		MSA022	Any
C1, C6, C7	3	1uF	CAP, CERM, 1 µF, 100 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206	1206	CGA5L2X7R2A105K160AA	TDK
C2, C8, C9	3	0.1uF	CAP, CERM, 0.1 µF, 50 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E2X7R1H104K080AA	TDK
C3, C4, C10, C11, C12, C13	6	1800pF	CAP, CERM, 1800 pF, 25 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCJ216R71E182KA01D	MuRata
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J3, J4, J13, J14	4		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions
J7, J8, J9, J10, J11, J12, J15, J16, J17, J18	10		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
TP3, TP4, TP5, TP8, TP13, TP14, TP15	7		PCB Pin, Swage Mount, TH	PCB Pin(2505-2)	2505-2-00-44-00-00-07-0	Mill-Max
U1	1		Dual 4-A High-Speed Low-Side MOSFET Drivers With Enable, DGN0008B	DGN0008B	UCC27423QDGNRQ1	Texas Instruments
U2	1		Dual 4-A High-Speed Low-Side MOSFET Drivers With Enable, DGN0008B	DGN0008B	UCC27424QDGNRQ1	Texas Instruments
U3	1		Dual 4-A High-Speed Low-Side MOSFET Drivers With Enable, D0008A	D0008A	UCC27425QDRQ1	Texas Instruments
C5, C14, C15	0	10uF	CAP, CERM, 10 µF, 50 V, ± 10%, X7S, AEC-Q200 Grade 1, 1210	1210	CGA6P3X7S1H106K250AB	TDK
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
J1, J2, J5, J6	0		Jack, SMA, PCB, Gold, SMT	SMA Jack	CONSMA001-SMD-G	Linx Technologies
Q1, Q2, Q3, Q4, Q5, Q6	0	30V	MOSFET, N-CH, 30 V, 3.7 A, AEC-Q101, SOT-23	SOT-23	BSR302NL6327HTSA1	Infineon Technologies
R1, R2, R4, R5	0	50	RES, 50, 1%, 0.1 W, 0603	0603	CRCW060350R0FKEA	Vishay-Dale
R3, R10	0	0	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America
R6, R7, R11, R12, R13, R14	0	1.0	RES, 1.0, 5%, 0.063 W, 0402	0402	CRCW04021R00JNED	Vishay-Dale
R8, R9, R15, R16, R17, R18	0	10.0k	RES, 10.0 k, 1%, 0.25 W, 1206	1206	CRCW120610K0FKEA	Vishay-Dale
TP6, TP7, TP9, TP10, TP11, TP12	0		PCB Pin, Swage Mount, TH	PCB Pin(2505-2)	2505-2-00-44-00-00-07-0	Mill-Max

2.3 Layout and Component Placement

Figure 2 and Figure 3 top and bottom assemblies of the printed circuit board (PCB) show the component placement on the EVM.

Figure 4 and Figure 5 show the top and bottom layouts, Figure 6 and Figure 7 show the top and bottom layers, and Figure 8 and Figure 9 show the top and bottom solder masks of the EVM.

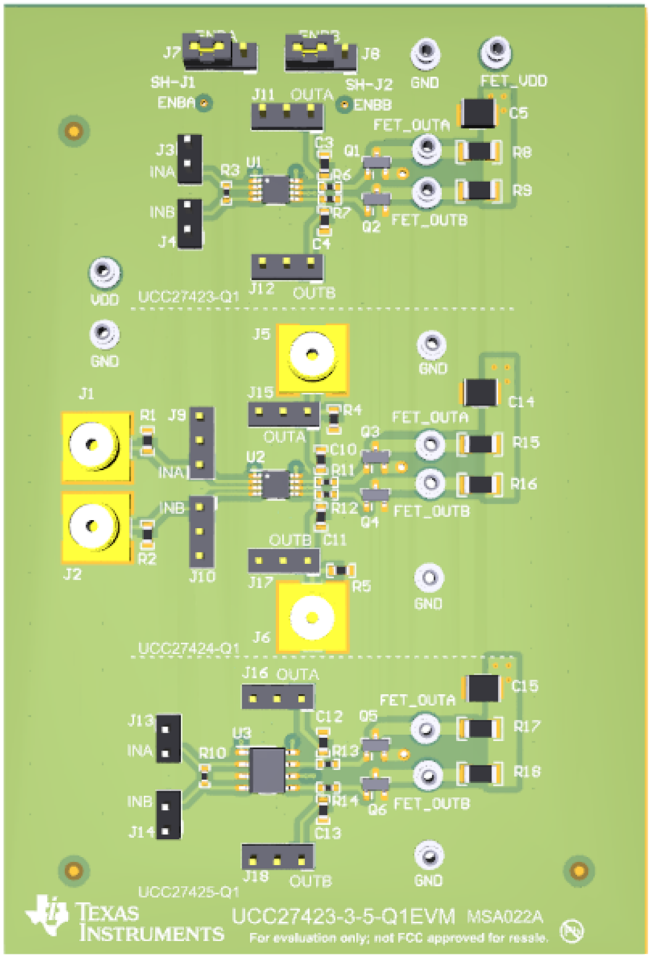


Figure 2. Component Placement—Top Assembly

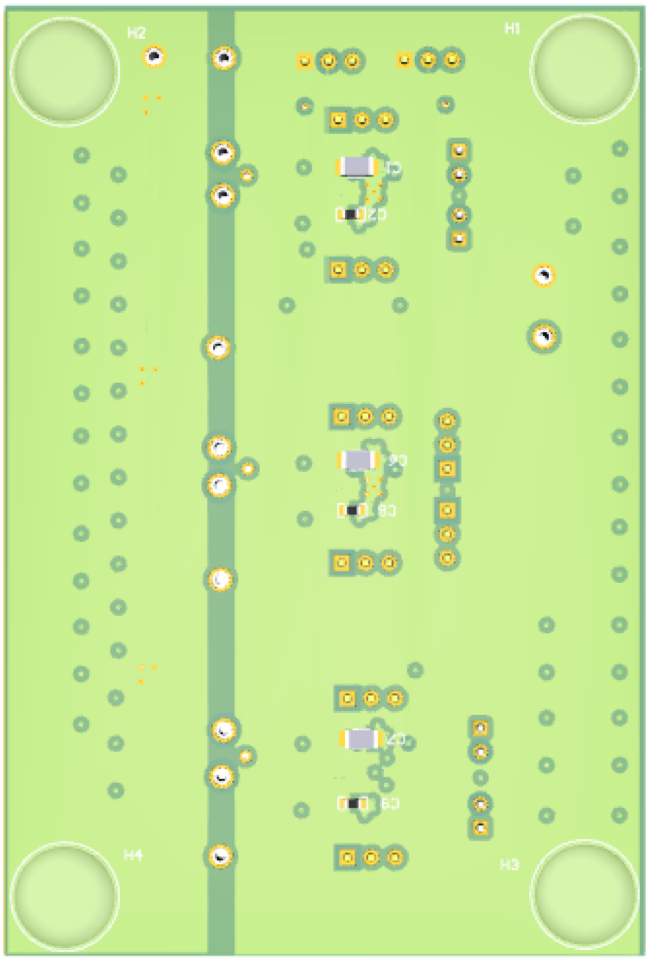


Figure 3. Component Placement—Bottom Assembly

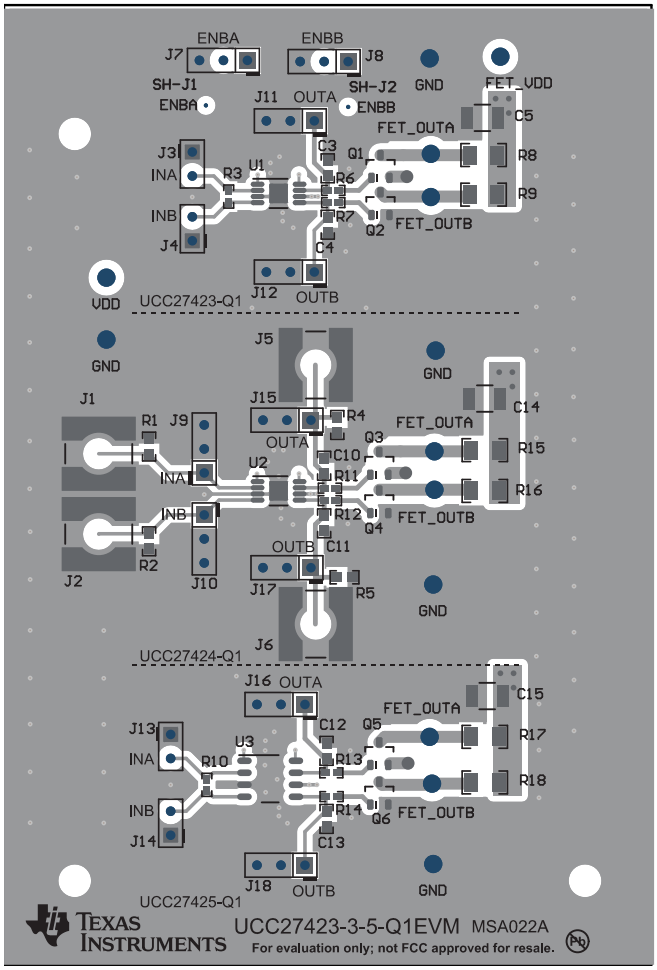


Figure 4. Layout—Top

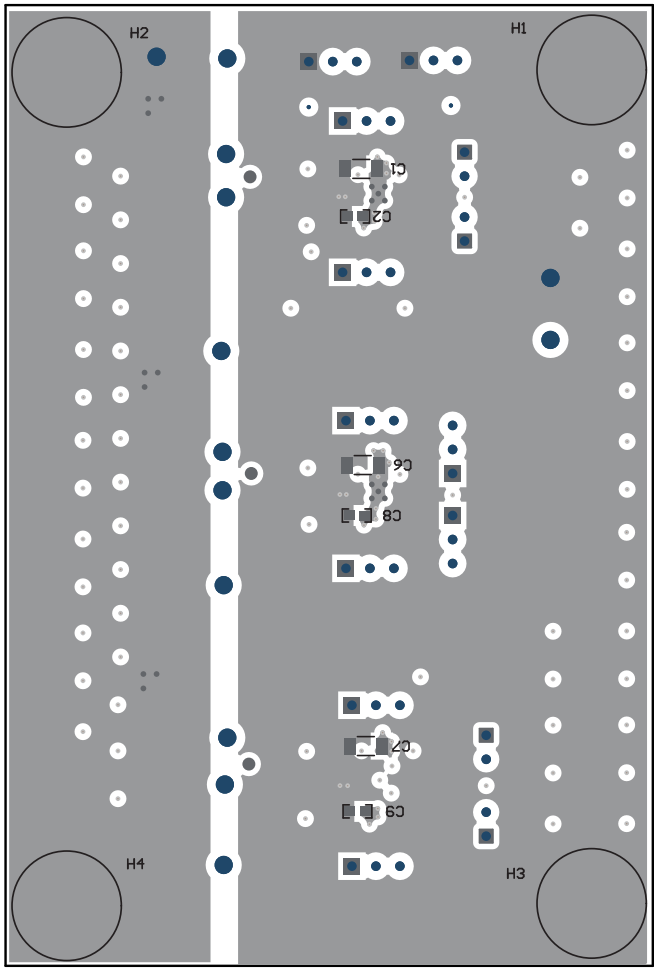


Figure 5. Layout—Bottom

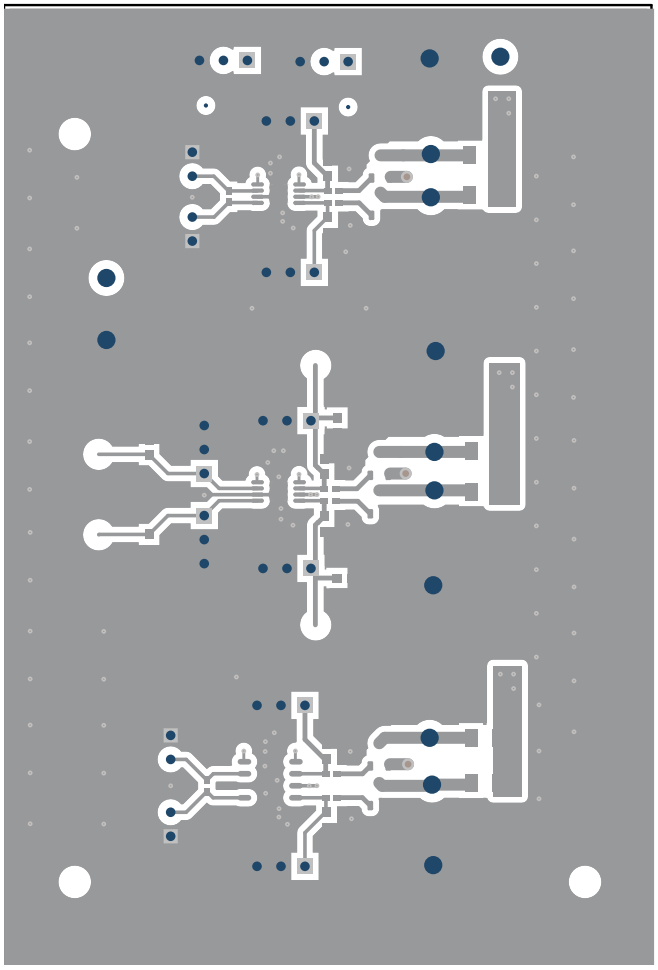


Figure 6. Top Layer

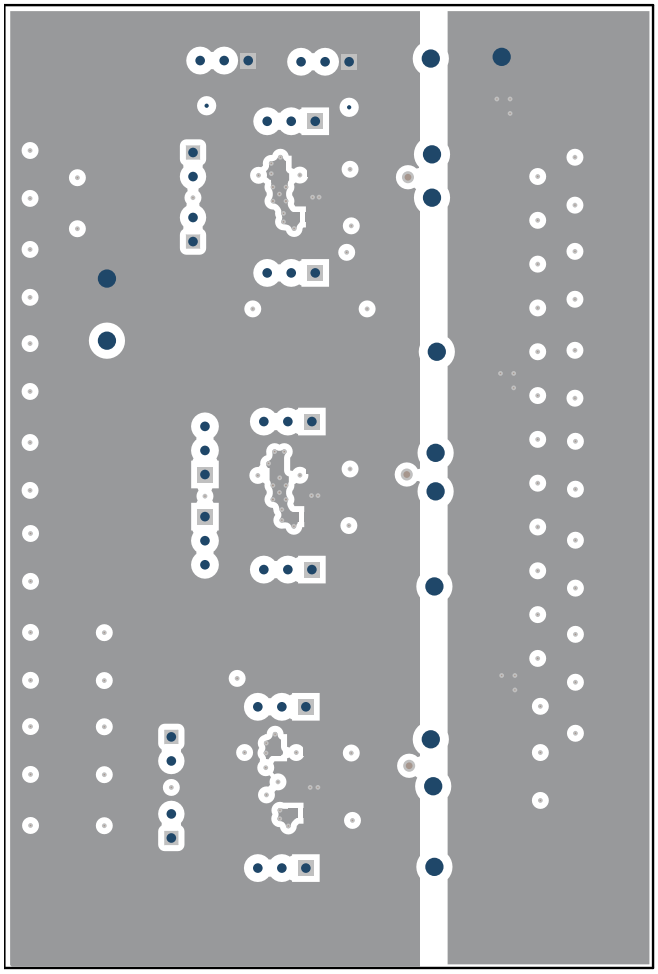


Figure 7. Bottom Layer

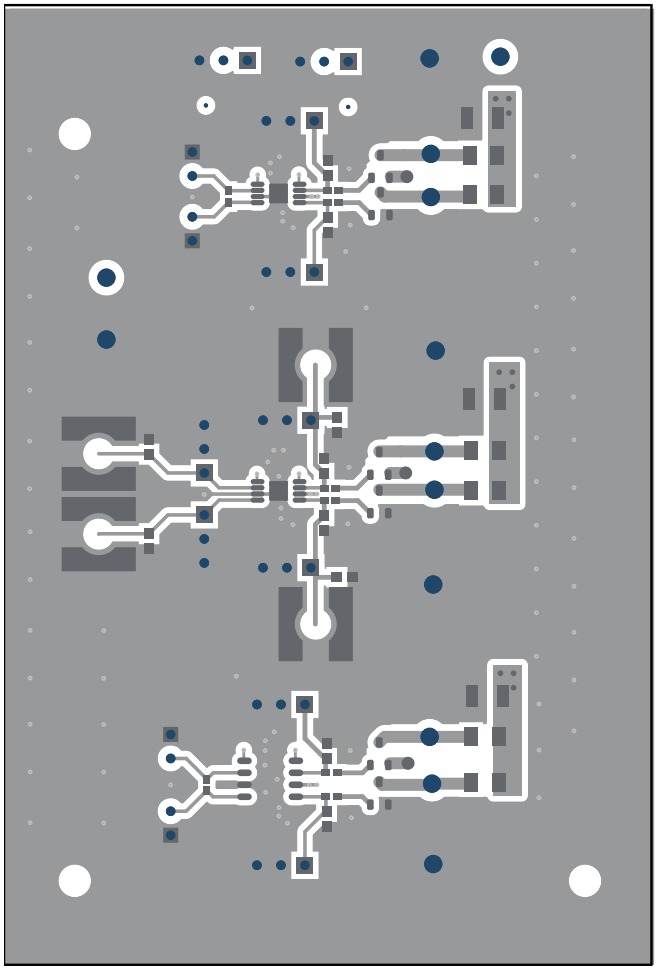


Figure 8. Top Solder Mask

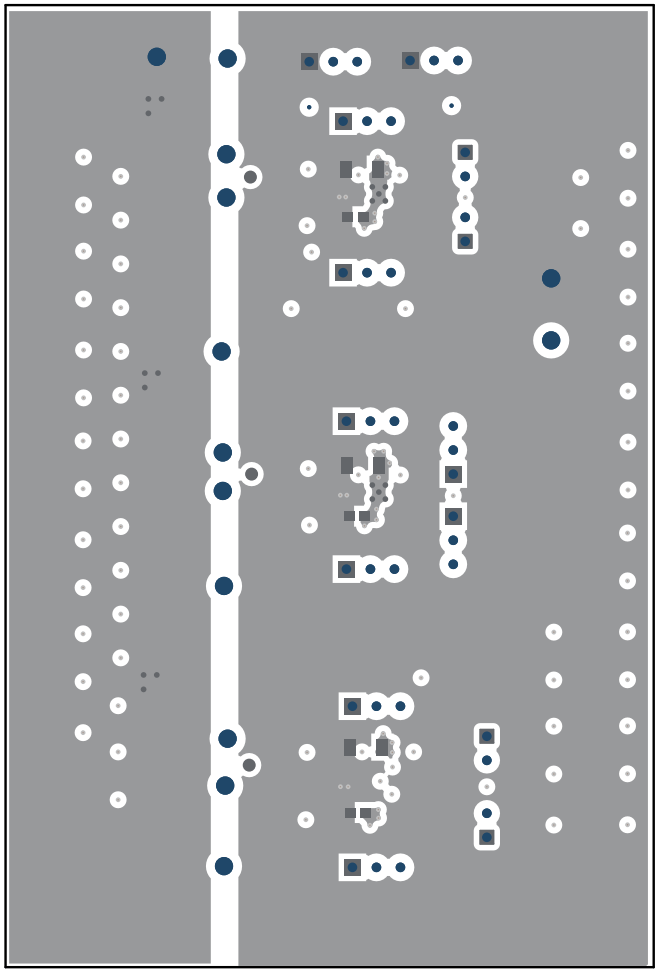


Figure 9. Bottom Solder Mask

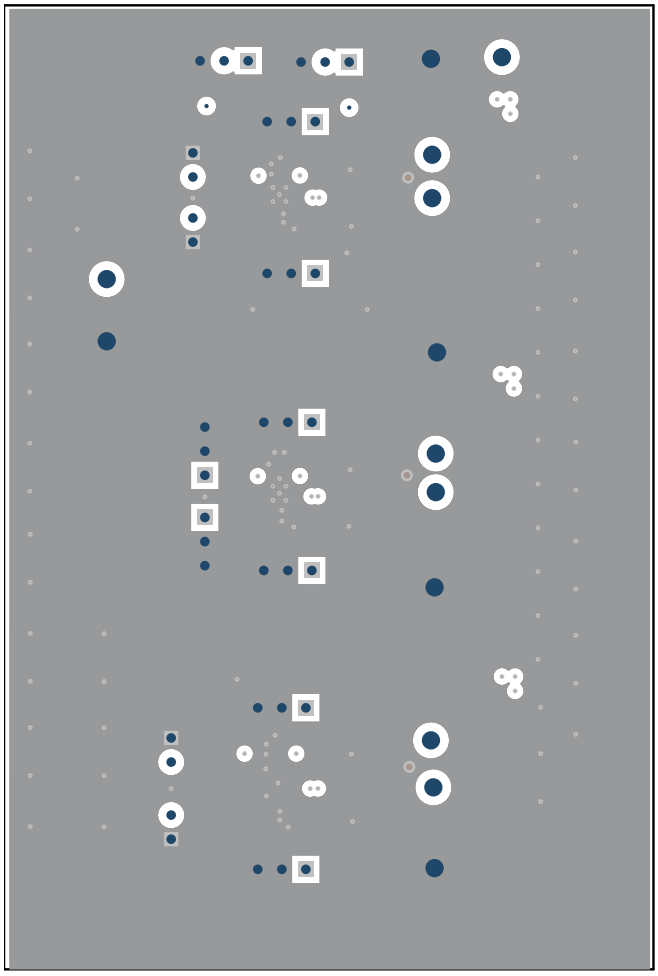


Figure 10. Ground Layer

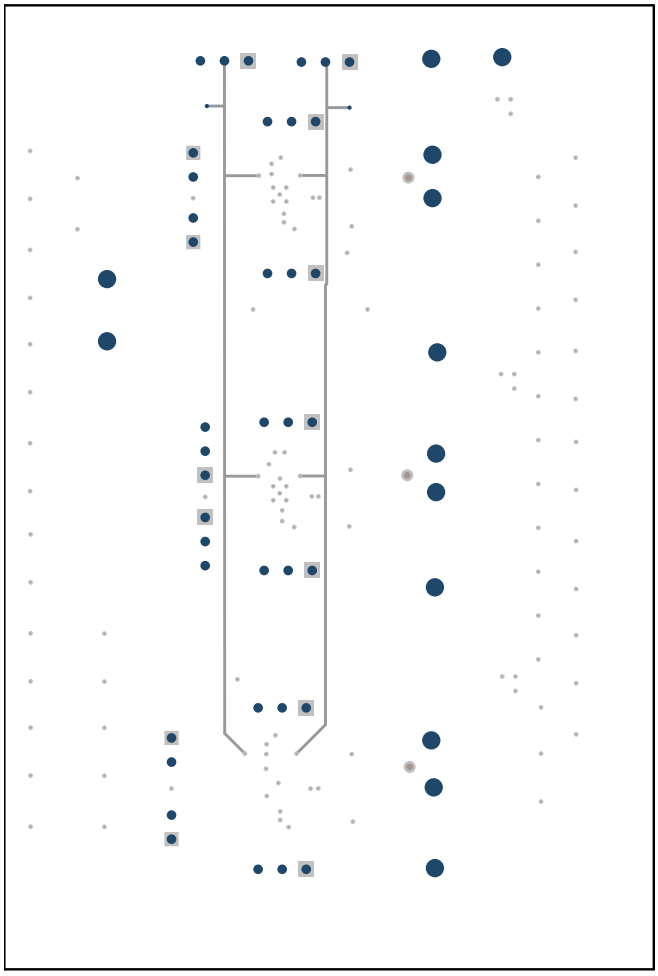


Figure 11. Signal Layer

3 EVM Test Points, Jumpers, and Connectors

This section describes the test points, jumpers, and connectors on the EVM as well as how to connect, set up, and properly use the EVM. Each device has independent signal connections, but all devices have a common VCC and ground.

3.1 EVM Test Points

Table 3 lists the test points and functional descriptions. All pins of the device are broken out to test points on the EVM.

Table 3. Test Points

Test Point	Test Point Silkscreen Label	Function	Description
TP1	ENBA	Enable driver A	Internally pulled up, can be disabled when input is low
TP2	ENBB	Enable driver B	Internally pulled up, can be disabled when input is low
TP3	VCC	Power supply	Power supply for the device
TP4	FET_VDD	Power supply	Power supply for MOSFET
TP5, TP8, TP13-15	GND	Ground	Connected with ground
TP6, TP9, TP11	FET_OUTA	MOSFET drain	Connected with MOSFET drain
TP7, TP10, TP12	FET_OUTB	MOSFET drain	Connected with MOSFET drain

3.2 EVM Jumpers

Table 4 lists the jumpers on the UCC27423-4-5-Q1 EVM. As ordered, the EVM will have two jumpers installed.

Table 4. List of Onboard Jumpers

Jumper	Device	Default Connection	Description
J7	All	ENBA to GND	Connect ENBA to GND to disable OUTA. Otherwise, connect ENBA to VCC or leave it floating.
J8	All	ENBB to GND	Connect ENBB to GND to disable OUTB. Otherwise, connect ENBB to VCC or leave it floating.

3.3 EVM Input/Output Connectors

Table 5 lists the following 2-pin headers that are input/output connecters for each device.

Table 5. List of Input/Output Connectors

Jumper	Part Number	Description
J3	UCC27423-Q1	INA device input (pin 2) and GND (pin 1)
J4		INB device input (pin 2) and GND (pin 1)
J11		OUTA device output (pin 1) and GND (pin 2 and pin 3)
J12		OUTB device output (pin 1) and GND (pin 2 and pin 3)
J9	UCC27424-Q1	INA device input (pin 1) and GND (pin 2 and pin 3)
J10		INB device input (pin 1) and GND (pin 2 and pin 3)
J15		OUTA device output (pin 1) and GND (pin 2 and pin 3)
J17		OUTB device output (pin 1) and GND (pin 2 and pin 3)
J13	UCC27425-Q1	INA device input (pin 2) and GND (pin 1)
J14		INB device input (pin 2) and GND (pin 1)
J16		OUTA device output (pin 1) and GND (pin 2 and pin 3)
J18		OUTB device output (pin 1) and GND (pin 2 and pin 3)

4 EVM Setup and Operation

This section describes the functionality and operation of the UCC27423-4-5-Q1 EVM. For the electrical characteristics of the device, refer to *UCC2742x-Q1 Dual 4-A High-Speed Low-Side MOSFET Drivers With Enable*.

4.1 Test Equipment

The test equipment includes:

DC Power Supply — DC power supply capable of providing at least 4 V

Signal Generator — Digital signal generator capable of producing at least one single ended CMOS type signal for PWM input (ENB input optional)

Oscilloscope — Oscilloscope with at least four channels of analog type capable of 100-MHz bandwidth with high-impedance scope probes capable of handling 50 V

Voltmeter — Digital voltmeter capable of monitoring input DC voltages, or other nodes around the EVM (the voltmeter can be omitted if the DC power supply monitors its own voltage and current levels)

Output Load — External output load such as a 1.8-nF capacitor

4.2 Recommended Test Setup and Operating Conditions

Figure 12 shows the EVM test setup. Table 6 lists the recommended operating conditions. The default connection of the enable pins is connected to ground.

NOTE: Remove all jumpers when testing the EVM.

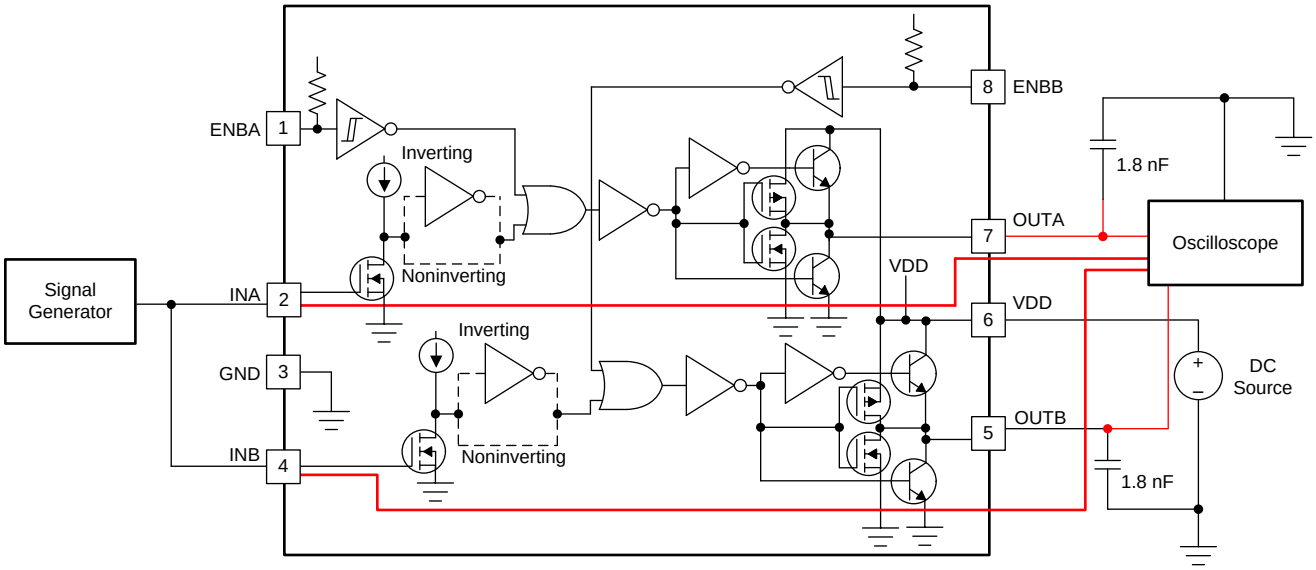


Figure 12. Recommended Test Setup

Table 6. Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
VDD	Supply voltage	4	15	V
INA	Input voltage	–2	15	V
INB				
ENA	Enable voltage	0	15	V
ENB				
T_J	Operating junction temperature	–40	125	℃

4.3 EVM Setup With FETs

4.3.1 Test Preparation

The UCC27423-4-5-Q1 EVM board has no installed FETs or peripheral components. To test the EVM with FETs, the user must install the FETs themself.

Figure 13 shows the FETs and peripheral components to be installed inside the red outlines. For detailed descriptions of each of the components, see Table 2.

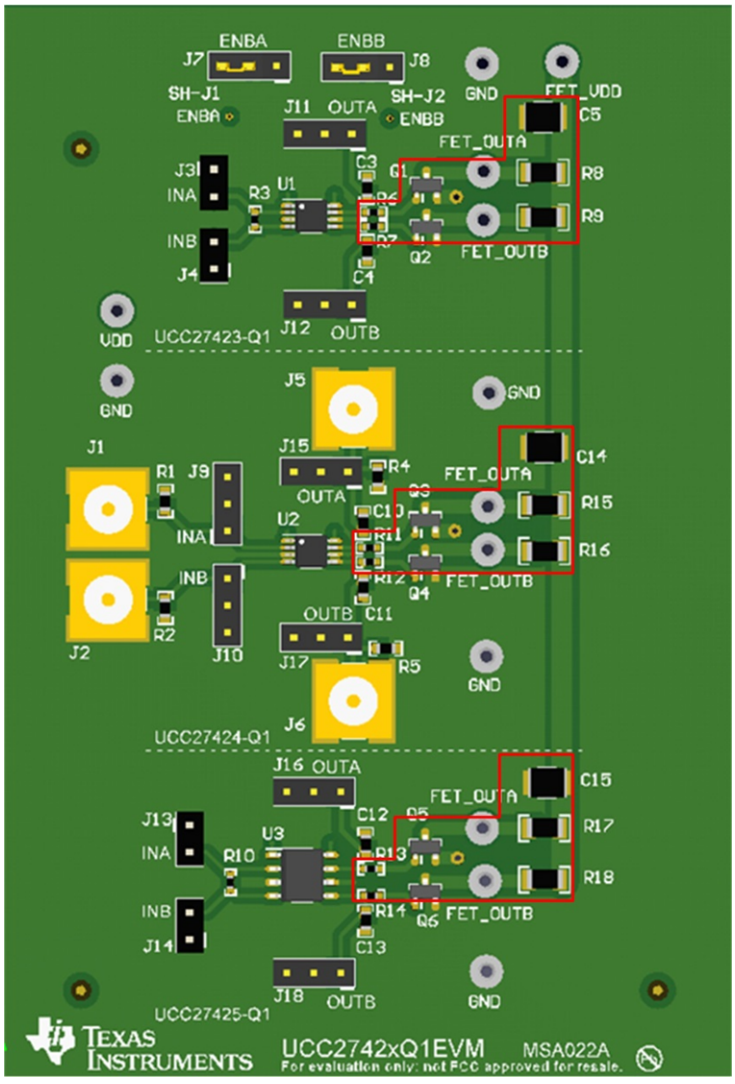


Figure 13. EVM installation With FETs

4.3.2 Power-Up Procedure

To power the EVM, follow these steps:

Step 1. Power the board with 5 V through VDD, and set the current limit below 1 A.

Step 2. Place a 5-V power supply between FET_VDD and GND, and set the current limit below 1 A.

Step 3. Connect the signal generator outputs to INA and INB and adjust the signal generator to produce a signal between 2.75 V and 5.5 V at desired frequency and duty cycle.

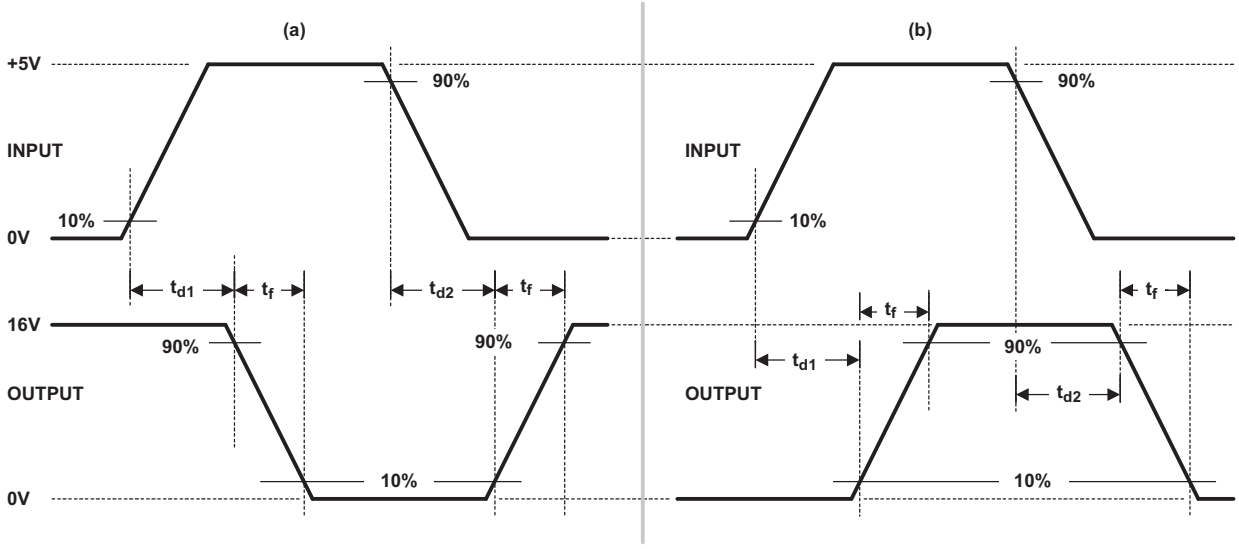
Step 4. Remove the jumpers on J7 and J8.

Step 5. Use FET_OUTA and FET_OUTB with a scope to capture desired waveforms.

5 Performance Data, Test Verfication Waveforms, and Typical Characteristic Curves

5.1 Propagation Delay, Rise and Fall Times

Figure 14 shows the propagation delay, rise and fall times as measured on the EVM. Figure 14 also shows the switching waveforms for inverting driver (a) and noninverting driver (b).



The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 14. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver

5.2 Propagation Delay, Rise, and Fall Times Results

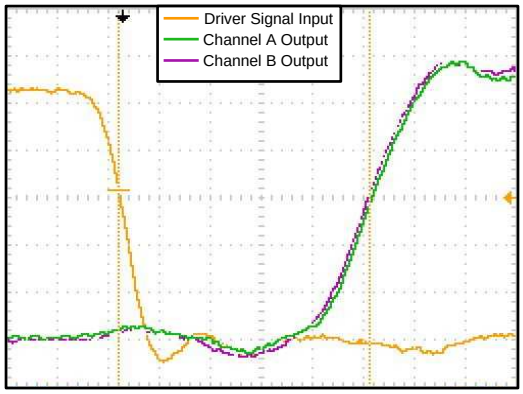
The load capacitance testing condition is 1.8 nF, VDD = 5 V, and the driver signal voltage is set to 5 V with f = 300 kHz, connected to INA and INB. Table 7 lists the EVM test results.

Table 7. EVM Test Results

Part Number	Delay Time, IN Rising (IN to OUT)	Delay Time, IN Falling (IN to OUT)	Rise Time	Fall Time
UCC27423-Q1	27 ns	49 ns	21 ns	16 ns
UCC27424-Q1	40 ns	34 ns	19 ns	17 ns
UCC27425-Q1	41 ns	51 ns	17 ns	16 ns

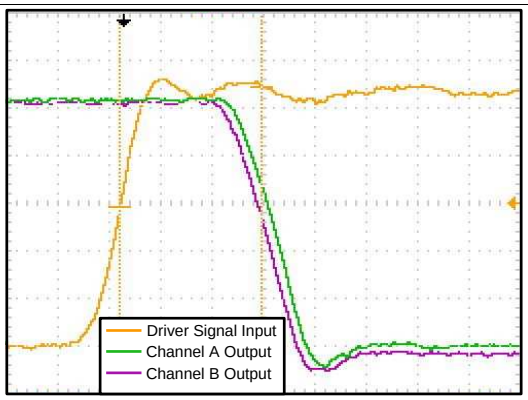
5.3 Typical Characteristic Curves

Figure 15 through Figure 20 show the propagation delay, rise time, and fall time measurements on the EVM.



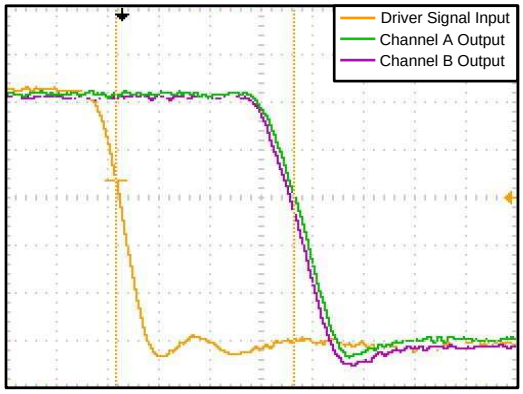
Time 10 ns/div, Amplitude 1 V/div

Figure 15. UCC27423-Q1 Input Falling



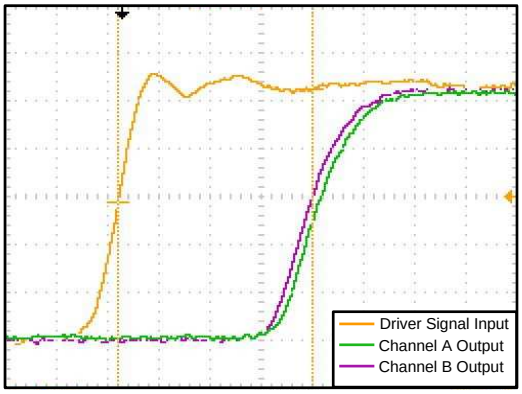
Time 10 ns/div, Amplitude 1 V/div

Figure 16. UCC27423-Q1 Input Rising



Time 10 ns/div, Amplitude 1 V/div

Figure 17. UCC27424-Q1 Input Falling

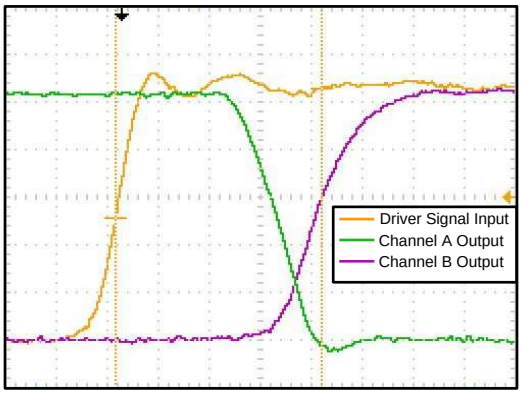


Time 10 ns/div, Amplitude 1 V/div

Figure 18. UCC27424-Q1 Input Rising

Time 10 ns/div, Amplitude 1 V/div

Figure 19. UCC27425-Q1 Input Falling



Time 10 ns/div, Amplitude 1 V/div

Figure 20. UCC27425-Q1 Input Rising

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2017) to A Revision	Page
• Added the *EVM Compatible Devices* table	2

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