*User's Guide*

# *TPS56339 Step-Down Converter Evaluation Module User's Guide*


**ABSTRACT**

This user's guide contains background information for the TPS56339 as well as support documentation for the TPS56339EVM evaluation module. Included are the performance specifications, the schematic, and the list of materials for the TPS56339EVM.


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## Trademarks

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# 1 Introduction

The TPS56339 is a single, Advanced Emulated Current Mode (AECM) control, synchronous Buck DC/DC converter, being able to deliver 3-A continuous output current, providing an advance Eco-mode to maintain high light load efficiency. The TPS56339 integrates 26-V capable MOSFETs which is suitable for applications working from 19-V bus power lines. The device implements an AECM control which can get fast transient response with fixed frequency. The fast transient response results in low voltage drop and the fixed frequency brings a better jitter permanence and predictable frequency for EMI design. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design over a wide voltage output range.Table 1-1 shows the rated input voltage and output current ranges for the evaluation module.

The TPS56339EVM is a single, synchronous buck converter providing 5 V at 3 A from 5.5 V to 24 V input. This user's guide describes the TPS56339EVM performance.

**Table 1-1. Input Voltage and Output Current Summary**

| EVM | Input Voltage Range | Output Current Range |
|---|---|---|
| TPS56339EVM | $V_{IN}$ = 5.5V to 24 V | 0 A to 3 A |

## 2 Performance Specification Summary

A summary of the TPS56339EVM performance specifications is provided in Table 2-1. Specifications are given for an input voltage of $V_{IN}$ = 19 V and an output voltage of 5.0 V, unless otherwise specified. The TPS56339EVM is designed and tested for $V_{IN}$ = 5.5 V to 24 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

**Table 2-1. TPS56339EVM Performance Specification Summary**

| Specification | Test Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Input voltage range | | 5.5 | 19 | 24 | V |
| $V_{START}$ Input start voltage | | | 6.6 | | V |
| $V_{STOP}$ Input stop voltage | | | 5.7 | | V |
| Output voltage set point | | | 5 | | V |
| Output current range | $V_{IN}$ = 6 V to 24 V | 0 | | 3 | A |
| Line regulation | $I_O$ = 3 A | | ±0.5% | | |
| Load regulation | $V_{IN}$ = 19 V | | ±0.5% | | |
| Output ripple voltage | $V_{IN}$ = 19 V, $I_O$ = 3 A | | <30 | | $mV_{PP}$ |
| Center operating frequency | | | 500 | | kHz |
| Maximum Efficiency | $V_{IN}$ = 19 V, $I_O$ = 3A | | 94.0% | | |

# 3 Modifications

These evaluation modules are designed to provide access to the features of the TPS56339. Some modifications can be made to this module.

## 3.1 Output Voltage Set Point

The voltage divider, R6 and R7, is used to set the output voltage. To change the output voltage of the EVM, it is necessary to change the value of resistor R6. Changing the value of R6 can change the output voltage above 0.8 V. The value of R6 for a specific output voltage can be calculated using Equation 1. Use 10 kΩ for R7.

$$R_6 = \left(\frac{V_{OUT}}{0.8} - 1\right) \cdot R_7 \tag{1}$$

Table 3-1 lists the R6 and R7 values for some common output voltages. Note that $V_{IN}$ must be in a range so that the minimum on-time is greater than 55 ns. The values in Table 3-1 are standard values, not the exact value calculated using Equation 1.

Be noted that the voltage rate of the output capacitors is only 16 VDC, higher voltage rate capacitors should be used when the configured output voltage is equal or higher than 12V.

**Table 3-1. Recommended Component Values**

| OUTPUT VOLTAGE(1) (V) | R6(2) (kΩ) | R7 (kΩ) | L1(3) (µH) | $C_{OUT}$ (4) (µF) | Range of $L1 \cdot C_{OUT\_E}$ (5) (µH×µF) |
|---|---|---|---|---|---|
| 1.05 | 3.16 | 10.0 | 1.5 | 2×22 | 48 to 188 |
| 1.8 | 12.4 | 10.0 | 2.2 | 2×22 | 64 to 250 |
| 2.5 | 21.5 | 10.0 | 3.3 | 2×22 | 87 to 334 |
| 3.3 | 31.6 | 10.0 | 4.7 | 2×22 | 107 to 404 |
| 5 | 52.3 | 10.0 | 5.6 | 2×22 | 93 to 334 |
| 12 | 140 | 10.0 | 6.8 | 3×22 | 45 to 137 |

(1) Please use the recommended L1 and $C_{OUT}$ combination of the higher and closest output rail for the unlisted output rails.
(2) R6 = 0 Ω for $V_{OUT}$ = 0.8 V.
(3) Inductance values are calculated based on $V_{IN}$ = 19 V, but they can also be used for other input voltages. User can calculate their preferred inductance value per TPS56339 datasheet.
(4) The $C_{OUT}$ is the sum of nominal output capacitance. Two 22-uF, 0805, 16VDC capacitors are recommended for $V_{OUT} \leq$ 5V, three 22-uF, 0805, 25VDC capacitors are recommended for $V_{OUT}$ > 5V.
(5) The $C_{OUT\_E}$ is the effective value after derating, the value of $L1 \cdot C_{OUT\_E}$ should be within in the range.

## 3.2 Adjustable UVLO

The under voltage lock out (UVLO) can be adjusted externally using R1 and R2. The EVM is set for a start voltage of 6.6 V and a stop voltage of 5.7 V using R1 = 174 kΩ and R2 = 36.5 kΩ. Use Equation 2 and Equation 3 to calculate required resistor values for different start and stop voltages. For higher light-load efficiency, consider choosing a larger R1 and R2. Make adjustments to $V_{start}$ or $V_{stop}$ for a proper R1. Once R1, R2 settled down, the $V_{EN}$ voltage need to be calculated by Equation 4 to make sure that it is lower than 5.5V with max $V_{IN}$, max $I_p$ and max $I_h$.

$$R_1 = \frac{V_{SATART}\frac{V_{EN\_FALL}}{V_{EN\_RISE}} - V_{STOP}}{I_p\left(1 - \frac{V_{EN\_FALL}}{V_{EN\_RISE}}\right) + I_h} \tag{2}$$

$$R_2 = \frac{R_1 \cdot V_{EN\_FALL}}{V_{STOP} - V_{EN\_FALL} + R_1 \cdot \left(I_p + I_h\right)} \tag{3}$$

$$V_{EN} = \frac{R_2 \cdot V_{IN} + R_1 R_2 \left(I_p + I_h\right)}{R_1 + R_2} \tag{4}$$

where

- $I_p$ = 1.2 µA
- $I_h$ = 3.1 µA
- $V_{ENfalling}$ = 1.12 V
- $V_{ENrising}$ = 1.18 V

# 4 EVM Photos

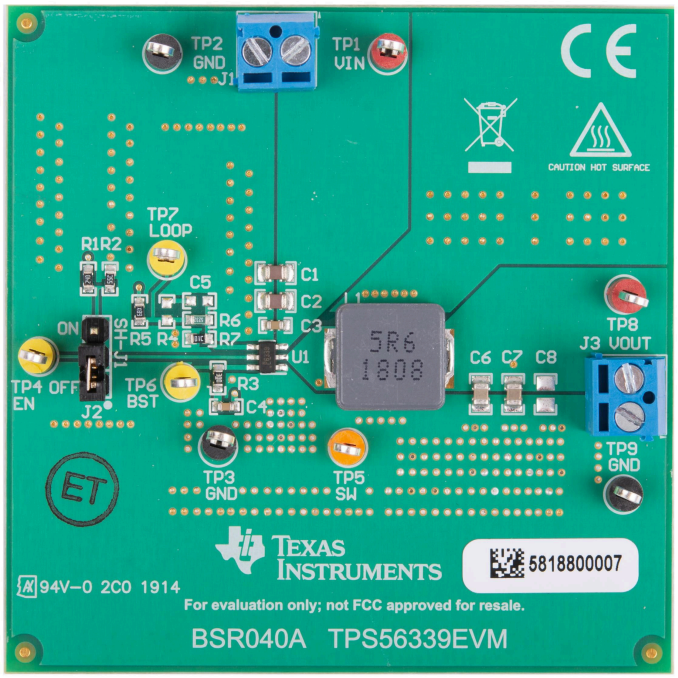


**Figure 4-1. TPS56339EVM Front Photo**

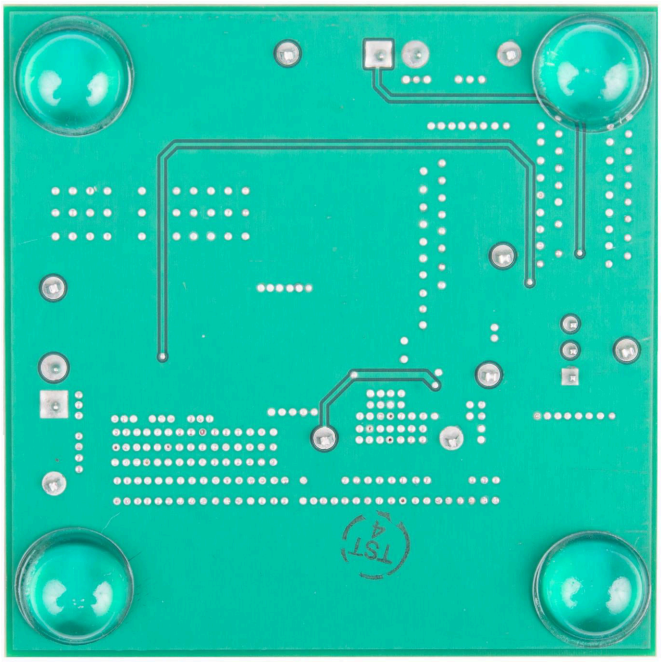

**Figure 4-2. TPS56339EVM Back Photo**

# 5 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS56339EVM evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, output line regulation, load transient response, output ripple, input ripple, start-up, output short and thermal performance. All the data and waveforms are tested under $V_{IN}$ = 19 V unless otherwise stated.

## 5.1 Input/Output Connections

The TPS56339EVM is provided with input/output connectors and test points as shown in Table 5-1. A power supply capable of supplying 3 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J3 through a pair of 20-AWG wires. The maximum load current capability must be at least 3 A to use the full capability of this EVM. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the $V_{IN}$ input voltages with TP2 providing a convenient ground reference. TP8 is used to monitor the output voltage with TP9 as the ground reference.

**Table 5-1. EVM Connectors and Test Points**

| Reference Designator | Function |
|---|---|
| J1 | VIN (see Table 1-1 for $V_{IN}$ range) |
| J3 | VOUT, 5 V at 3 A maximum |
| J2 | 3-pin header for enable. Connect Pin2 to Pin1 to disable, Connect Pin2 to Pin3 to enable by resistor network, open to enable by EN floating. |
| TP1 | $V_{IN}$ test point at VIN connector |
| TP2 | GND test point at VIN connector |
| TP3 | GND test point |
| TP4 | EN test point |
| TP5 | SW test point |
| TP6 | Boot test point |
| TP7 | Test point between voltage divider network and output. Used for loop response measurements. |
| TP8 | Output voltage test point at VOUT connector |
| TP9 | GND test point at VOUT connector |

## 5.2 Start-Up Procedure

1. Ensure that the jumper at J2 (Enable control) pins 1 and 2 are covered to shunt EN to GND, disabling the output.

2. Apply appropriate VIN voltage to VIN (J1-1) and GND (J1-2).

3. Move the jumper at J2 (Enable control) away from pins 1 and 2 (EN and GND) or move the jumper at J2 from pin 1 and pin 2 to pin 2 and pin3 to enable the output.

## 5.3 Efficiency

The efficiency of this EVM peaks at a load current of about 0.5 A – 1 A, and then decreases as the load current increases towards full load. Figure 5-1 shows the efficiency for the TPS56339EVM at an ambient temperature of 25 °C. Figure 5-2 shows the efficiency for the TPS56339EVM on a semi-log scale to better show light load efficiency.

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

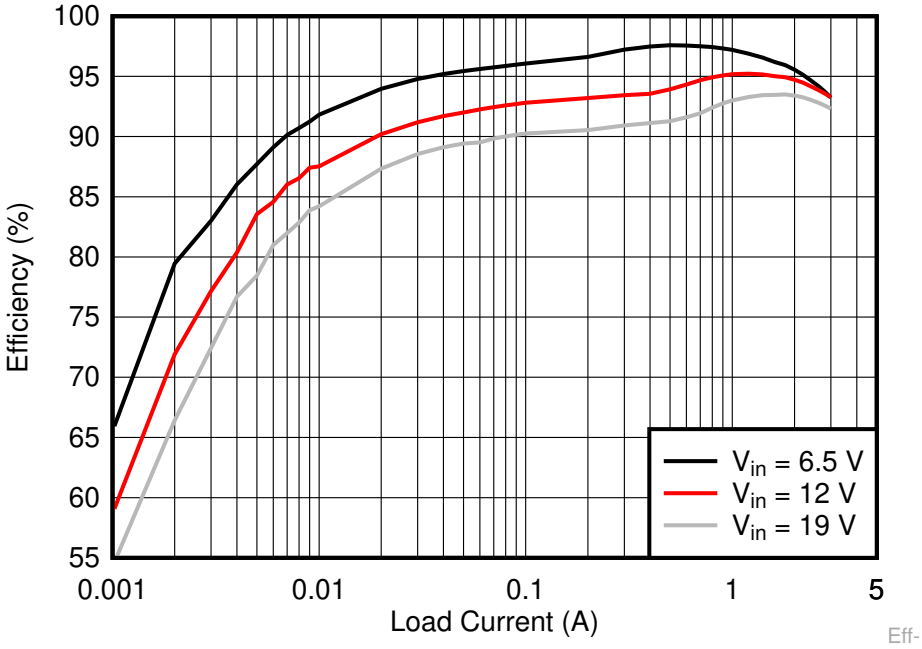


**Figure 5-1. TPS56339EVM Efficiency**

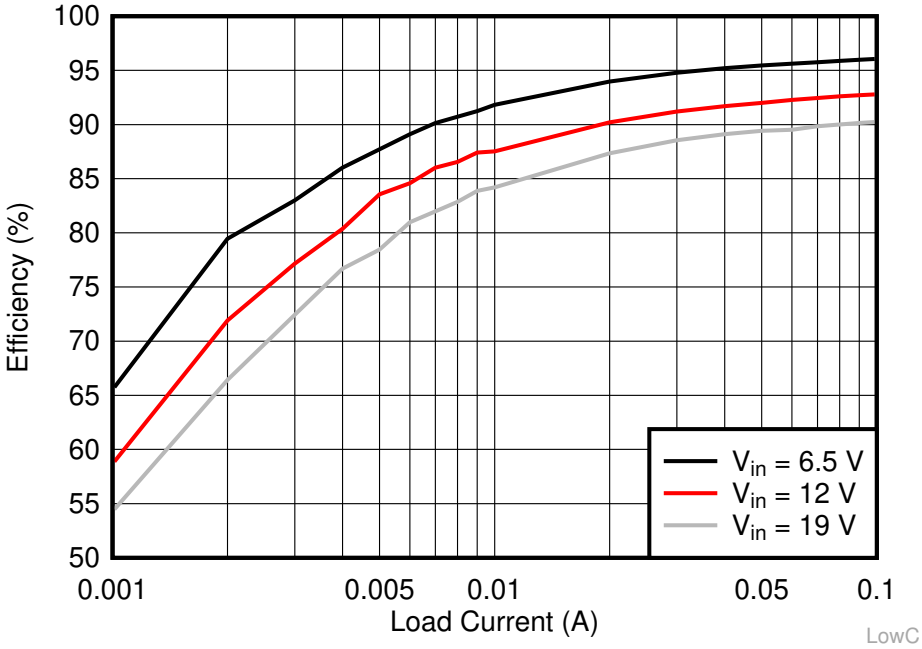


**Figure 5-2. TPS56339EVM Low Current Efficiency**

## 5.4 Output Voltage Load Regulation

Figure 5-3 shows the load regulation for the TPS56339EVM. Measurements are given for an ambient temperature of 25 °C.

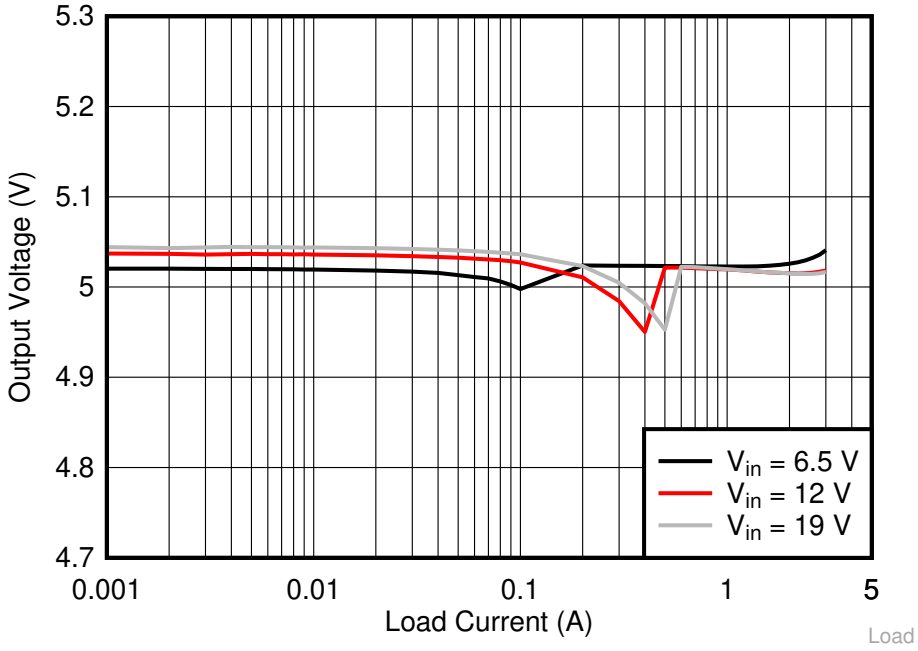


**Figure 5-3. TPS56339EVM Load Regulation**

## 5.5 Output Voltage Line Regulation

Figure 5-4 shows the line regulation for the TPS56339EVM.

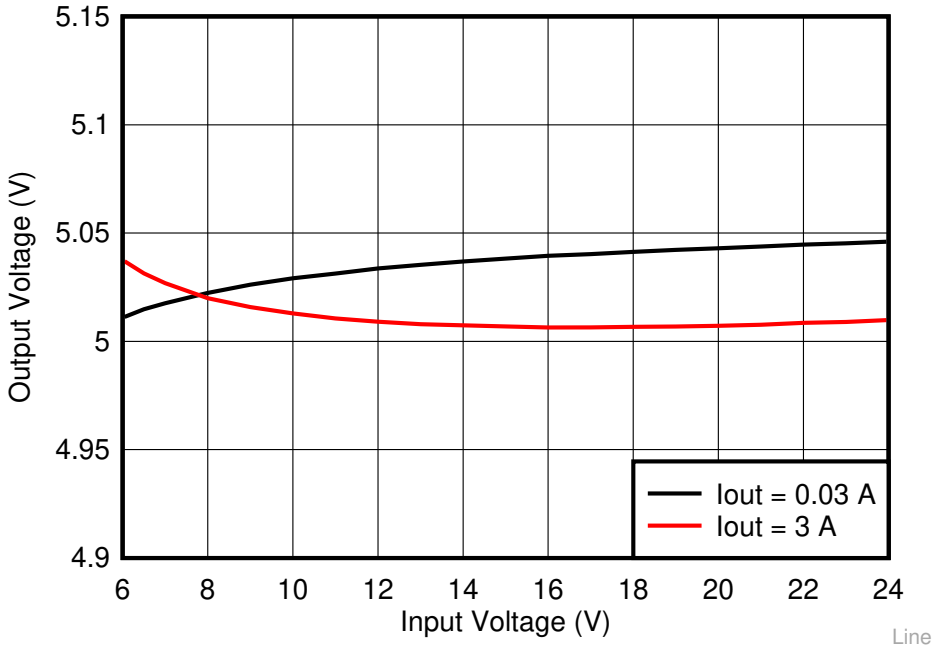


**Figure 5-4. TPS56339EVM Line Regulation**

## 5.6 Load Transients

Figure 5-5 and Figure 5-6 show the TPS56339EVM response to load transients. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

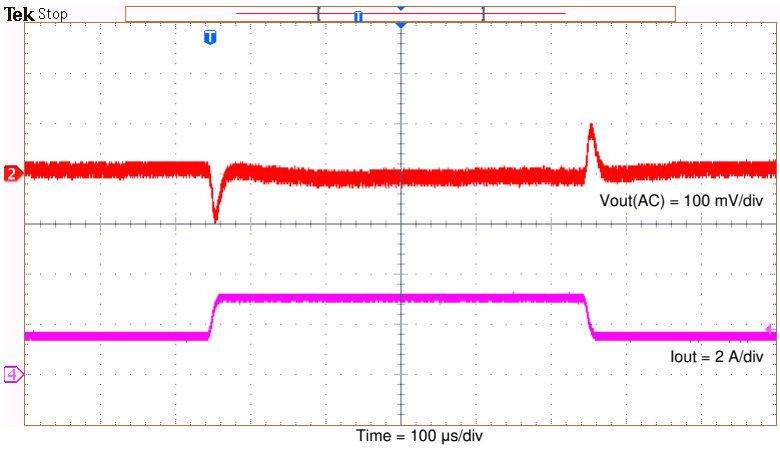


**Figure 5-5. TPS56339EVM Transient Response 1.5 to 3 A**

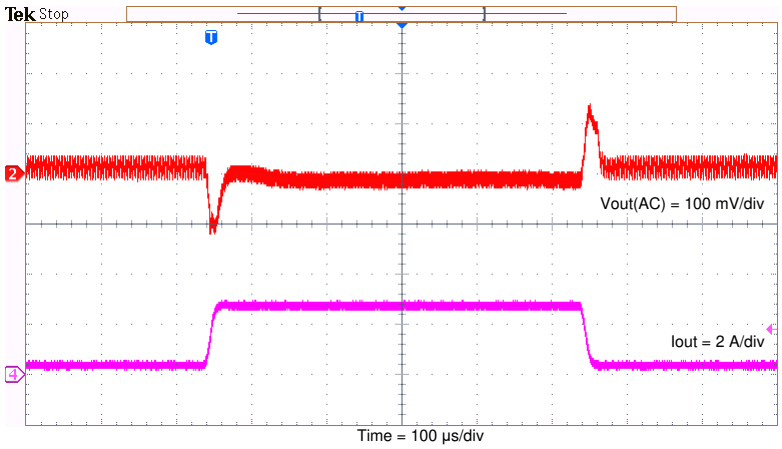


**Figure 5-6. TPS56339EVM Transient Response 0.3 to 2.7 A**

## 5.7 Voltage Ripple

Figure 5-7, Figure 5-8 and Figure 5-9 show the TPS56339EVM output voltage ripple for full-load, skip-mode, light-load and no-load operation. $V_{IN}$ = 19 V. The output The ripple voltage is measured directly across the output capacitors.

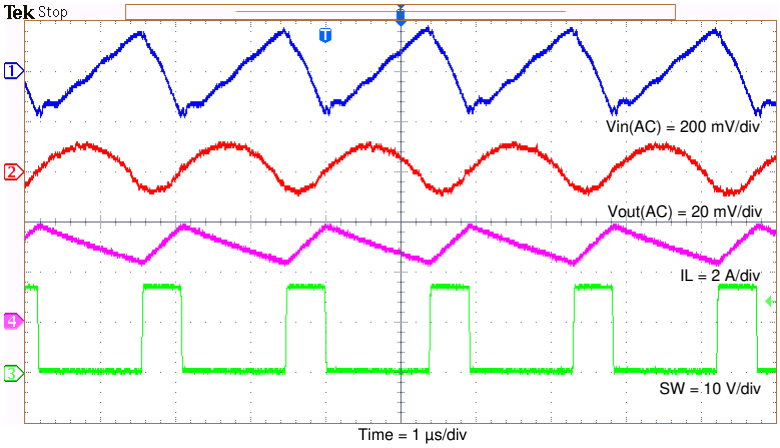


**Figure 5-7. TPS56339EVM Output Ripple, $I_{OUT}$ = 3 A**

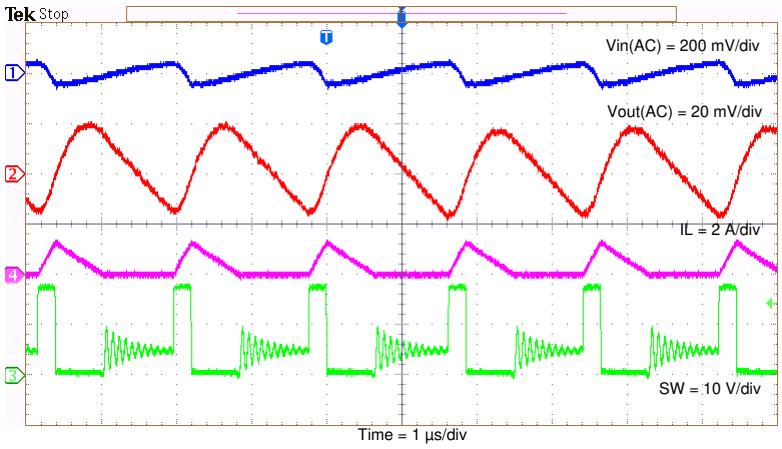


**Figure 5-8. TPS56339EVM Output Ripple, $I_{OUT}$ = 0.3 A**

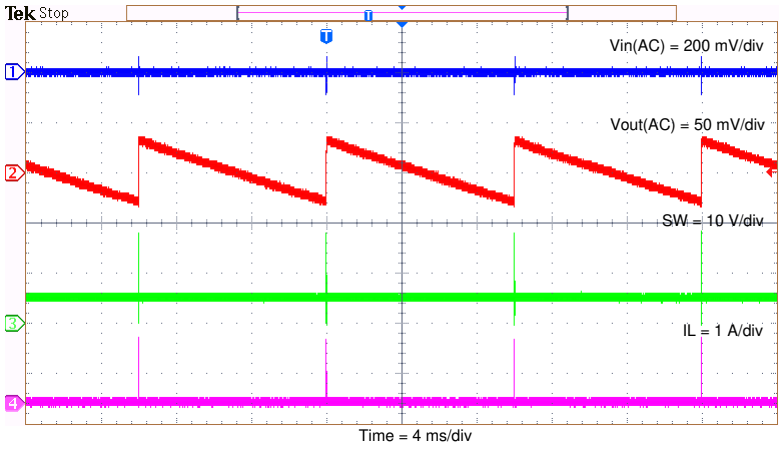


**Figure 5-9. TPS56339EVM Output Ripple, $I_{OUT}$ = 0 A**

## 5.8 Powering Up

Figure 5-10 and Figure 5-11 show the start-up waveforms for the TPS56339EVM. In Figure 5-10, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1 and R2 resistor divider network. In Figure 5-11, the input voltage is initially applied and the output is inhibited by using a 3.3-V logic signal between EN and GND. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 5 V. The input voltage for these plots is 19 V and the load current is 3 A.

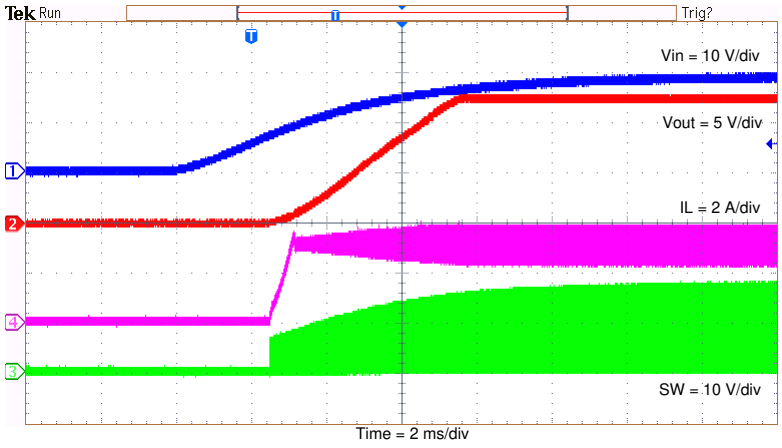


**Figure 5-10. TPS56339EVM Startup Relative to $V_{IN}$**

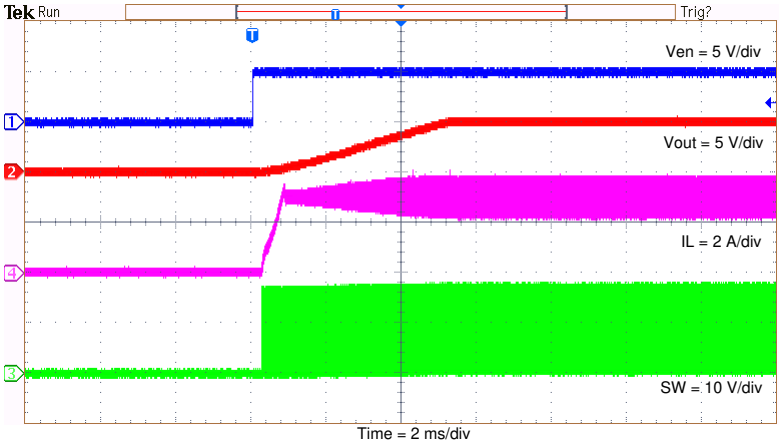


**Figure 5-11. TPS56339EVM Startup Relative to Enable**

## 5.9 Powering Down

Figure 5-12 and Figure 5-13 show the start-up waveforms for the TPS56339EVM. In Figure 5-12, the output voltage ramps down as soon as the input voltage falls below the UVLO stop threshold as set by the R1 and R2 resistor divider network. In Figure 5-13, the output is inhibited by using a 5-V logic signal between EN and GND. The input voltage for these plots is 19 V and the load current is 3 A.

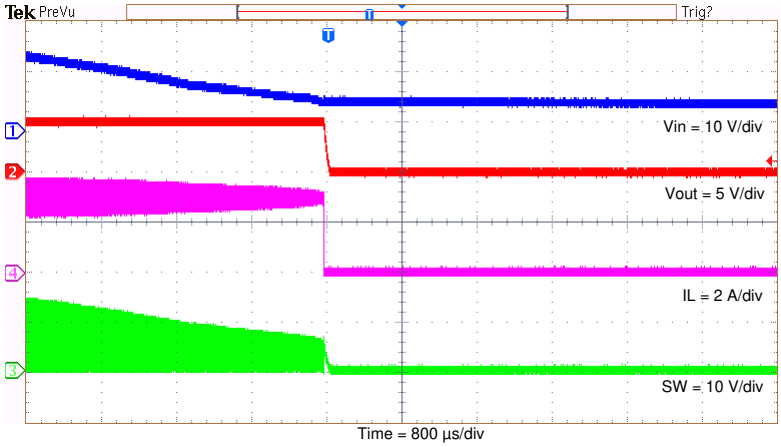


**Figure 5-12. TPS56339EVM Shutdown Relative to $V_{IN}$**

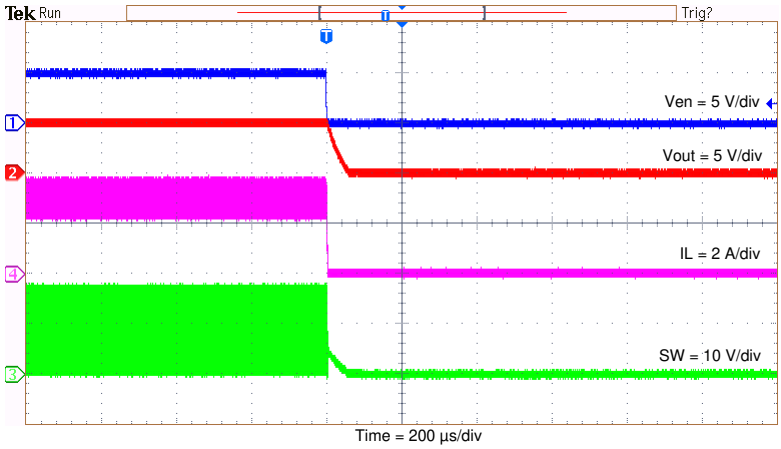


**Figure 5-13. TPS56339EVM Shutdown Relative to EN**

## 5.10 Output Short Protection and Recovery

Figure 5-14 and Figure 5-15 show the waveforms of output short protection and recovery.

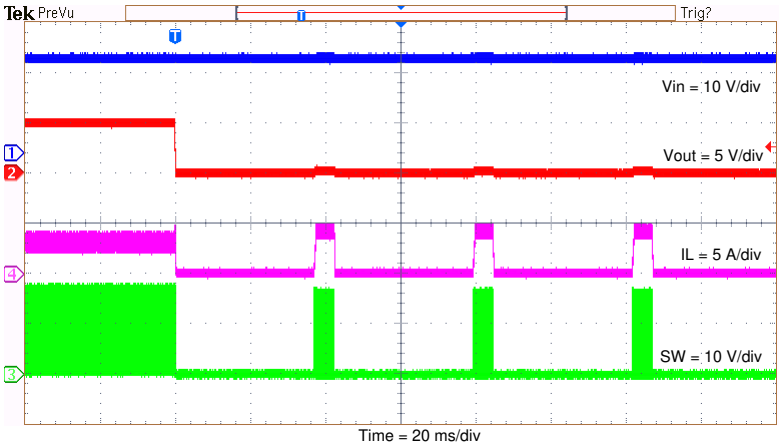


**Figure 5-14. TPS56339EVM Short Protection**

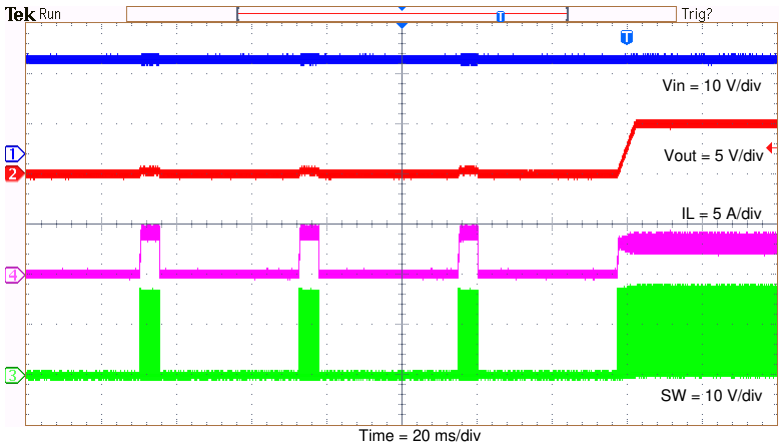


**Figure 5-15. TPS56339EVM Short Recovery**

## 5.11 Thermal Performance

Figure 5-16 shows the thermal performance of the TPS56339EVM under $V_{IN}$ = 19 V, $V_{OUT}$ = 5 V, $I_{OUT}$ = 3 A.

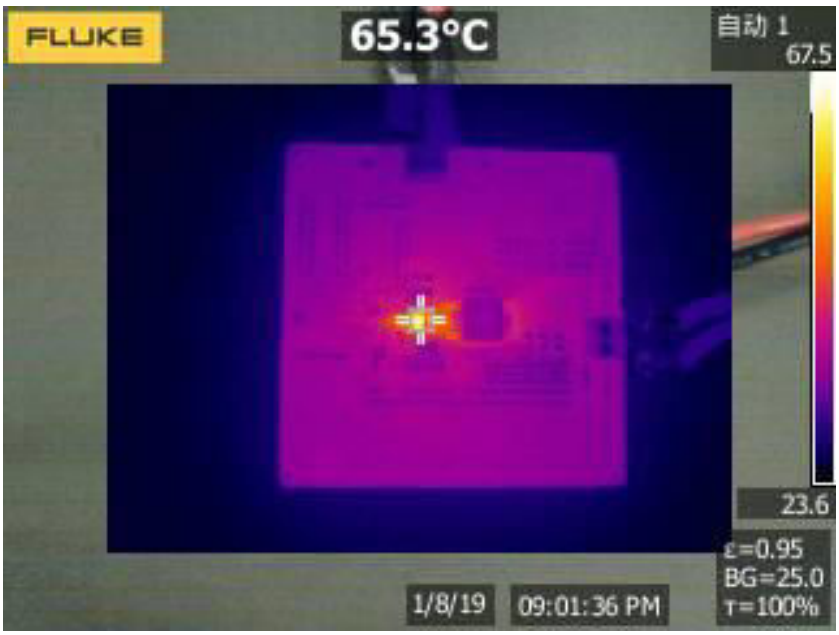


**Figure 5-16. TPS56339EVM Thermal Performance**

# 6 Board Layout

This section provides a description of the TPS56339EVM, board layout, and layer illustrations.

## 6.1 Layout

Figure 6-1 , Figure 6-2 and Figure 6-3 show the board layout for the TPS56339EVM. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for $V_{IN}$, $V_{OUT}$, and SW. Also on the top layer are connections for the remaining pins of the TPS56339 and a large area filled with ground. To facilitate the placement of the main input bypass capacitor as close to the $V_{IN}$ and GND pins as possible. The input decoupling capacitors (C2, and C3) and bootstrap capacitor (C4) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. For the TPS56339, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply.

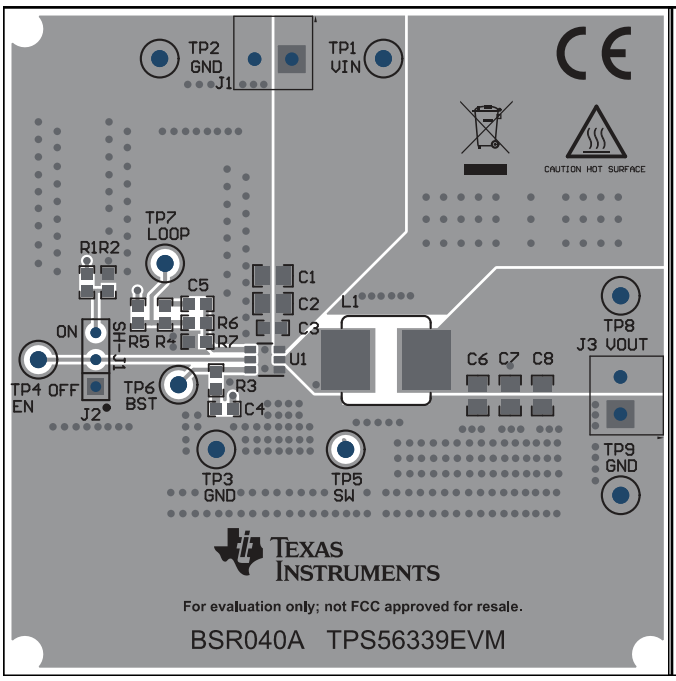


**Figure 6-1. Top Assembly**

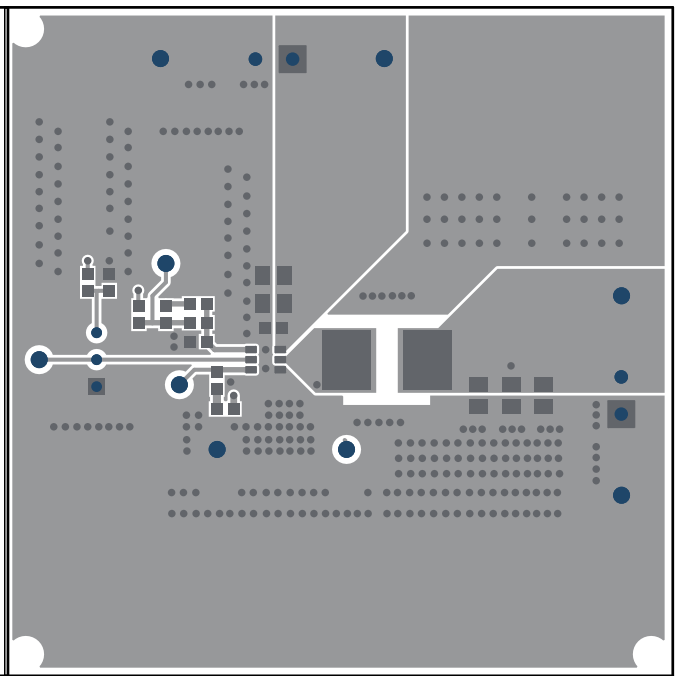

**Figure 6-2. Top Layer**

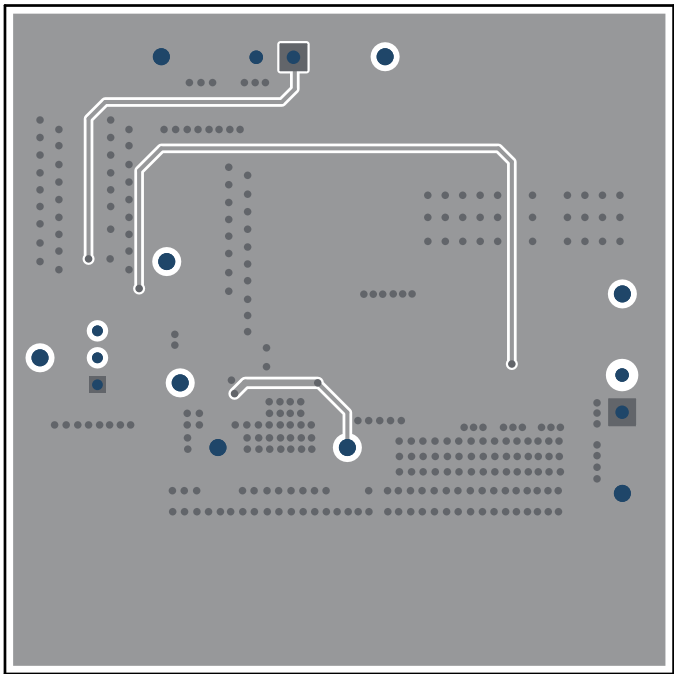

**Figure 6-3. Bottom Layer**

# 7 Schematic and List of Materials

This section presents the TPS56339EVM schematic and list of materials.

## 7.1 Schematic

Figure 7-1 is the schematic for the TPS56339EVM.

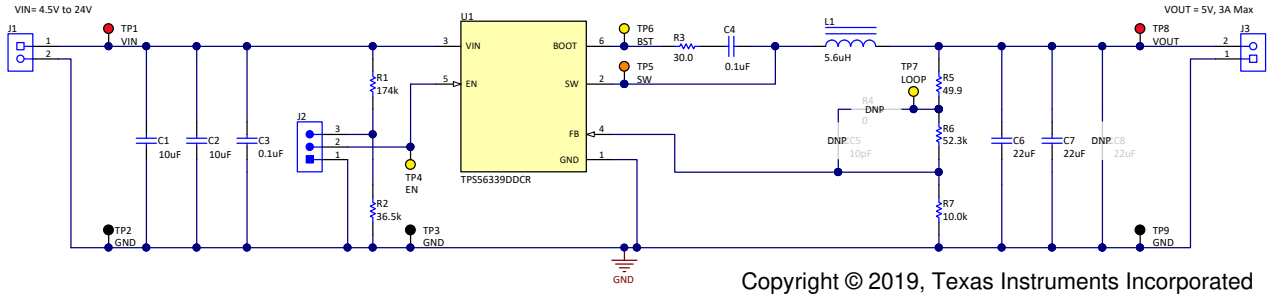




**Figure 7-1. TPS56339EVM Schematic**

## 7.2 List of Materials

Table 7-1 presents the list of materials for the TPS56339EVM.

**Table 7-1. TPS56339EVM List of Materials**

| Designator | Qty | Value | Description | Package Reference | Part Number | Manufacturer | Alternate PartNumber | Alternate Manufacturer |
|---|---|---|---|---|---|---|---|---|
| C1, C2 | 2 | 10uF | CAP, CERM, 10 uF, 35 V, +/- 10%, X5R, 0805 | 0805 | GRM21BR6YA106KE43L | Murata | | |
| C3, C4 | 2 | 0.1uF | CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603 | 0603 | 885012206095 | Murata | | |
| C6, C7 | 2 | 22uF | CAP, CERM, 22 uF, 16 V, +/- 20%, X5R, 0805 | 0805 | GRM21BR61C226ME44 | Murata | | |
| J1, J3 | 2 | | Terminal Block, 3.5mm Pitch, 2x1, TH | 7.0x8.2x6.5mm | ED555/2DS | On-Shore Technology | | |
| J2 | 1 | | Header, 100mil, 3x1, Tin, TH | Header, 3 PIN, 100mil, Tin | PEC03SAAN | Sullins Connector Solutions | | |
| L1 | 1 | 5.6uH | Inductor, Shielded, Powdered Iron, 5.6 uH, 7.4 A, 0.0268 ohm, SMD | 322x158x322mil | SRP1038A-5R6M | Vishay-Dale | SRP1038A-5R6M | Bourns |
| R1 | 1 | 174k | RES, 174 k, 0.1%, 0.1 W, 0603 | 0603 | RT0603BRD07174KL | Yageo America | | |
| R2 | 1 | 36.5k | RES, 36.5 k, 0.1%, 0.1 W, 0603 | 0603 | 'RT0603BRD0736K5L | Yageo America | | |
| R3 | 1 | 30.0 | RES, 30.0, 1%, 0.1 W, 0603 | 0603 | RC0603FR-0730RL | Panasonic | | |
| R5 | 1 | 49.9 | RES, 49.9, 0.5%, 0.1 W, 0603 | 0603 | RT0603DRE0749R9L | Yageo America | | |
| R6 | 1 | 52.3k | RES, 52.3 k, 0.1%, 0.1 W, 0603 | 0603 | 'RT0603BRD0752K3L | Susumu Co Ltd | | |
| R7 | 1 | 10.0k | RES, 10.0 k, 0.1%, 0.1 W, 0603 | 0603 | 'RT0603BRD0710KL | Yageo America | | |
| SH-JP1 | 1 | 1x2 | Shunt, 100mil, Gold plated, Black | Shunt | 969102-0000-DA | 3M | | |
| TP1, TP8 | 2 | | Test Point, Multipurpose, Red, TH | Red Multipurpose Testpoint | 5010 | Keystone | | |
| TP2, TP3, TP9 | 3 | | Test Point, Multipurpose, Black, TH | Black Multipurpose Testpoint | 5011 | Keystone | | |
| TP4, TP6, TP7 | 3 | | Test Point, Multipurpose, Yellow, TH | Yellow Multipurpose Testpoint | 5014 | Keystone | | |
| TP5 | 1 | | Test Point, Multipurpose, Orange, TH | Orange Multipurpose Testpoint | 5013 | Keystone | | |
| U1 | 1 | | 4.5V to 24 V Input, 3-A Synchronous Step-Down Voltage Regulator, DDC0006A | DDC0006A | TPS56339DDCR | Texas Instruments | TPS56339DDCT | Texas Instruments |

# 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (May 2019) to Revision C (July 2021) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document. | 3 |
| • Updated user's guide title | 3 |

| Changes from Revision A (November 2018 May 2019) to Revision B () | Page |
|---|---|
| • Added Figure 4-1 TPS56339EVM front and back images | 7 |

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