User's Guide

Powering DRA821 with TPS6594-Q1 and LP8764-Q1

ABSTRACT

This user's guide can be used as a guide for integrating the TPS6594-Q1 and LP8764-Q1 power management integrated circuits (PMICs) into a system powering the DRA821 processor.

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1 Introduction

This user's guide defines the power distribution network (PDN) between the TPS6594-Q1 and LP8764-Q1 devices and the DRA821 processor. This document describes the platform power resource connections, digital control connections, and PMIC sequencing settings to support the different processor state transitions. The PMIC default non-volatile memory (NVM) settings, internal state transitions, and power sequences are also defined in this document. This user's guide does not provide information about the electrical characteristics, external components, package, or the functionality of the PMICs or processor. For such information and the full register maps, refer to the data sheet for each device. In the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material, the data sheet specification is the definitive source.

2 Device Versions

There are different versions of the TPS6594-Q1 and LP8764-Q1 devices available with unique NVM settings to support different processor solutions. The unique NVM settings for each PMIC device are optimized per PDN design to support different processors, processing loads, SDRAM types, system functional safety levels, and end product features - such as low power modes, processor interface levels, SD Card, and so forth. The NVM settings can be distinguished using the TI_NVM_ID register. In this user guide, each PMIC device is distinguished by the TI orderable part number, TI_NVM_ID, and TI_NVM_REV values listed in Table 2-1.

Table 2-1. TPS6594-Q1 and LP8764-Q1 NVM Settings and Orderable Part Numbers

PDN USE CASE	Orderable Part Number	Device Mode	TI_NVM_ID	TI_NVM_REV
• Up to 4.25 A(1) on the CORE rail • Up to 4.25 A(1) on the CPU rails • Up to 3.4 A(1) on the SDRAM, with support for LPDDR4 • Supports Functional Safety up to ASIL-D level • Supports low power modes, including MCU-only, GPIO Retention, and DDR Retention states • Supports I/O level of 3.3 V or 1.8 V • Supports use of SD card	TPS6594141B	Primary	0x1B	0x01
	LP876441B1	Secondary	0xB1	0x01

(1) TI recommends having 15% margin between the maximum expected load current and the maximum current allowed per each PMIC output rail.

3 Processor Connections

This section details how the TPS6594-Q1 and LP8764-Q1 power resources and GPIO signals are connected to the processor and other peripheral components to support the PDN use case.

Figure 3-1 shows the detailed power mapping between the processor and the TPS6594-Q1 and LP8764-Q1 PMICs. In this configuration, both PMICs use a 3.3 V input voltage. For Functional Safety applications, there is a protection FET before VCCA that connects to the OVPGDRV pin of the primary PMIC, allowing voltage monitoring of the input supply to the PMICs.

The VCCA voltage must be the first voltage applied to the PMIC devices. VIO_IN of the PMICs must be supplied after VCCA. In this configuration, VIO_IN is supplied by the load switch that also supplies the VDDSHVx_MCU voltage domain of the processor to allow the digital components of the PMIC devices (such as GPIOs) to remain supplied in MCU-only mode. Additionally, by controlling VIO_IN of both PMICs through this load switch, the system can also reduce power consumption in GPIO Retention or DDR Retention modes, since the load switch is disabled.

This PDN supports the use of either a single dual load switch (TPS22966-Q1) with an AEC-100 Grade 2 (-40 to +105°C) temperature rating or two single load switches (TPS22965-Q1) with an AEC-100 Grade 1 (-40 to +125°C) rating if a higher ambient temperature range is desired. The PDN diagrams of this section also include a few optional discrete power components to support additional system functions that may be needed. The TLV70033-Q1 LDO is used to support compliant USB data eye performance by supplying a low noise 3.3 V for USB 2.0 interface integration. The TLV70018-Q1 LDO is available to support on-board EFUSE programming on high security SoC PNs. Alternative LDOs can be chosen for SD card dual-voltage I/O support (3.3 V and 1.8 V), TLV7103318-Q1 dual-voltage LDO can be used to enable compliant, dual voltage, high-speed SD card operations.

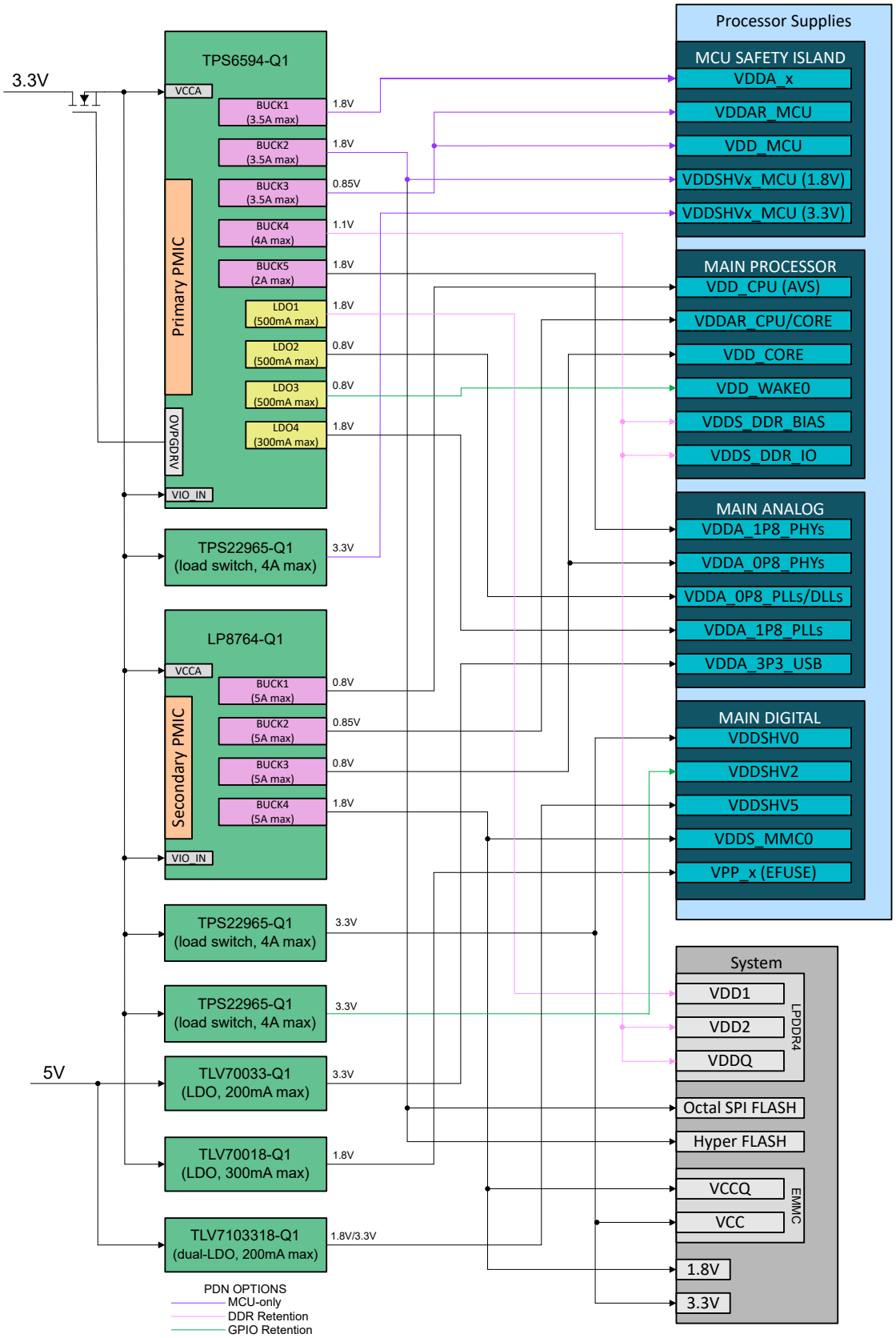


Figure 3-1. TPS6594-Q1 and LP8764-Q1 Power Connections

The power resource assignments shown in Figure 3-1 enable the support for different processor low-power modes, including MCU-only mode, GPIO Retention, and DDR Retention. Please use Table 3-1 as a guide to

understand which power resources are required to support different system features. If the system feature listed is not required, the power resource connection can be removed.

Table 3-1. Power Resources by System Power States

Device	PMIC Resource	Processor Domains	Power States			
			Active SoC	MCU - only	GPIO Retention	DDR Retention
TPS6594-Q1	BUCK1	VDDA_x	Required	Required		
	BUCK2	VDDSHVx_MCU (1.8V)	Required	Required		
	BUCK3	VDD_MCU, VDDAR_MCU	Required	Required		
	BUCK4	VDDS_DDR_BIAS, VDDS_DDR_IO	Required			Required
	BUCK5	VDDA_1P8_PHYs	Required			
	LDO1	N/A	Required			Required
	LDO2	VDDA_0P8_PLLs/DLLs	Required			
	LDO3	VDD_WAKE0	Required		Required	
	LDO4	VDDA_1P8_PLLs	Required			
LP8764-Q1	BUCK1	VDD_CPU	Required			
	BUCK2	VDDAR_CPU/CORE	Required			
	BUCK3	VDD_CORE, VDDA_0P8_PHYs	Required			
	BUCK4	VDDS_MMC0	Required			
TPS22965-Q1	Load Switch	VDDSHVx_MCU (3.3 V)	Required	Required		
TPS22966-Q1	Load Switch 1	VDDSHV0(1)	Required			
	Load Switch 2	VDDSHV2			Required	

(1) VDDSHV5 can also be powered by this rail if an SD card is not required in the system.

Figure 3-2 shows the digital control signal mapping between the processor and the PMIC devices. For the two PMIC devices to work together, the primary PMIC and secondary PMIC must establish an SPMI communication channel. The SPMI bus allows the TPS6594-Q1 and LP8764-Q1 to synchronize their internal Pre-Configurable State Machines (PFSM) so that they operate as one PFSM across all power and digital resources. The GPIO_5 and GPIO_6 pins on the TPS6594-Q1 and GPIO_8 and GPIO_9 pins on LP8764-Q1 are assigned for this functionality. In addition, the LDOVINT pin of the primary PMIC must be connected to the ENABLE input (GPIO_4 of LP8764-Q1) of the secondary PMIC to correctly initiate the PFSM.

Other digital connections from the TPS6594-Q1 devices to the processor allow support for error monitoring, processor reset, processor wake up, and system low-power modes. Specific GPIO pins have been assigned to key signals in order to ensure proper operation during low power modes when only a few GPIO pins remain operational.

To support DDR retention low power mode, the following PMIC GPIO functions are required:

1. GPIO_2 and GPIO_3 of LP8764-Q1 connected to an external, low voltage latch to create a sustained control signal to DDR_RET of the processor. The latch is needed since the PMIC VIO_IN power rail supplying GPIO_2 and 3 is disabled during DDR Retention state.
2. Sustained GPIO_9 of TPS6594-Q1 connected to the enable input of a 3.3V in-line load switch to the MCU.
3. Sustained GPIO_4 of TPS6594-Q1 with NVM default function set as LP_WKUP1 and mask bit set high to avoid false triggering until CAN wakeup signal is armed. SW must properly arm CAN PHY so that wakeup signal is set high and unmask GPIO_4 before entering GPIO Retention state.

GPIO_4 of TPS6594-Q1 is powered by the VRTC internal voltage domain of the PMIC. The LDOVRTC regulator supplies always-on functions, such as the wake-up function of GPIO_4. This enables GPIO_4 to be used as a wake-up source in LP_STANDBY when LDO_VINT is turned off.

To support GPIO retention low power mode, the following PMIC GPIO functions are required:

1. Sustained GPIO_7 of LP8764-Q1 connected to the enable input of an in-line load switch to control the 3.3 V GPIO retention domain.

Additional digital options also include GPIO_10 of TPS6594-Q1, which can be configured by software as a 32 kHz clock output for the processor oscillator input (LFOSC). There is also the option to disable the watchdog timer using hardware, by pulling GPIO_8 of TPS6594-Q1 high. Lastly, GPIO_1 of LP8764-Q1 is included in the power up sequence to enable external regulators, for options such as DDR I/O.

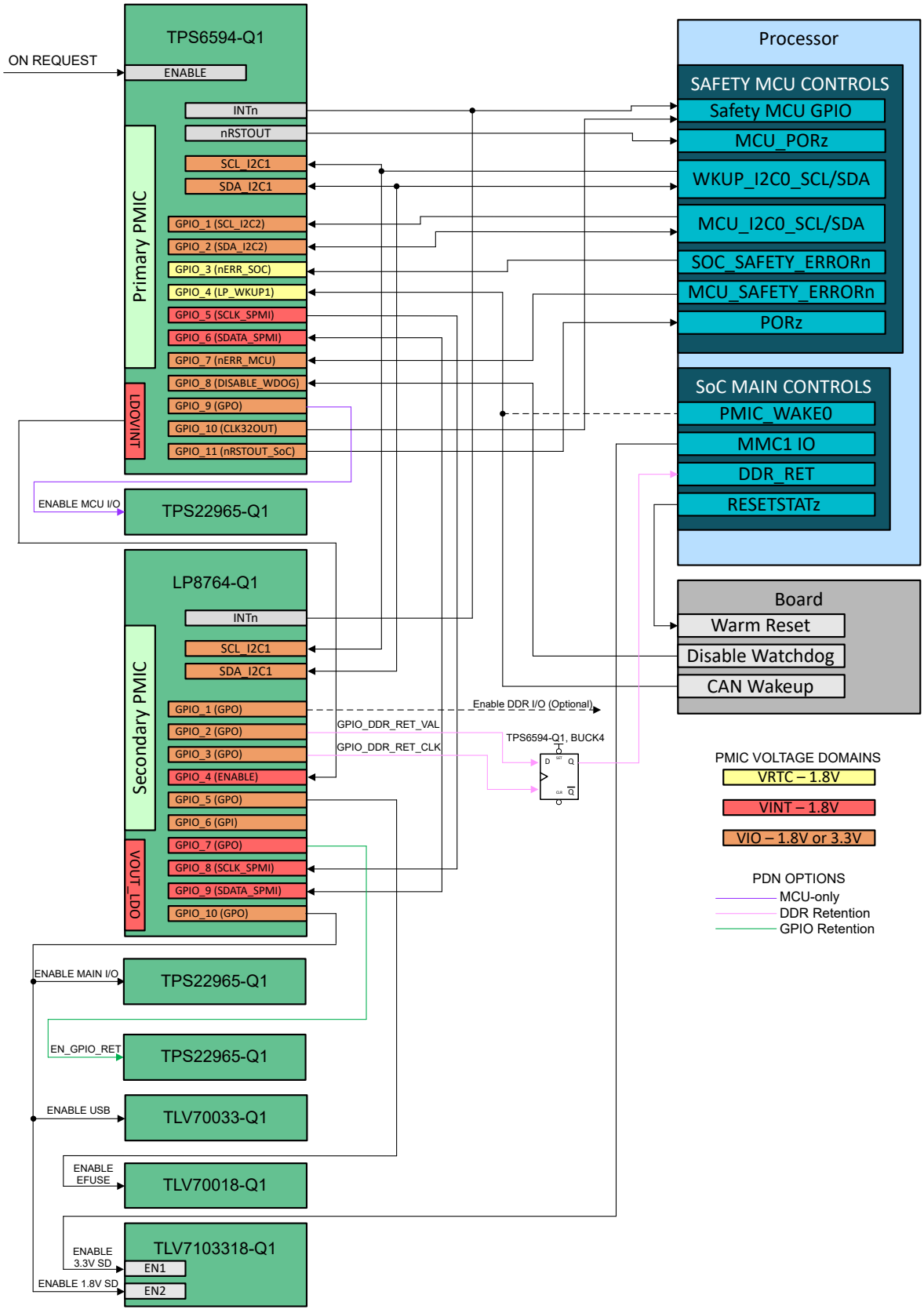


Figure 3-2. TPS6594-Q1 and LP8764-Q1 Digital Connections

The digital connections shown in Figure 3-2 allow system features including MCU-only mode, GPIO retention mode, DDR retention mode, and functional safety systems capable of supporting up to ASIL-D. Please use Table

3-2 as a guide to understand GPIO assignments required for these features. If the feature listed is not required, the digital connection can be removed. For details on how functional safety related connections help achieve functional safety system-level goals, see Section 4.

Table 3-2. Digital Connections by System Feature

Device	PMIC Digital Signal	System Digital Signal	System Features				
			Active SoC	Functional Safety	MCU - only	GPIO Retention	DDR Retention
TPS6594-Q1	nPWRON/ ENABLE	System ON Request	Required				
	INT(1)	Safety MCU GPIO		Required			
	nRSTOUT(1)	MCU_PORz	Required		Required		
	SCL_I2C1	WKUP_I2C0_SCL	Required				
	SDA_I2C1	WKUP_I2C0_SDA	Required				
	GPIO_1	MCU_I2C0_SCL		Required			
	GPIO_2	MCU_I2C0_SCL		Required			
	GPIO_3	SOC_SAFETY_ERRORn		Optional			
	GPIO_4(2)	CAN Wakeup				Required	Required
	GPIO_5	PMIC SPMI CLK	Required				
	GPIO_6	PMIC SPMI DATA	Required				
	GPIO_7	MCU_SAFETY_ERRORn		Optional			
	GPIO_8 (5)	Disable Watchdog	(3)	(3)			
	GPIO_9	ENABLE MCU I/O	Required				
	GPIO_10(4)	WKUP_LFOSC0	Required				
	GPIO_11(1)	SOC_PORz		Required	Required		
LP8764-Q1	INT(1)	Safety MCU GPIO		Required			
	SCL_I2C1	WKUP_I2C0_SCL	Required				
	SDA_I2C1	WKUP_I2C0_SDA	Required				
	GPIO_1	Enable DDR I/O (Optional)					
	GPIO_2(5)	External Latch Data Input					Required
	GPIO_3(5)	External Latch Clock Input					Required
	GPIO_4	TPS6594-Q1 LDOVINT	Required				
	GPIO_5(5)	Enable EFUSE					
	GPIO_6 (5)	N/A					
	GPIO_7	EN_GPIO_RET	Required				Required
	GPIO_8	PMIC SPMI CLK	Required				
	GPIO_9	PMIC SPMI DATA	Required				
	GPIO_10	Enable Main I/O			Required	Required	Required

(1) This pin is open-drain to enable voltage translation to correct voltage level for processor interface.
(2) Software must unmask GPIO_4 before the system expects to trigger a wakeup on this pin.
(3) If it is desired to disable the watchdog through hardware, GPIO_8 is required and must be set high by the time nRSTOUT goes high. After nRSTOUT is high, the watchdog state is latched and the pin can be configured for other functions through software.
(4) GPIO_10 is set as a general purpose input (GPI) by default to allow processor to boot up before sourcing the 32 kHz to the processor, since both bootmode and low frequency clock inputs to the processor utilize the same pin.
(5) This GPIO is not required for power sequencing or PMIC functionality and can be configured by software for a different purpose if desired.

4 Supporting Functional Safety Systems

By using the TPS6594-Q1 and LP8764-Q1 solution to power the DRA821 processor, the system can leverage the following PMIC functional safety features:

- Independent Power Control of MCU and Main Rails
- Independent Monitoring and Reset for MCU and Main Rails
- Input Supply Monitoring
- Output Voltage and Current Monitoring
- Question & Answer Watchdog
- Fault Reporting Interrupts
- Enable Drive Pin that provides an independent path to disable system actuators
- Error Pin Monitoring
- Internal Diagnostics including voltage monitoring, temperature monitoring, and Built-In Self-Test

Refer to the Safety Manuals of the TPS6594-Q1 and LP8764-Q1 devices for full descriptions and analysis of the PMIC functional safety features. These functional safety features can assist in achieving up to ASIL-D rating for a system. Additionally, these features help in achieving the functional safety assumptions utilized by the processor to achieve up to ASIL-D rating. See the DRA821 Safety Manual for Jacinto™ 7 Processors for a complete list of functional safety system assumptions.

4.1 Achieving ASIL-B System Requirements

To achieve a system functional safety level of ASIL-B, the following PDN features are available:

- PMIC over voltage and under voltage monitoring on the power resource voltage outputs
- PMIC over-voltage monitoring and protection on the input to the PMIC (VCCA)
- Watchdog monitoring of safety processor
- MCU error monitoring
- MCU reset
- I2C communication
- Error indicator, EN_DRV, for driving external circuitry (optional)
- Read-back of EN_DRV pin

The PDN has an in-line, external power FET between the input supply and PMICs. This FET can quickly isolate the PMICs when an over-voltage event greater than 6 V is detected on the input supply to protect the system from being damaged, as shown in Figure 3-1. Note that any power rail connected after the FET can be protected from an over voltage event. Any power connected upstream from the FET is not protected from over voltage events. In Figure 3-1 the load switches that supply power to the MCU and Main I/O domains and the discrete buck supplying the DDR are all connected after the FET to extend the over voltage protection to these processor domains and discrete power resources.

The PMIC internal over voltage and under voltage monitoring and their respective monitoring threshold levels can be enabled through I2C after startup. To monitor the load switch voltage that supplies the MCU I/O of the processor, it is recommended to use the processor POK monitor built into the VDDSHV0_MCU voltage domain.

The PMIC Internal Q&A Watchdog is enabled by default on the TPS6594-Q1 device. Once the device is in ACTIVE state, the trigger or Q&A watchdog settings can be configured through the secondary I2C in the device. The steps for configuring the watchdog settings can be found in the TPS6594-Q1 data sheet. Setting the DISABLE_WDOG signal high on TPS6594-Q1 GPIO_8 disables the watchdog timer if this feature needs to be suspended or is not required in the system.

GPIO_7 of the TPS6594-Q1 PMIC is configured as the MCU error signal monitoring, and must be enabled though the ESM_MCU_EN register bit. MCU reset is supported through the connection between the primary PMIC nRSTOUT pin and the MCU_PORz of the processor. Lastly, there are 2 I2C ports between the TPS6594-Q1 and the processor. The first is used for all non-watchdog communication, such as voltage level control, and the second allows the watchdog monitoring to be on an independent communication channel.

There is an option to use the EN_DRV of theTPS6594-Q1 PMIC to indicate an error has been detected and the system is entering SAFE state. This signal can be utilized if the system has some additional external circuitry that needs to be driven by an error event. In this PDN, the EN_DRV is not utilized, but available if needed.

4.2 Achieving up to ASIL-D System Requirements

For ASIL-C or ASIL-D systems, there are additional features to the ones described in Section 4.1 that can be utilized. These features include:

- PMIC current monitoring on all output power rails
- Isolation of the MCU and Main power domains of the processor
- SoC reset

The current monitoring is enabled by default for all BUCKs and LDOs for the TPS6594-Q1 and LP8764-Q1 devices. Additionally, Figure 3-1 shows that the MCU domain of the processor is powered by different power resources of the PMICs than the main power domain of the processor. SoC reset functionality is supported through the connection of GPIO_11 on TPS6594-Q1, configured as nRSTOUT_SoC, to the PORz pin of the processor.

Note

Residual voltage checking is available on the PMICs to prevent startup when output rails are not discharged below 100 mV as may happen under a fault condition. However, this feature is not enabled in the NVM settings of this PDN to support repetitive power cycling during system software development.

5 Static NVM Settings

The TPS6594-Q1 and LP8764-Q1 devices consist of fixed registers and configurable registers that are loaded from the NVM. For all NVM registers, the initial NVM settings that load into the registers are provided in this section. Note that these initial NVM settings can be changed during state transitions, such as moving from STANDBY to ACTIVE mode. The full register map, including default values of fixed registers, is located in the corresponding PMIC data sheet. Empty values indicate that the device does not have the register included. For example, LP8764-Q1 does not have BUCK5 registers at all and therefore the values for it are empty.

5.1 Application-Based Configuration Settings

In the LP876441B1-Q1 and TPS6594141B-Q1 data sheet, there are multiple application-based configurations for each BUCK to operate within. Table 5-1 includes the different configurations available:

Table 5-1. LP876441B1-Q1 and TPS6594141B-Q1 Use Cases

TPS6594141B-Q1	LP876441B1-Q1
2.2 MHz Single Phase for DDR Termination	2.2MHz Single-Phase for DDR Termination
4.4 MHz VOUT Less than 1.9 V, Multiphase	4.4MHz Single-Phase and Multi-Phase
4.4 MHz VOUT Less than 1.9 V, Single Phase	4.4MHz Single-Phase, Low Output Voltage
4.4 MHz VOUT Greater than 1.7 V, Single Phase	4.4MHz Single-Phase, High Output Voltage
2.2 MHz VOUT Less than 1.9 V, Multiphase or Single Phase	2.2MHz Single-Phase Configuration with 5.0V VIN
2.2 MHz Full VOUT Range with 5.0 V VIN, Single Phase	2.2MHz Single-Phase and Multi-Phase Configuration
2.2 MHz Full VOUT and Full VIN Range, Single Phase	2.2MHz Single-Phase Generic Configuration

The seven configurations also have optimal output inductance values that optimize the performance of each buck under these various conditions. Table 5-2 shows the default configurations for the BUCKs. These settings cannot be changed after device startup.

Table 5-2. Application Use Case Settings

Device	BUCK Rail	Default Application Use Case	Recommended Inductor Value
TPS6594141B-Q1	BUCK1	4.4 MHz VOUT Less than 1.9 V, Single Phase	220 nH
	BUCK2	4.4 MHz VOUT Less than 1.9 V, Single Phase	220 nH
	BUCK3	4.4 MHz VOUT Less than 1.9 V, Single Phase	220 nH
	BUCK4	4.4 MHz VOUT Less than 1.9 V, Single Phase	220 nH
	BUCK5	4.4 MHz VOUT Less than 1.9 V, Single Phase	220 nH
LP876441B1-Q1	BUCK1	4.4MHz Single-Phase, Low Output Voltage	220 nH
	BUCK2	4.4MHz Single-Phase, Low Output Voltage	220 nH
	BUCK3	4.4MHz Single-Phase, Low Output Voltage	220 nH
	BUCK4	4.4MHz Single-Phase, Low Output Voltage	220 nH

5.2 Device Identification Settings

These settings are used to distinguish which device is detected in a system. These settings cannot be changed after device startup.

Table 5-3. Device Identification NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
DEV_REV	DEVICE_ID	0x82	0x82	0x86	0x86
NVM_CODE_1	TI_NVM_ID	0x1B	0x1B	0xb1	0xb1
NVM_CODE_2	TI_NVM_REV	0x1	0x1	0x1	0x1
PHASE_CONFIG	MP_CONFIG	0x1	1+1+1+1+1	0x1	1+1+1+1

5.3 BUCK Settings

These settings detail the default voltages, configurations, and monitoring of the BUCK rails. All these settings can be changed though I^2C after startup.

Table 5-4. BUCK NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
BUCK1_CTRL	BUCK1_EN(1)	0x0	Disabled; BUCK1 regulator	0x0	Disabled; BUCK1 regulator
	BUCK1_FPWM	0x0	PFM and PWM operation (AUTO mode).	0x0	PFM and PWM operation (AUTO mode).
	BUCK1_FPWM_MP	0x0	Automatic phase adding and shedding.	0x0	Automatic phase adding and shedding.
	BUCK1_VMON_EN(1)	0x0	Disabled; OV, UV, SC and ILIM comparators.	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK1_VSEL	0x0	BUCK1_VOUT_1	0x0	BUCK1_VOUT_1
	BUCK1_PLDN	0x1	Enabled; Pull-down resistor	0x1	Enabled; Pull-down resistor
	BUCK1_RV_SEL	0x1	Enabled	0x1	Enabled
BUCK1_CONF	BUCK1_SLEW_RATE	0x3	5.0 mV/µs	0x3	5.0 mV/µs
	BUCK1_ILIM	0x5	5.5 A	0x7	7.5 A
BUCK2_CTRL	BUCK2_EN(1)	0x0	Disabled; BUCK2 regulator	0x0	Disabled; BUCK2 regulator
	BUCK2_FPWM	0x0	PFM and PWM operation (AUTO mode).	0x0	PFM and PWM operation (AUTO mode).
	BUCK2_VMON_EN(1)	0x0	Disabled; OV, UV, SC and ILIM comparators.	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK2_VSEL	0x0	BUCK2_VOUT_1	0x0	BUCK2_VOUT_1
	BUCK2_PLDN	0x1	Enabled; Pull-down resistor	0x1	Enabled; Pull-down resistor
	BUCK2_RV_SEL	0x1	Enabled	0x1	Enabled
BUCK2_CONF	BUCK2_SLEW_RATE	0x3	5.0 mV/µs	0x3	5.0 mV/µs
	BUCK2_ILIM	0x5	5.5 A	0x7	7.5 A
BUCK3_CTRL	BUCK3_EN(1)	0x0	Disabled; BUCK3 regulator	0x0	Disabled; BUCK3 regulator
	BUCK3_FPWM	0x0	PFM and PWM operation (AUTO mode).	0x0	PFM and PWM operation (AUTO mode).
	BUCK3_FPWM_MP	0x0	Automatic phase adding and shedding.	0x0	Automatic phase adding and shedding.
	BUCK3_VMON_EN(1)	0x0	Disabled; OV, UV, SC and ILIM comparators.	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK3_VSEL	0x0	BUCK3_VOUT_1	0x0	BUCK3_VOUT_1
	BUCK3_PLDN	0x1	Enabled; Pull-down resistor	0x1	Enabled; Pull-down resistor
	BUCK3_RV_SEL	0x1	Enabled	0x1	Enabled
BUCK3_CONF	BUCK3_SLEW_RATE	0x3	5.0 mV/µs	0x3	5.0 mV/µs
	BUCK3_ILIM	0x5	5.5 A	0x7	7.5 A
BUCK4_CTRL	BUCK4_EN(1)	0x0	Disabled; BUCK4 regulator	0x0	Disabled; BUCK4 regulator
	BUCK4_FPWM	0x0	PFM and PWM operation (AUTO mode).	0x0	PFM and PWM operation (AUTO mode).
	BUCK4_VMON_EN(1)	0x0	Disabled; OV, UV, SC and ILIM comparators.	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK4_VSEL	0x0	BUCK4_VOUT_1	0x0	BUCK4_VOUT_1
	BUCK4_PLDN	0x1	Enabled; Pull-down resistor	0x1	Enabled; Pull-down resistor
	BUCK4_RV_SEL	0x1	Enabled	0x1	Enabled
BUCK4_CONF	BUCK4_SLEW_RATE	0x3	5.0 mV/µs	0x3	5.0 mV/µs
	BUCK4_ILIM	0x5	5.5 A	0x7	7.5 A

Table 5-4. BUCK NVM Settings (continued)

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
BUCK5_CTRL	BUCK5_EN(1)	0x0	Disabled; BUCK5 regulator		
	BUCK5_FPWM	0x0	PFM and PWM operation (AUTO mode).		
	BUCK5_VMON_EN(1)	0x0	Disabled; OV, UV, SC and ILIM comparators.		
	BUCK5_VSEL	0x0	BUCK5_VOUT_1		
	BUCK5_PLDN	0x1	Enable Pull-down resistor		
	BUCK5_RV_SEL	0x1	Enabled		
BUCK5_CONF	BUCK5_SLEW_RATE	0x3	5.0 mV/µs		
	BUCK5_ILIM	0x3	3.5 A		
BUCK1_VOUT_1	BUCK1_VSET1	0xb2	1.80 V	0x37	0.800 V
BUCK1_VOUT_2	BUCK1_VSET2	0x0	0.3 V	0x0	0.3 V
BUCK2_VOUT_1	BUCK2_VSET1	0xb2	1.80 V	0x41	0.850 V
BUCK2_VOUT_2	BUCK2_VSET2	0x0	0.3 V	0x0	0.3 V
BUCK3_VOUT_1	BUCK3_VSET1	0x41	0.850 V	0x37	0.800 V
BUCK3_VOUT_2	BUCK3_VSET2	0x0	0.3 V	0x0	0.3 V
BUCK4_VOUT_1	BUCK4_VSET1	0x73	1.10 V	0xb2	1.80 V
BUCK4_VOUT_2	BUCK4_VSET2	0x0	0.3 V	0x0	0.3 V
BUCK5_VOUT_1	BUCK5_VSET1	0xb2	1.80 V		
BUCK5_VOUT_2	BUCK5_VSET2	0x0	0.3 V		
BUCK1_PG_WINDOW	BUCK1_OV_THR	0x2	+4% / +40 mV	0x2	+4% / +40 mV
	BUCK1_UV_THR	0x2	-4% / -40 mV	0x2	-4% / -40 mV
BUCK2_PG_WINDOW	BUCK2_OV_THR	0x2	+4% / +40 mV	0x2	+4% / +40 mV
	BUCK2_UV_THR	0x2	-4% / -40 mV	0x2	-4% / -40 mV
BUCK3_PG_WINDOW	BUCK3_OV_THR	0x2	+4% / +40 mV	0x2	+4% / +40 mV
	BUCK3_UV_THR	0x2	-4% / -40 mV	0x2	-4% / -40 mV
BUCK4_PG_WINDOW	BUCK4_OV_THR	0x2	+4% / +40 mV	0x2	+4% / +40 mV
	BUCK4_UV_THR	0x2	-4% / -40 mV	0x2	-4% / -40 mV
BUCK5_PG_WINDOW	BUCK5_OV_THR	0x2	+4% / +40 mV		
	BUCK5_UV_THR	0x2	-4% / -40 mV		
VMON1_PG_WINDOW	VMON1_RANGE			0x0	0.3 - 3.34 V
	VMON1_UV_THR			0x0	-3% / -30 mV / (-150 mV)
	VMON1_OV_THR			0x0	+3% / +30 mV / (+150 mV)
VMON1_PG_LEVEL	VMON1_PG_SET			0x0	0x0
VMON2_PG_WINDOW	VMON2_RANGE			0x0	0.3 - 3.34 V
	VMON2_UV_THR			0x0	-3% / -30 mV / (-150 mV)
	VMON2_OV_THR			0x0	+3% / +30mV / (+150 mV)

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

5.4 LDO Settings

These settings detail the default voltages, configurations, and monitoring of the LDO rails. All these settings can be changed though I^2C after startup. Note that only TPS6594141B-Q1 device contains LDO outputs.

Table 5-5. LDO NVM Settings

Register Name	Field Name	TPS6594141B-Q1	
		Value	Description
LDO1_CTRL	LDO1_EN(1)	0x0	Disabled; LDO1 regulator.
	LDO1_PLDN	0x2	250 Ohm
	LDO1_VMON_EN(1)	0x0	Disable OV and UV comparators.
	LDO1_RV_SEL	0x1	Enabled
LDO2_CTRL	LDO2_EN(1)	0x0	Disabled; LDO2 regulator.
	LDO2_PLDN	0x1	125 Ohm
	LDO2_VMON_EN(1)	0x0	Disabled; OV and UV comparators.
	LDO2_RV_SEL	0x1	Enabled
LDO3_CTRL	LDO3_EN(1)	0x0	Disabled; LDO3 regulator.
	LDO3_PLDN	0x1	125 Ohm
	LDO3_VMON_EN(1)	0x0	Disabled; OV and UV comparators.
	LDO3_RV_SEL	0x1	Enabled
LDO4_CTRL	LDO4_EN(1)	0x0	Disabled; LDO4 regulator.
	LDO4_PLDN	0x1	125 Ohm
	LDO4_VMON_EN(1)	0x0	Disabled; OV and UV comparators.
	LDO4_RV_SEL	0x1	Enabled
LDO1_VOUT	LDO1_VSET	0x1c	1.80 V
	LDO1_BYPASS	0x0	Linear regulator mode.
LDO2_VOUT	LDO2_VSET	0x8	0.80 V
	LDO2_BYPASS	0x0	Linear regulator mode.
LDO3_VOUT	LDO3_VSET	0x8	0.80 V
	LDO3_BYPASS	0x0	Linear regulator mode.
LDO4_VOUT	LDO4_VSET	0x38	1.800 V
LDO1_PG_WINDOW	LDO1_OV_THR	0x2	+4% / +40 mV
	LDO1_UV_THR	0x2	-4% / -40 mV
LDO2_PG_WINDOW	LDO2_OV_THR	0x2	+4% / +40 mV
	LDO2_UV_THR	0x2	-4% / -40 mV
LDO3_PG_WINDOW	LDO3_OV_THR	0x2	+4% / +40 mV
	LDO3_UV_THR	0x2	-4% / -40 mV
LDO4_PG_WINDOW	LDO4_OV_THR	0x2	+4% / +40 mV
	LDO4_UV_THR	0x2	-4% / -40 mV

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

5.5 VCCA Settings

These settings detail the default monitoring enabled on VCCA. All these settings can be changed though I^2C after startup.

Table 5-6. VCCA NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
VCCA_VMON_CTRL	VMON_DEGLITCH_SEL	0x1	20 us	0x1	VCCA 20us, VMON/BUCK 20us
	VMON2_RV_SEL			0x0	Disabled
	VMON2_EN			0x0	Disabled; OV and UV comparators.
	VMON1_RV_SEL			0x0	Disabled
	VMON1_EN			0x0	Disabled; OV and UV comparators.
	VCCA_VMON_EN	0x1	Enabled; OV and UV comparators.	0x1	Enabled; OV and UV comparators.
VCCA_PG_WINDOW	VCCA_OV_THR	0x7	+10%	0x7	+10%
	VCCA_UV_THR	0x7	-10%	0x7	-10%
	VCCA_PG_SET	0x0	3.3 V	0x0	3.3 V

5.6 GPIO Settings

These settings detail the default configurations of the GPIO rails. All these settings can be changed though I^2C after startup. Note that the contents of the GPIOx_SEL field determine which other fields in the GPIOx_CONF and GPIO_OUT_x registers are applicable. To understand which NVM fields apply to each GPIOx_SEL option, see the *Digital Signal Descriptions* section in TPS6594-Q1 and LP8764-Q1 data sheets.

Table 5-7. GPIO NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
GPIO1_CONF	GPIO1_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO1_DIR	0x0	Input	0x1	Output
	GPIO1_SEL	0x1	SCL_I2C2/CS_SPI	0x0	GPIO1
	GPIO1_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO1_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO1_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x0	No deglitch, only synchronization.
GPIO2_CONF	GPIO2_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO2_DIR	0x0	Input	0x0	Input
	GPIO2_SEL	0x2	SDA_I2C2/SDO_SPI	0x0	GPIO2
	GPIO2_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO2_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO2_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x1	8 us deglitch time.
GPIO3_CONF	GPIO3_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO3_DIR	0x0	Input	0x0	Input
	GPIO3_SEL	0x2	NERR_SOC	0x0	GPIO3
	GPIO3_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO3_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO3_DEGLITCH_EN	0x1	8 us deglitch time.	0x1	8 us deglitch time.

Table 5-7. GPIO NVM Settings (continued)

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
GPIO4_CONF	GPIO4_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO4_DIR	0x0	Input	0x0	Input
	GPIO4_SEL	0x6	LP_WKUP1	0x0	GPIO4
	GPIO4_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO4_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO4_DEGLITCH_EN	0x1	8 us deglitch time.	0x1	8 us deglitch time.
GPIO5_CONF	GPIO5_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO5_DIR	0x0	Input	0x0	Input
	GPIO5_SEL	0x1	SCLK_SPMI	0x0	GPIO5
	GPIO5_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO5_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO5_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x1	8 us deglitch time.
GPIO6_CONF	GPIO6_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO6_DIR	0x0	Input	0x0	Input
	GPIO6_SEL	0x1	SDATA_SPMI	0x0	GPIO6
	GPIO6_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO6_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO6_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x1	8 us deglitch time.
GPIO7_CONF	GPIO7_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO7_DIR	0x0	Input	0x1	Output
	GPIO7_SEL	0x1	NERR_MCU	0x0	GPIO7
	GPIO7_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO7_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO7_DEGLITCH_EN	0x1	8 us deglitch time.	0x0	No deglitch, only synchronization.
GPIO8_CONF	GPIO8_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO8_DIR	0x0	Input	0x0	Input
	GPIO8_SEL	0x3	DISABLE_WDOG	0x1	SCLK_SPMI
	GPIO8_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO8_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO8_DEGLITCH_EN	0x1	8 us deglitch time.	0x0	No deglitch, only synchronization.
GPIO9_CONF	GPIO9_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO9_DIR	0x1	Output	0x0	Input
	GPIO9_SEL	0x0	GPIO9	0x1	SDATA_SPMI
	GPIO9_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO9_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO9_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x0	No deglitch, only synchronization.

Table 5-7. GPIO NVM Settings (continued)

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
GPIO10_CONF	GPIO10_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO10_DIR	0x0	Input	0x1	Output
	GPIO10_SEL	0x0	GPIO10	0x0	GPIO10
	GPIO10_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO10_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO10_DEGLITCH_EN	0x1	8 us deglitch time.	0x0	No deglitch, only synchronization.
GPIO11_CONF	GPIO11_OD	0x1	Open-drain output		
	GPIO11_DIR	0x1	Output		
	GPIO11_SEL	0x2	NRSTOUT_SOC		
	GPIO11_PU_SEL	0x0	Pull-down resistor selected		
	GPIO11_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.		
	GPIO11_DEGLITCH_EN	0x0	No deglitch, only synchronization.		
NPWRON_CONF	NPWRON_SEL	0x0	ENABLE		
	ENABLE_PU_SEL	0x0	Pull-down resistor selected		
	ENABLE_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.		
	ENABLE_DEGLITCH_EN	0x1	8 us deglitch time when ENABLE, 50 ms deglitch time when NPWRON.		
	ENABLE_POL	0x0	Active high	0x0	Active high
	NRSTOUT_OD	0x1	Open-drain output		
GPIO_OUT_1	GPIO1_OUT(1)	0x0	Low	0x0	Low
	GPIO2_OUT(1)	0x0	Low	0x0	Low
	GPIO3_OUT(1)	0x0	Low	0x0	Low
	GPIO4_OUT(1)	0x0	Low	0x0	Low
	GPIO5_OUT(1)	0x0	Low	0x0	Low
	GPIO6_OUT(1)	0x0	Low	0x0	Low
	GPIO7_OUT(1)	0x0	Low	0x0	Low
	GPIO8_OUT(1)	0x0	Low	0x0	Low
GPIO_OUT_2	GPIO9_OUT(1)	0x0	Low	0x0	Low
	GPIO10_OUT(1)	0x0	Low	0x0	Low
	GPIO11_OUT(1)	0x0	Low		

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

5.7 Finite State Machine (FSM) Settings

These settings describe how the PMIC output rails are assigned to various system-level states. Also, the default trigger for each system-level state is described. All these settings can be changed though I^2C after startup.

Table 5-8. FSM NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
RAIL_SEL_1	BUCK1_GRP_SEL	0x1	MCU rail group	0x2	SOC rail group
	BUCK2_GRP_SEL	0x1	MCU rail group	0x2	SOC rail group
	BUCK3_GRP_SEL	0x1	MCU rail group	0x2	SOC rail group
	BUCK4_GRP_SEL	0x1	MCU rail group	0x2	SOC rail group

Table 5-8. FSM NVM Settings (continued)

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
RAIL_SEL_2	BUCK5_GRP_SEL	0x2	SOC rail group		
	LDO1_GRP_SEL	0x1	MCU rail group		
	LDO2_GRP_SEL	0x2	SOC rail group		
	LDO3_GRP_SEL	0x1	MCU rail group		
RAIL_SEL_3	VMON2_GRP_SEL			0x0	No group assigned
	VMON1_GRP_SEL			0x0	No group assigned
	LDO4_GRP_SEL	0x2	SOC rail group		
	VCCA_GRP_SEL	0x1	MCU rail group	0x1	MCU rail group
FSM_TRIG_SEL_1	MCU_RAIL_TRIG	0x2	MCU power error	0x2	MCU power error
	SOC_RAIL_TRIG	0x3	SOC power error	0x3	SOC power error
	OTHER_RAIL_TRIG	0x3	SOC power error	0x3	SOC power error
	SEVERE_ERR_TRIG	0x0	Immediate shutdown	0x0	Immediate shutdown
FSM_TRIG_SEL_2	MODERATE_ERR_TRIG	0x1	Orderly shutdown	0x1	Orderly shutdown

5.8 Interrupt Settings

These settings detail the default configurations for what is monitored by nINT pin. All these settings can be changed though I^2C after startup.

Table 5-9. Interrupt NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
FSM_TRIG_MASK_1	GPIO1_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO1_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO2_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO2_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO3_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO3_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO4_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO4_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_2	GPIO5_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO5_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO6_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO6_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO7_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO7_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO8_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO8_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'

Table 5-9. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
FSM_TRIG_MASK_3	GPIO9_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO9_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO10_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO10_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO11_FSM_MASK	0x1	Masked		
	GPIO11_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'		
MASK_BUCK1_2	BUCK1_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK1_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK1_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK2_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK2_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK2_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
MASK_BUCK3_4	BUCK3_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK3_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK3_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK4_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK4_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK4_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
MASK_BUCK5	BUCK5_ILIM_MASK	0x0	Interrupt generated		
	BUCK5_OV_MASK	0x0	Interrupt generated		
	BUCK5_UV_MASK	0x0	Interrupt generated		
MASK_LDO1_2	LDO1_OV_MASK	0x0	Interrupt generated		
	LDO1_UV_MASK	0x0	Interrupt generated		
	LDO2_OV_MASK	0x0	Interrupt generated		
	LDO2_UV_MASK	0x0	Interrupt generated		
	LDO1_ILIM_MASK	0x0	Interrupt generated		
	LDO2_ILIM_MASK	0x0	Interrupt generated		
MASK_LDO3_4	LDO3_OV_MASK	0x0	Interrupt generated		
	LDO3_UV_MASK	0x0	Interrupt generated		
	LDO4_OV_MASK	0x0	Interrupt generated		
	LDO4_UV_MASK	0x0	Interrupt generated		
	LDO3_ILIM_MASK	0x0	Interrupt generated		
	LDO4_ILIM_MASK	0x0	Interrupt generated		
MASK_VMON	VMON2_UV_MASK			0x1	Interrupt not generated.
	VMON2_OV_MASK			0x1	Interrupt not generated.
	VMON1_UV_MASK			0x1	Interrupt not generated.
	VMON1_OV_MASK			0x1	Interrupt not generated.
	VCCA_OV_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	VCCA_UV_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.

Table 5-9. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
MASK_GPIO1_8_FALL	GPIO1_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO2_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO3_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO4_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO5_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO6_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO7_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO8_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
MASK_GPIO1_8_RISE	GPIO1_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO2_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO3_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO4_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO5_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO6_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO7_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO8_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
MASK_GPIO9_11 / MASK_GPIO9_10	GPIO9_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO9_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO10_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO11_FALL_MASK	0x1	Interrupt not generated.		
	GPIO10_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO11_RISE_MASK	0x1	Interrupt not generated.		
MASK_STARTUP	NPWRON_START_MASK	0x1	Interrupt not generated.		
	ENABLE_MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
	FSD_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
MASK_MISC	TWARN_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BIST_PASS_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	EXT_CLK_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
MASK_MODERATE_ERR	BIST_FAIL_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	REG_CRC_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	SPMI_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	NPWRON_LONG_MASK	0x1	Interrupt not generated.		
	PFSM_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
MASK_FSM_ERR	WD_MASK			0x1	Interrupt not generated.
	IMM_SHUTDOWN_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	MCU_PWR_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	SOC_PWR_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	ORD_SHUTDOWN_MASK	0x0	Interrupt generated	0x0	Interrupt generated

Table 5-9. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
MASK_COMM_ERR	COMM_FRM_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	COMM_CRC_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	COMM_ADR_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	I2C2_CRC_ERR_MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
	I2C2_ADR_ERR_MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
MASK_READBACK_ERR	EN_DRV_READBACK_MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
	NINT_READBACK_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	NRSTOUT_READBACK_ MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
	NRSTOUT_SOC_ READBACK_MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
MASK_ESM	ESM_SOC_PIN_MASK	0x1	Interrupt not generated.		
	ESM_SOC_RST_MASK	0x1	Interrupt not generated.		
	ESM_SOC_FAIL_MASK	0x1	Interrupt not generated.		
	ESM_MCU_PIN_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	ESM_MCU_RST_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	ESM_MCU_FAIL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.

5.9 POWERGOOD Settings

These settings detail the default configurations for what is monitored by PGOOD pin. All these settings can be changed though I^2C after startup.

Table 5-10. POWERGOOD NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
PGOOD_SEL_1	PGOOD_SEL_BUCK1	0x0	Masked	0x0	Masked
	PGOOD_SEL_BUCK2	0x0	Masked	0x0	Masked
	PGOOD_SEL_BUCK3	0x0	Masked	0x0	Masked
	PGOOD_SEL_BUCK4	0x0	Masked	0x0	Masked
PGOOD_SEL_2	PGOOD_SEL_BUCK5	0x0	Masked		
PGOOD_SEL_3	PGOOD_SEL_LDO1	0x0	Masked		
	PGOOD_SEL_LDO2	0x0	Masked		
	PGOOD_SEL_LDO3	0x0	Masked		
	PGOOD_SEL_LDO4	0x0	Masked		

Table 5-10. POWERGOOD NVM Settings (continued)

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
PGOOD_SEL_4	PGOOD_SEL_VCCA	0x0	Masked	0x0	Masked
	PGOOD_SEL_VMON1			0x0	Masked
	PGOOD_SEL_VMON2			0x0	Masked
	PGOOD_SEL_TDIE_WARN	0x0	Masked	0x0	Masked
	PGOOD_SEL_NRSTOUT	0x0	Masked	0x0	Masked
	PGOOD_SEL_NRSTOUT_ SOC	0x0	Masked	0x0	Masked
	PGOOD_POL	0x0	PGOOD signal is high when monitored inputs are valid	0x0	PGOOD signal is high when monitored inputs are valid
	PGOOD_WINDOW	0x1	Both undervoltage and overvoltage are monitored	0x0	Only undervoltage is monitored

5.10 Miscellaneous Settings

These settings detail the default configurations of additional settings, such as spread spectrum, BUCK frequency, and LDO timeout. All these settings can be changed though I^2C after startup.

Table 5-11. Miscellaneous NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
PLL_CTRL	EXT_CLK_FREQ	0x1	2.2 MHz	0x0	1.1 MHz
CONFIG_1	TWARN_LEVEL	0x0	130C	0x0	130C
	TSD_ORD_LEVEL	0x0	140C	0x0	140C
	I2C1_HS	0x0	Standard, fast or fast+ by default, can be HS-mode by HS-mode controller code.	0x0	Standard, fast or fast+ by default, can be HS-mode by HS-mode controller code.
	I2C2_HS	0x0	Standard, fast or fast+ by default, can be HS-mode by HS-mode controller code.	0x0	Standard, fast or fast+ by default, can be HS-mode by HS-mode controller code.
	EN_ILIM_FSM_CTRL	0x0	Buck/LDO regulators ILIM interrupts do not affect FSM triggers.	0x0	Buck regulators ILIM interrupts do not affect FSM triggers.
	NSLEEP1_MASK	0x0	NSLEEP1(B) affects FSM state transitions.	0x1	NSLEEP1(B) does not affect FSM state transitions.
	NSLEEP2_MASK	0x0	NSLEEP2(B) affects FSM state transitions.	0x1	NSLEEP2(B) does not affect FSM state transitions.
CONFIG_2	BB_CHARGER_EN	0x0	Disabled		
	BB_VEOC	0x0	2.5V		
	BB_ICHR	0x0	100uA		
RECOV_CNT_REG_2	RECOV_CNT_THR	0xf	0xf	0xf	0xf
BUCK_RESET_REG	BUCK1_RESET	0x0	0x0	0x0	0x0
	BUCK2_RESET	0x0	0x0	0x0	0x0
	BUCK3_RESET	0x0	0x0	0x0	0x0
	BUCK4_RESET	0x0	0x0	0x0	0x0
	BUCK5_RESET	0x0	0x0		
SPREAD_SPECTRUM_1	SS_EN	0x0	Spread spectrum disabled	0x0	Spread spectrum disabled
	SS_MODE	0x1	Mixed dwell	0x1	Mixed dwell
	SS_DEPTH	0x0	No modulation	0x0	No modulation

Table 5-11. Miscellaneous NVM Settings (continued)

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
SPREAD_SPECTRUM_2	SS_PARAM1	0x7	0x7	0x7	0x7
	SS_PARAM2	0xc	0xc	0xc	0xc
FREQ_SEL	BUCK1_FREQ_SEL	0x1	4.4 MHz	0x1	4.4 MHz
	BUCK2_FREQ_SEL	0x1	4.4 MHz	0x1	4.4 MHz
	BUCK3_FREQ_SEL	0x1	4.4 MHz	0x1	4.4 MHz
	BUCK4_FREQ_SEL	0x1	4.4 MHz	0x1	4.4 MHz
	BUCK5_FREQ_SEL	0x1	4.4 MHz		
FSM_STEP_SIZE	PFSM_DELAY_STEP	0xb	0xb	0xb	0xb
LDO_RV_TIMEOUT_REG_1	LDO1_RV_TIMEOUT	0xf	16ms		
	LDO2_RV_TIMEOUT	0xf	16ms		
LDO_RV_TIMEOUT_REG_2	LDO3_RV_TIMEOUT	0xf	16ms		
	LDO4_RV_TIMEOUT	0xf	16ms		
USER_SPARE_REGS	USER_SPARE_1	0x0	0x0	0x0	0x0
	USER_SPARE_2	0x0	0x0	0x0	0x0
	USER_SPARE_3	0x0	0x0	0x0	0x0
	USER_SPARE_4	0x0	0x0	0x0	0x0
ESM_MCU_MODE_CFG	ESM_MCU_EN	0x0	ESM_MCU disabled.	0x0	ESM_MCU disabled.
ESM_SOC_MODE_CFG	ESM_SOC_EN	0x0	ESM_SoC disabled.		
RTC_CTRL_2	XTAL_EN	0x1	Crystal oscillator is enabled		
	LP_STANDBY_SEL	0x0	LDOINT is enabled in standby state.	0x0	Normal standby state is used.
	FAST_BIST	0x0	Logic and analog BIST is run at BOOT BIST.	0x0	Logic and analog BIST is run at BOOT BIST.
	STARTUP_DEST	0x3	ACTIVE	0x3	ACTIVE
	XTAL_SEL	0x1	9 pF		
PFSM_DELAY_REG_1	PFSM_DELAY1	0x54	0x54		

5.11 Interface Settings

These settings detail the default interface, interface configurations, and device addresses. These settings cannot be changed after device startup.

Table 5-12. Interface NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
SERIAL_IF_CONFIG	I2C_SPI_SEL	0x0	I2C	0x0	I2C
	I2C1_SPI_CRC_EN	0x0	CRC disabled	0x0	CRC disabled
	I2C2_CRC_EN	0x0	CRC disabled	0x0	CRC disabled
I2C1_ID_REG	I2C1_ID	0x48	0x48	0x4c	0x4C
I2C2_ID_REG	I2C2_ID	0x12	0x12	0x13	0x13

5.12 Multi-Device Settings

These settings detail whether the device is a operating as a primary or secondary in the system. These settings cannot be changed after device startup.

Table 5-13. Multi-Device NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
SPMI_CONFIG_1	SPMI_CRC_EN	0x1	SPMI CRC check enabled	0x1	SPMI CRC check enabled
	SPMI_MODE_SEL	0x1	Primary mode	0x0	Secondary mode
	SPMI_CLK_SEL	0x2	5MHz	0x2	5MHz
SPMI_CONFIG_2	SPMI_IF_SEL	0x0	Debug feature and uses primary logic to implement logical secondary.	0x0	Debug feature and uses primary logic to implement logical secondary.
	SPMI_RETRY_LIMIT	0x3	Three retries in case of error detected	0x3	Three retries in case of error detected
	SPMI_WD_AUTO_BOOT	0x1	SPMI auto boot enabled	0x1	SPMI auto boot enabled
	SPMI_EN	0x1	SPMI enabled	0x1	SPMI enabled
	SPMI_WD_EN	0x1	SPMI WD enabled	0x1	SPMI WD enabled
SPMI_CONFIG_3	SPMI_WD_BOOT_INTERVAL	0x8	0x8	0x8	0x8
	SPMI_WD_RUNTIME_INTERVAL	0x8	0x8	0x8	0x8
SPMI_CONFIG_4	SPMI_WD_RESPONSE_TIMEOUT	0x8	0x8	0x8	0x8
	SPMI_PFSM_RESPONSE_ TIMEOUT	0x8	0x8	0x8	0x8
SPMI_CONFIG_5	SPMI_WD_BOOT_BIST_TIMEOUT	0x8	0x8	0x8	0x8
	SPMI_WD_RUNTIME_BIST_TIMEOUT	0x8	0x8	0x8	0x8
SPMI_CONFIG_6	SPMI_BOOT_DELAY	0x0	0x0	0x0	0x0
SPMI_ID	SPMI_SID	0x5	0x5	0x3	0x3
	SPMI_MID	0x0	0x0	0x0	0x0

5.13 Watchdog Settings

These settings detail the default watchdog addresses. These settings can be changed though I^2C after startup.

Table 5-14. Watchdog NVM Settings

Register Name	Field Name	TPS6594141B-Q1		LP876441B1-Q1	
		Value	Description	Value	Description
WD_THR_CFG	WD_EN	0x1	Watchdog enabled.	0x0	Watchdog disabled.
WD_LONGWIN_CFG	WD_LONGWIN	0xFF	0xFF	0x00	0x00

6 Pre-Configurable Finite State Machine (PFSM) Settings

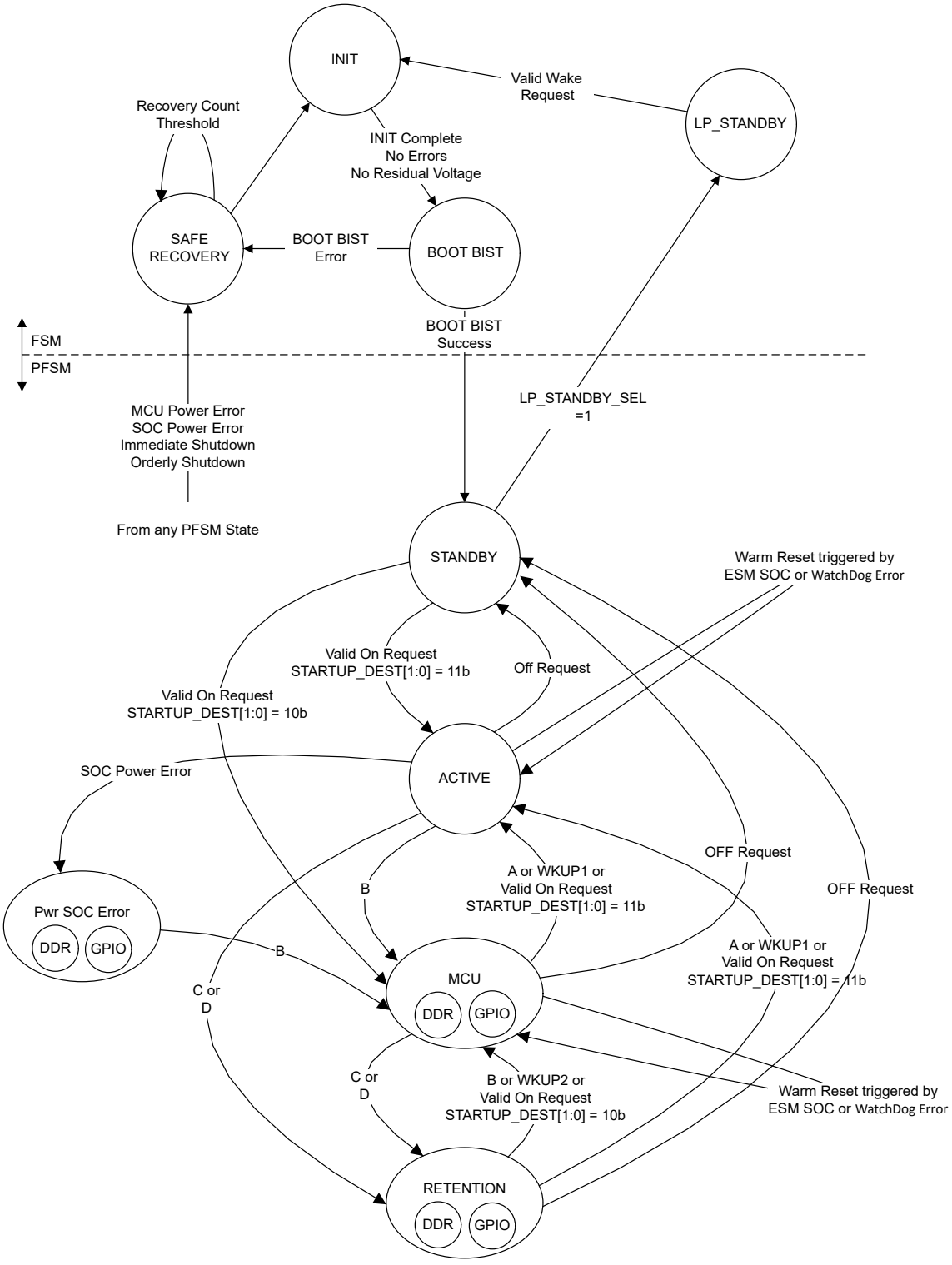
This section describes the default PFSM settings of the TPS6594-Q1 and LP8764-Q1 devices. These settings cannot be changed after device startup.

6.1 Configured States

In this PDN, the following four power states are configured into the PMIC devices:

- Standby
- Active
- MCU Only
- PWR SoC Error
- Retention (both DDR and GPIO retention modes)

In Figure 6-1, the configured power states are described, along with the transition conditions required to move between configured states. Additionally, the transitions to hardware states, such as SAFE RECOVERY are described.



Trigger	NSLEEP2	NSLEEP1
A	1	1
B	1	0
C	0	1
D	0	0

Figure 6-1. Pre-Configurable State Machine (PFSM) States and Transitions

The definition for each power state is described below:

STANDBY The PMICs are powered by a valid supply on the system power rail (VCCA > VCCA_UV) and waiting for a start-up event or condition. All device resources are powered down in the STANDBY state. EN_DRV is forced low in this state. The processor is in the Off State, no voltage domains are energized. Refer to the TO_SAFE_ORDERLY and TO_STANDBY sequence description.

The STANDBY state is also entered when an error occurs and the PMIC transitions out of the PFSM mission states and into the FSM states. When the device returns from the FSM state the to PFSM the first state is represented by STANDBY with all of the resources powered down and EN_DRV forced low. The sequence TO_SAFE_SEVERE is performed before the PMIC leaves the PFSM and enter the FSM state SAFE_RECOVERY.

ACTIVE The PMICs are powered by a valid supply and have received a start-up event. The PMICs have full capacity to supply the processor and other platform modules. The processor has completed a recommended power up sequence with all voltage domains energized in both MCU & Main processor sections. MCU can now set the ENABLE_DRV bit high. Refer to the TO_ACTIVE sequence description.

MCU ONLY The PMICs are powered by a valid supply. Only the power resources assigned to the MCU Safety Island are on. If a given resource is maintained active, then all linked subsystems are automatically maintained active. ENABLE_DRV bit can be set high by the MCU, or remains unchanged in this state. Refer to the TO_MCU sequence description.

Pwr SoC Error The PMICs are powered by a valid supply. Only the power resources assigned to the MCU Safety Island are on. Refer to the PWR_SOC_ERROR sequence description. The only active trigger is 'B', requiring the PMICs to return to the MCU_ONLY mode. The return to MCU_ONLY mode and eventually ACTIVE mode is only recommended after the interrupts which caused the SOC_PWR_ERROR have been cleared.

RETENTION (DDR or GPIO) The PMICs are powered by a valid supply. Only the power resources assigned to the retention rails are on or in LPM depending on the specific resource setting. If a given resource is maintained active, then all linked subsystems are automatically maintained active. ENABLE_DRV bit is cleared by the device in this state. If the I2C_6 bit is set high in both PMICs, they enter GPIO retention state. If the I2C_7 bit is set high in both PMICs, they enter DDR retention state. These bits need to be set by I2C before a trigger for the retention state occurs. Refer to the TO_RETENTION sequence description.

6.2 PFSM Triggers

As shown in Section 6, there are various triggers that can enable a state transition between configured states. Table 6-1 describes each trigger and its associated state transition from highest priority (Immediate Shutdown) to lowest priority (I2C_3). Active triggers of higher priority block triggers of lower priority and the associated sequence.

Table 6-1. State Transition Triggers

Trigger	Priority (ID)	Immediate (IMM)	REENTERANT	PFSM Current State	PFSM Destination State	Power Sequence or Function Executed
Immediate Shutdown(8)	0	True	False	STANDBY, ACTIVE, MCU ONLY, RETENTION	SAFE(1)	TO_SAFE_SEVERE
MCU Power Error	1	True	False	STANDBY, ACTIVE, MCU ONLY, RETENTION	SAFE(1)	TO_SAFE
Orderly Shutdown(8)	2	True	False	STANDBY, ACTIVE, MCU ONLY, RETENTION	SAFE(1)	TO_SAFE_ORDERLY
OFF Request	4	False	False	STANDBY, ACTIVE, MCU ONLY, RETENTION	STANDBY(2)	TO_STANDBY
WDOG Error	5	False	True	ACTIVE	ACTIVE	ACTIVE_TO_WARM
ESM MCU Error	6	False	True	ACTIVE	ACTIVE	

Table 6-1. State Transition Triggers (continued)

Trigger	Priority (ID)	Immediate (IMM)	REENTERANT	PFSM Current State	PFSM Destination State	Power Sequence or Function Executed
ESM SOC Error	7	False	True	ACTIVE	ACTIVE	ESM_SOC_ERROR
WDOG Error	8	False	True	MCU ONLY	MCU ONLY	MCU_TO_WARM
ESM MCU Error	9	False	True	MCU ONLY	MCU ONLY	ESM_ERROR
SOC Power Error(8)	10	False	False	ACTIVE	Pwr SoC Error	PWR_SOC_ERR
I2C_1 bit is high(3)	11	False	True	ACTIVE, MCU ONLY	No State Change	Execute RUNTIME BIST
I2C_2 bit is high(3)	12	False	True	ACTIVE, MCU ONLY	No State Change	Enable I^2C CRC on I^2C1 and I^2C2 on all devices.(4)
ON Request	13	False	False	STANDBY, ACTIVE, MCU ONLY, RETENTION	ACTIVE	TO_ACTIVE
WKUP1 goes high	14	False	False	STANDBY, ACTIVE, MCU ONLY, RETENTION	ACTIVE	
NSLEEP1 and NSLEEP2 are high(5)	15	False	False	STANDBY, ACTIVE, MCU ONLY, RETENTION	ACTIVE	
MCU ON Request	16	False	False	STANDBY, ACTIVE(7), MCU ONLY, RETENTION	MCU ONLY	TO_MCU
WKUP2 goes high	17	False	False	STANDBY, ACTIVE, MCU ONLY, RETENTION	MCU ONLY	
NSLEEP1 goes low and NSLEEP2 goes high(5)	18	False	False	ACTIVE, MCU ONLY, RETENTION	MCU ONLY	
NSLEEP1 goes low and NSLEEP2 goes low(5)	19	False	False	ACTIVE, MCU ONLY	Suspend-to-RAM	TO_RETENTION
NSLEEP1 goes high and NSLEEP2 goes low(5)	20	False	False	ACTIVE, MCU ONLY	Suspend-to-RAM	
I2C_0 bit goes high(3)	21(9)	False	False	STANDBY, ACTIVE, MCU ONLY	LP_STANDBY(2)	TO_STANDBY
I2C_3 bit goes high(3)	22(9)	False	False	ACTIVE, MCU ONLY	No State Change	Devices are prepared for OTA NVM update.(6)

(1) From the SAFE state, the PFSM automatically transitions to the hardware FSM state of SAFE_RECOVERY. From the SAFE_RECOVERY state, the recovery counter is incremented and compared to the recovery count threshold (see RECOV_CNT_REG_2, in Table 5-11). If the recovery count threshold is reached, then the PMICs halt recovery attempts and require a power cycle. Refer to the data sheet for more details.

(2) If the LP_STANDBY_SEL bit is set in the TPS6594141B-Q1 (see RTC_CTRL_2, in Table 5-11), then the PFSM transitions to the hardware FSM state of LP_STANDBY. When LP_STANDBY is entered, then please use the appropriate mechanism to wakeup the device as determined by the means of entering LP_STANDBY. Refer to the data sheet for more details. LP_STANDBY_SEL in the LP876441B1-Q1 is not applicable to the PFSM triggers.

(3) I2C_0, I2C_1, I2C_2 and I2C_3 are self-clearing triggers.

(4) Enabling the I^2C CRC, enables the CRC on both I2C1 and I2C2, however, the I2C2 is disabled for 2ms after the CRC is enabled. Be aware when using the watchdog Q&A before enabling I^2C CRC. The recommendation is to enable the I^2C CRC first, and then after 2ms, start the watchdog Q&A.

(5) NSLEEP1 and NSLEEP2 of the primary PMIC can be accessed through the GPIO pin or through a register bit. If either the register bit or the GPIO pin is pulled high, the NSLEEPx value is read as a *high* logic level.

(6) After completion of an OTA update, the processor is required to initiate a reset of the PMICs to apply the new NVM settings.

(7) These triggers can originate from either the TPS6594141B or the LP9876441B1.

(8) Trigger IDs 21 and 22 are not available until the NSLEEP bits are masked: NSLEEP2_MASK=NSLEEP1_MASK=1.
(9) Trigger IDs 3, 25, and 26 are enabled and activated by the power sequences. These triggers are used to manage the transition between the PFSM and the FSM.

6.3 Power Sequences

6.3.1 TO_SAFE_SEVERE

The TO_SAFE_SEVERE sequence will shut down all rails without. The sequence immediately ceaseses BUCK switching and enables the pulldown resistors of the BUCKs and LDOs. This is to prevent any damage of the PMICs in case of over voltage on VCCA or thermal shutdown. The timing is illustrated in Figure 6-2.

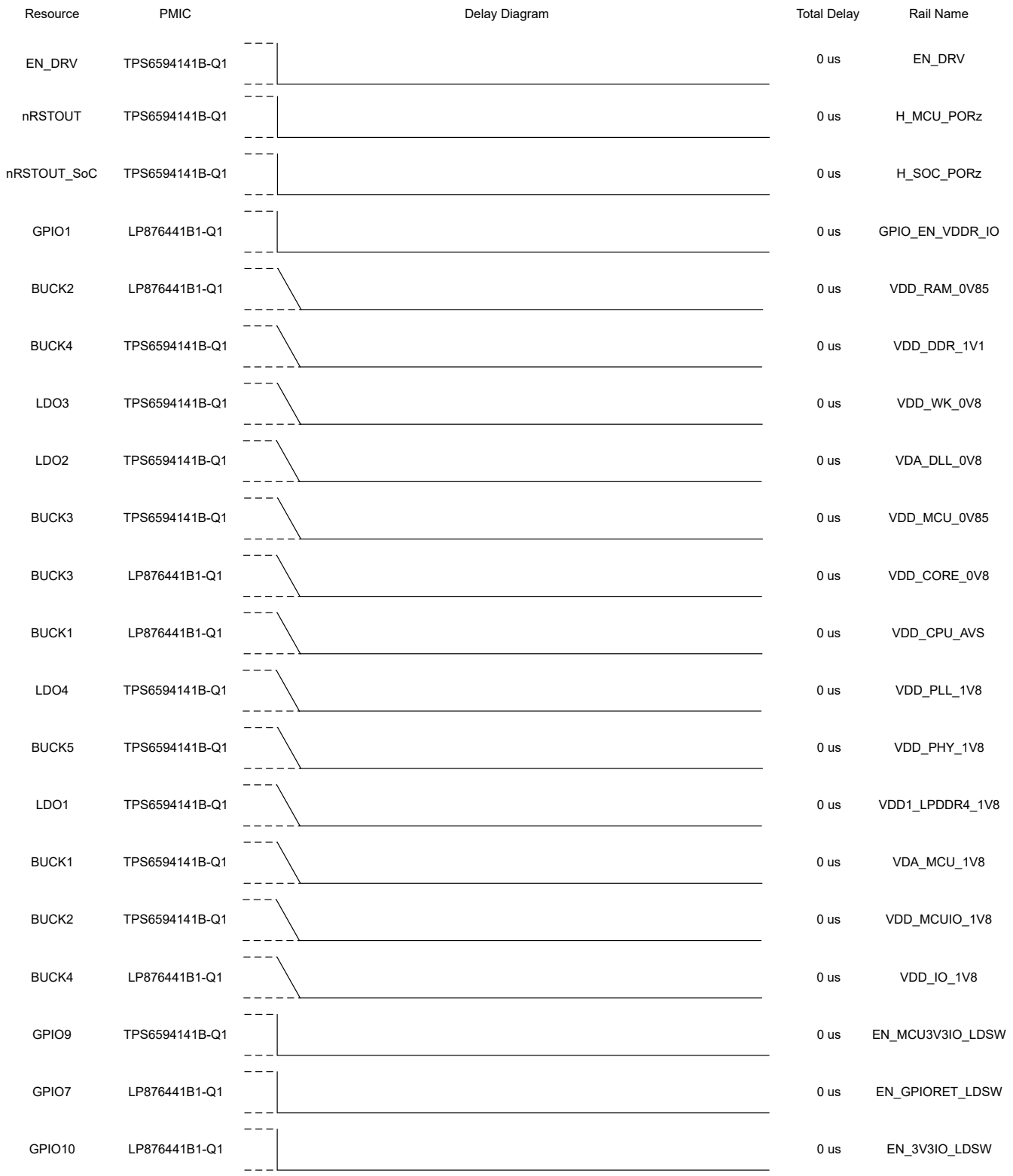


Figure 6-2. TO_SAFE_SEVERE Sequence

6.3.2 TO_SAFE_ORDERLY and TO_STANDBY

If a moderate error occurs, an orderly shutdown trigger is generated. This trigger shuts down the PMIC outputs using the recommended power down sequence and proceed to the SAFE state.

If an OFF request occurs, such as the ENABLE pin of the primary TPS6594-Q1 device being pulled low, the same power down sequence occurs, except that the PMICs go to STANDBY (LP_STANDBY_SEL=0) or

LP_STANDBY (LP_STANDBY_SEL=1) states, rather than going to the SAFE state. The power sequence for both of these events is shown in Figure 6-3.

Both the TO_SAFE_ORDERLY and TO_STANDBY sequences set the SPMI_LP_EN and FORCE_EN_DRV_LOW in the TPS6594141B while only the SPMI_LP_EN is set in the LP876441B1.

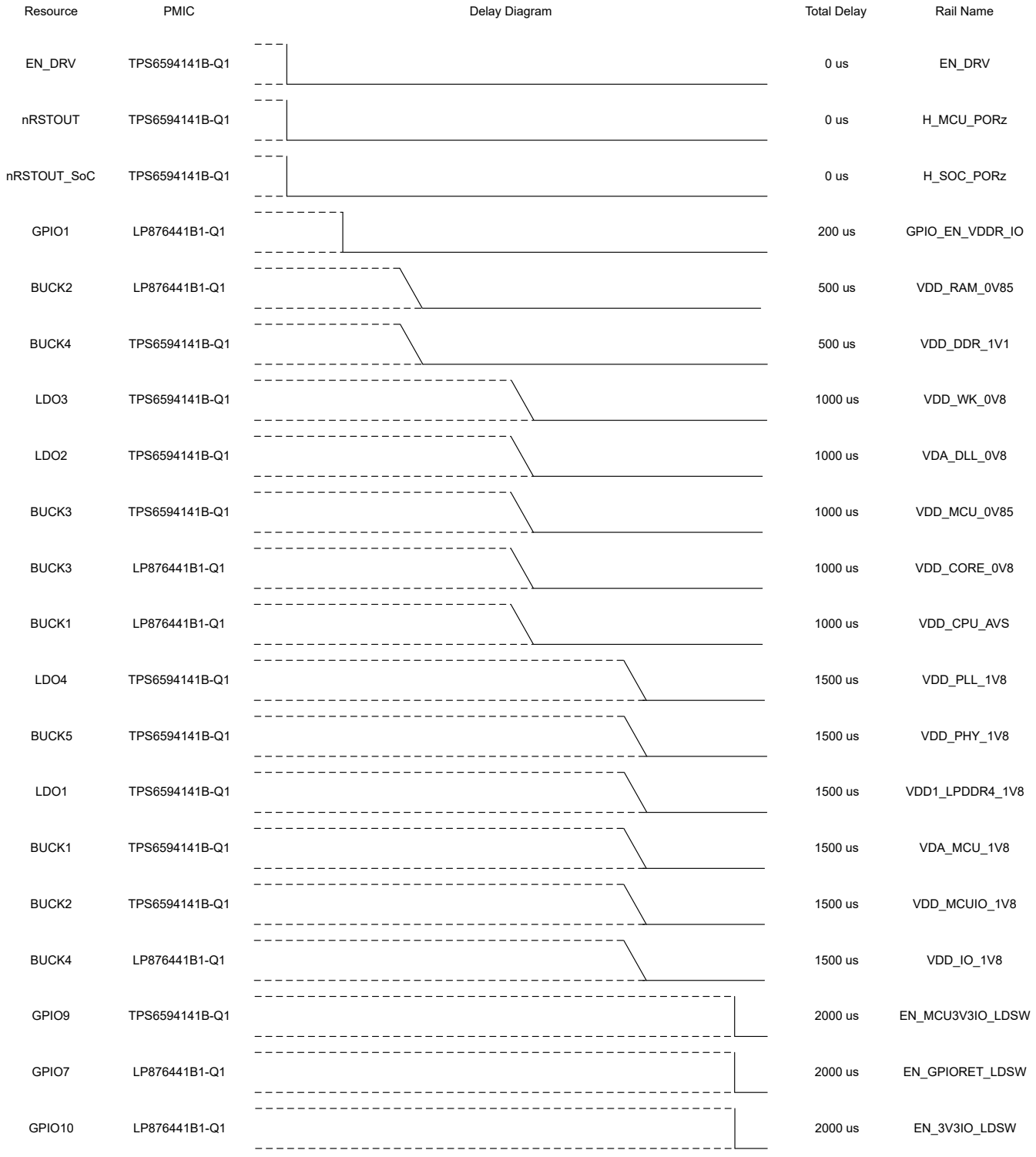


Figure 6-3. TO_SAFE_ORDERLY and TO_STANDBY Sequence

At the end of the TO_SAFE_ORDERLY both PMICs wait approximately 16 ms before executing the following instructions:

```
//TPS6594141B
// Clear AMUXOUT_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x00 MASK=0xEF
// Reset all BUCKs
REG_WRITE_MASK_IMM ADDR=0x87 DATA=0x1F MASK=0xE0
//LP8764418B1
// Reset all BUCKs
REG_WRITE_MASK_IMM ADDR=0x87 DATA=0x0F MASK=0xF0
```

The resetting of the BUCK regulators is done in preparation to transitioning to the SAFE_RECOVERY state. This means that the PMIC leaves the mission state. The SAFE_RECOVERY state is where the recovery mechanism increments the recovery counter and determines if the recovery count threshold is reached before attempting to recover.

At the end of the TO_STANDBY sequence, the 16 ms delay is found in the TPS6594141B device only and the same AMUXOUT_EN, CLKMON_EN, and LPM_EN bit manipulations are made in both PMICs. The BUCKs are not reset. After these instructions, the TPS6594141B performs an additional check to determine if the LP_STANDBY_SEL is true. If true then the PMICs enter the LP_STANDBY state and leave the mission state. If the LP_STANDBY_SEL is false, then the PMICs remain in the mission state defined by STANDBY in Figure 6-1.

6.3.3 ACTIVE_TO_WARM

The ACTIVE_TO_WARM sequence can be triggered by either a watchdog or ESM_MCU error. In the event of a trigger, the nRSTOUT and nRSTOUT_SOC signals are driven low and the recovery count (register RECOV_CNT_REG_1) increments. Then, all BUCKs and LDOs are reset to their default voltages. The PMICs remain in the ACTIVE state.

Note

GPIOs do not reset during the sequence as shown in Figure 6-4.

At the beginning of the sequence the following instructions are executed:

```
//TPS6594141B
// Set FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x08 MASK=0xF7
// Clear nRSTOUT and nRSTOUT_SOC
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x00 MASK=0xFC
// Increment the recovery counter
REG_WRITE_MASK_IMM ADDR=0xa5 DATA=0x01 MASK=0xFE
```

Note

The watchdog or ESM error is an indication of a significant error which has taken place outside of the PMIC. The PMIC does not actually transition through the safe recovery as with an MCU_POWER_ERR, however, in order to maintain consistency all of the regulators are returned to the values stored in NVM and the recovery counter is incremented. If the recovery counter exceeds the recovery count threshold the PMICs stay in the safe recovery state.

Note

After the ACTIVE_TO_WARM sequence the MCU is responsible for managing the EN_DRV and recovery counter. At the end of the sequence the 'FORCE_EN_DRV_LOW' bit is cleared so that the MCU can set the ENABLE_DRV bit.

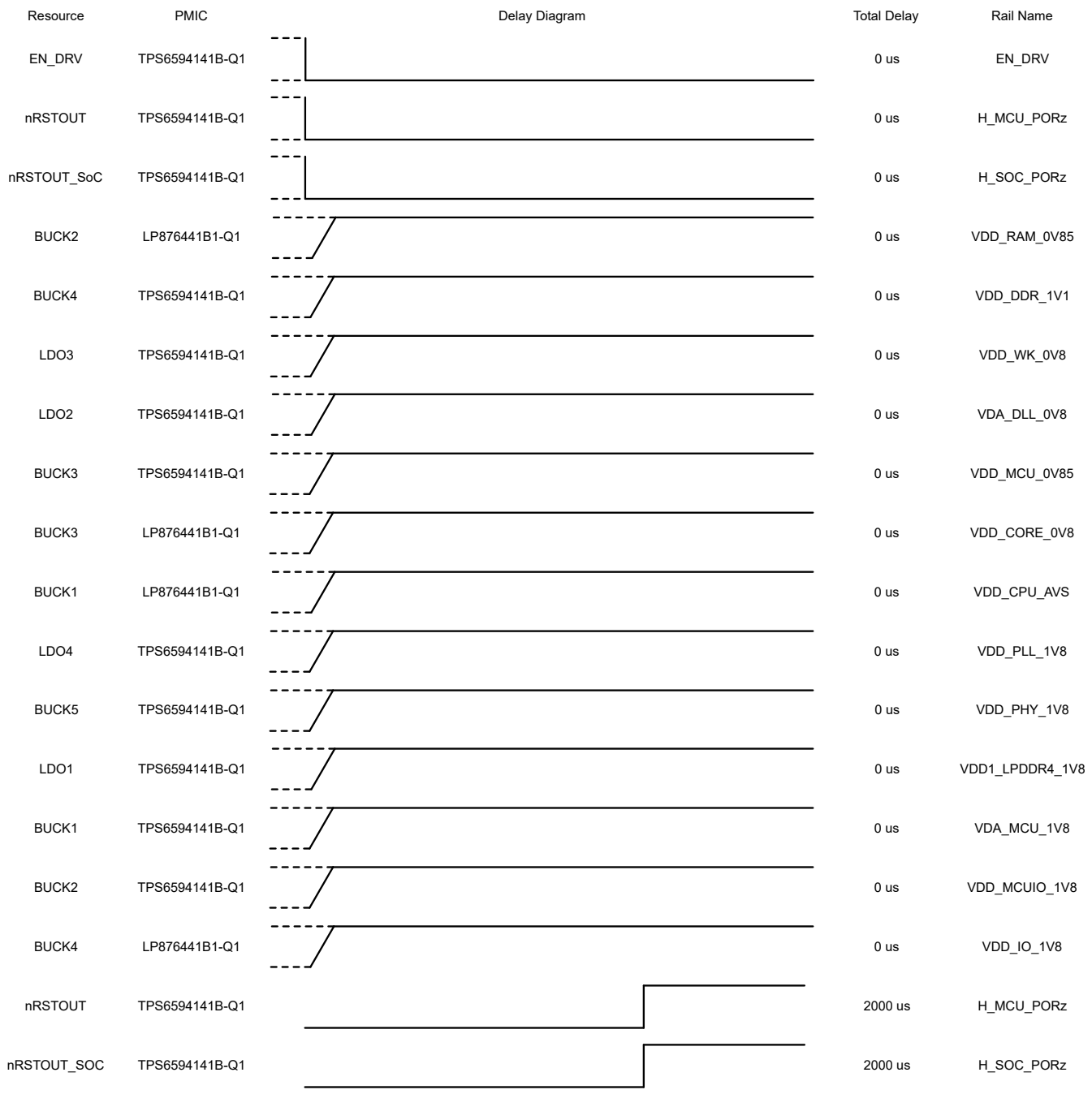


Figure 6-4. ACTIVE_TO_WARM Sequence

Note

The regulator transitions do not represent enabling of the regulators but the time at which the voltages are restored to their default values. Since this sequence originates from the ACTIVE state all of the regulators are on.

6.3.4 ESM_SOC_ERROR

In the event of an ESM_SOC error, the nRSTOUT_SOC signal is driven low and then driven high again after 200 µs. There is no change to the power rails. The sequence is shown in Figure 6-5.

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT_SOC	TPS6594141B-Q1		0 us	SOC_PORz_1V8
nRSTOUT_SOC	TPS6594141B-Q1		200 us	SOC_PORz_1V8

Figure 6-5. ESM_SOC_ERROR Sequence

6.3.5 PWR_SOC_ERROR

In the event of an error on any of the power rails which are part of the SOC power rail group, the PWR_SOC_ERROR sequence is performed. The nRSTOUT_SOC pin is pulled low and the SOC power rails execute a normal processor power down sequence except the MCU power group remains energized as shown in Figure 6-6. The state of the I2C_6 and I2C_7 triggers in both PMICs determines whether the IO and DDR supplies and control signals remain energized (I2C_6=1, I2C_7=1) or disabled (I2C_6=0, I2C_7=0), as shown in Figure 6-7.

In the start of the sequence the following instructions are executed:

```
// TPS6594141B
// Set AMUXOUT_EN and CLKMON_EN, clear LPM_EN and nRSTOUT_SOC
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x18 MASK=0xE1
// Clear SPMI_LPM_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x00 MASK=0xEF
//LP876441B1
// Set CLKMON_EN, clear LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x18 MASK=0xE3
// Clear SPMI_LPM_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x00 MASK=0xEF
```

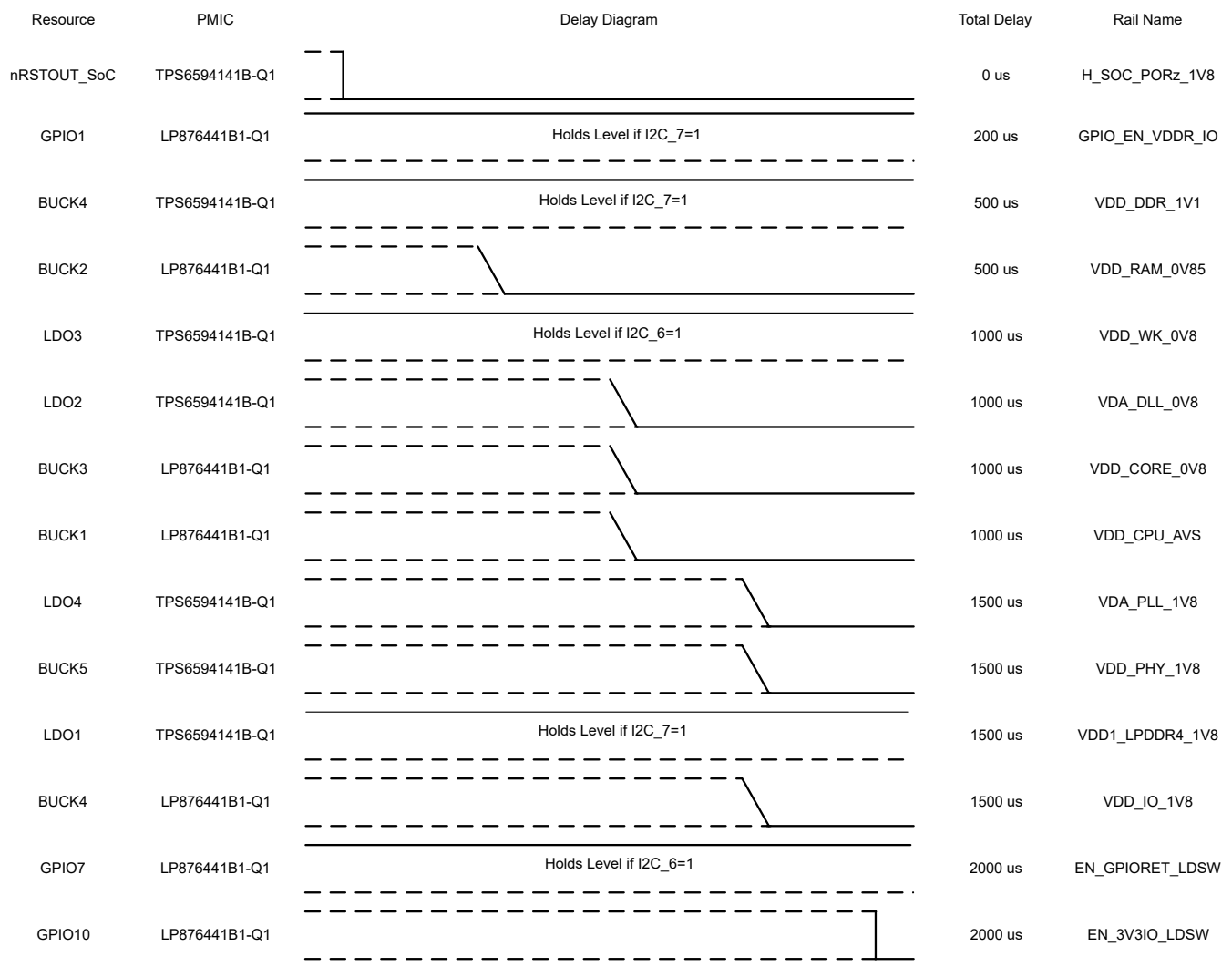


Figure 6-6. PWR_SOC_ERROR with I2C_6 and I2C_7 High in both PMICs

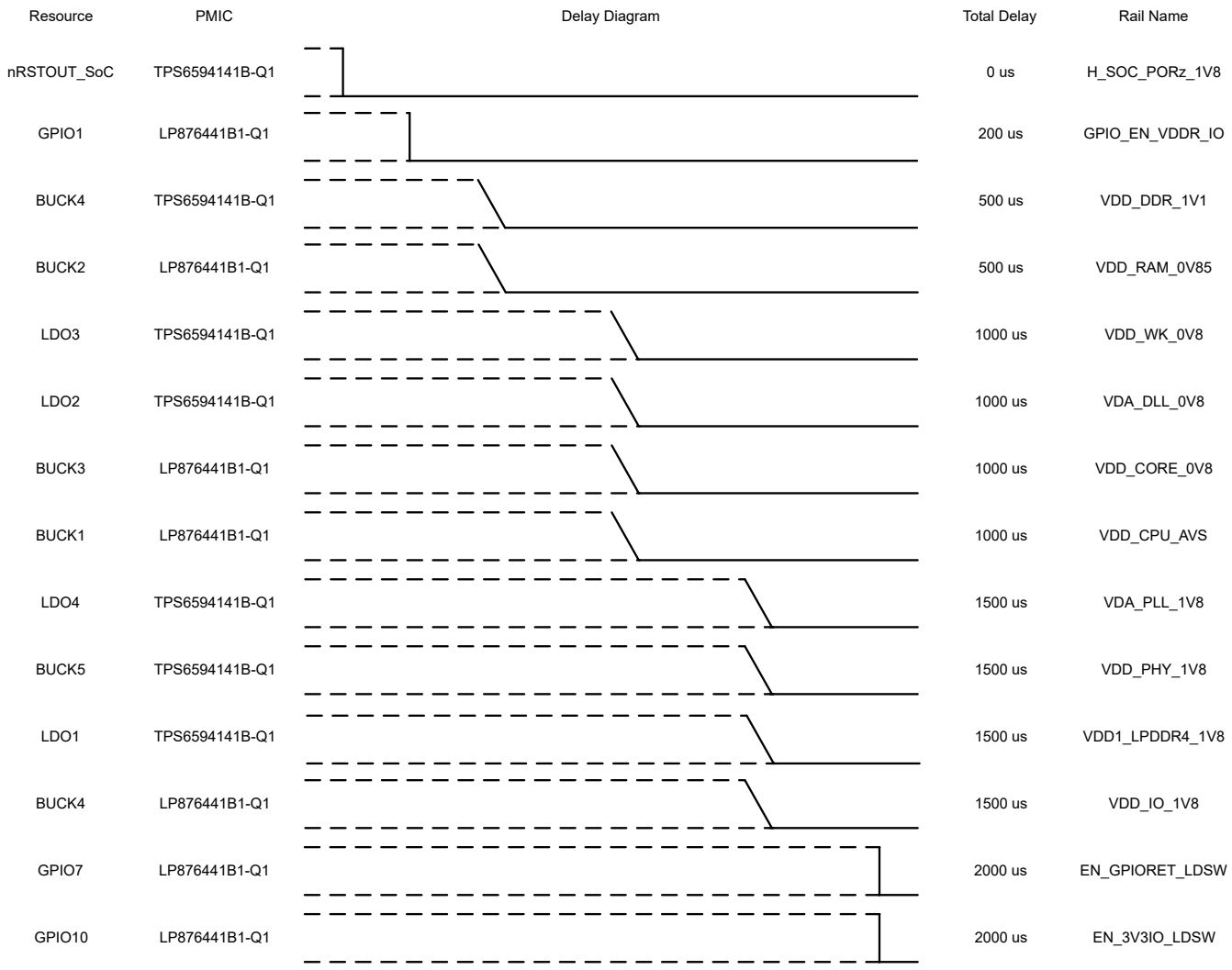


Figure 6-7. PWR_SOC_ERROR with I2C_6 and I2C_7 Low in both PMICs

6.3.6 MCU_TO_WARM

The MCU_TO_WARM, similar to the ACTIVE_TO_WARM sequence does not result in a state change. The event and sequence originate from the MCU_ONLY state and stays in the MCU_ONLY state. In the sequence, the recover counter (found in register, RECOV_CNT_REG_1) is incremented and the nRSTOUT (MCU_PORz) signal is driven low. The MCU relevant BUCK and LDOs are reset to their default voltages at the time indicated in Figure 6-8, and finally nRSTOUT is set high after 2ms. Please note that the GPIOs do not reset during the MCU warm reset event.

Also, at the beginning of the sequence the following instructions are executed to increment the recovery counter and configure the PMICs:

```
// TPS6594141B
// Set FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x08 MASK=0xF7
// Clear nRSTOUT
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x00 MASK=0xFE
// Increment Recovery Counter
REG_WRITE_MASK_IMM ADDR=0xa5 DATA=0x01 MASK=0xFE
```

Note

The watchdog is an indication of a significant error which has taken place outside of the PMIC. The PMIC does not actually transition through the safe recovery as with an MCU_POWER_ERR, however, in order to maintain consistency all of the regulators are returned to the values stored in NVM and the recovery counter is incremented. If the recovery counter exceeds the recovery count threshold the PMICs stay in the safe recovery state.

Note

After the MCU_TO_WARM sequence the MCU is responsible for managing the EN_DRV and recovery counter. At the end of the sequence the 'FORCE_EN_DRV_LOW' bit is cleared so that the MCU can set the ENABLE_DRV bit.

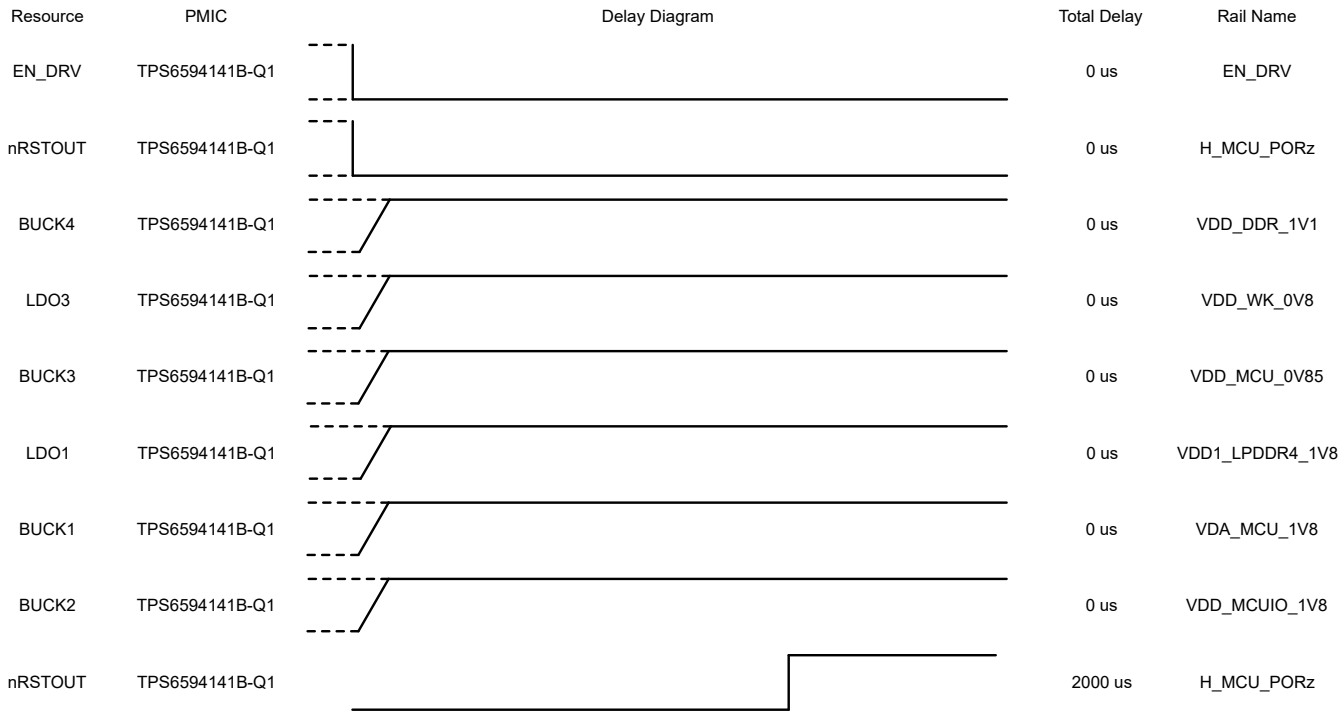


Figure 6-8. MCU_TO_WARM Sequence

Note

The regulator transitions do not represent enabling of the regulators but the time at which the voltages are restored to their default values. Since this sequence originates from the MCU_ONLY state these regulators are on.

6.3.7 TO_MCU

The TO_MCU sequence first turns off rails and GPIOs which are assigned to the SOC power group. The sequence enables the MCU rails, in the event that they are not already active (when transitioning from STANDBY to MCU_ONLY for example). If the I2C_6 bit (FSM_I2C_TRIGGERS register) is set high in both PMICs, the PMICs retain the processor GPIOs while keeping the MCU active as shown in Figure 6-9. If the I2C_7 bit (FSM_I2C_TRIGGERS register) is set high in both PMICs, they retain the SRAM while keeping the MCU active as shown in Figure 6-10. If both bits are set high in both devices, both GPIO and DDR rails are retained while the MCU is active, as shown in Figure 6-11. Lastly, if both I2C_6 and I2C_7 are set low in both devices, only the MCU rails remain active in this state as shown in Figure 6-12. These bits need to be set by I2C in both PMICs before a trigger for the retention state occurs.

Similar to the TO_ACTIVE sequence, the nRSTOUT signal is delayed 9ms after TPS65941B BUCK3 regulator is enabled by default. This delay is always 500us plus the time set by the PFSM_DELAY1 register. This value can be changed before entering the retention state to control when the nRSTOUT pin is released.

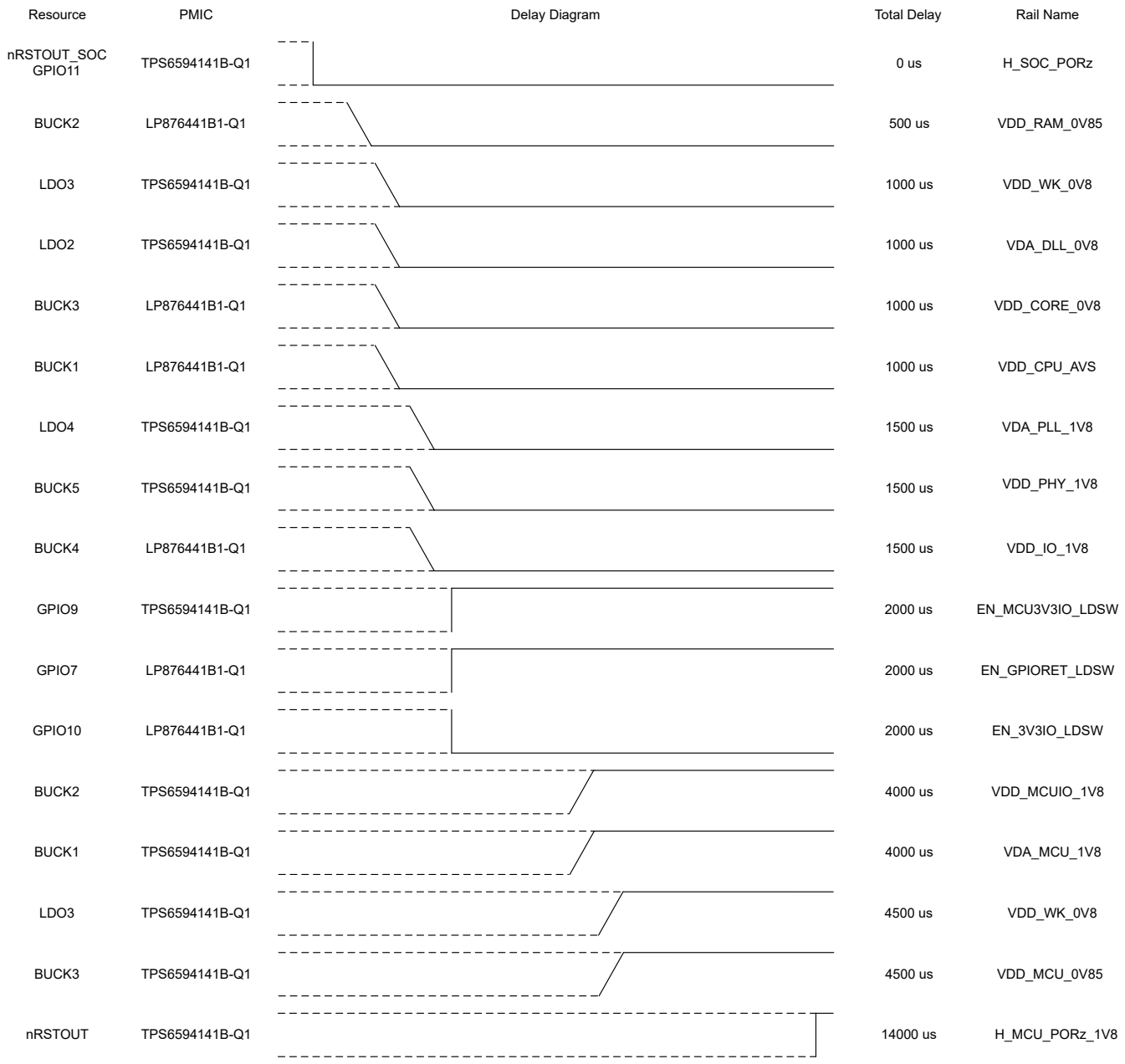


Figure 6-9. TO_MCU Sequence with I2C_6 = 1 and I2C7 = 0 in both PMICs

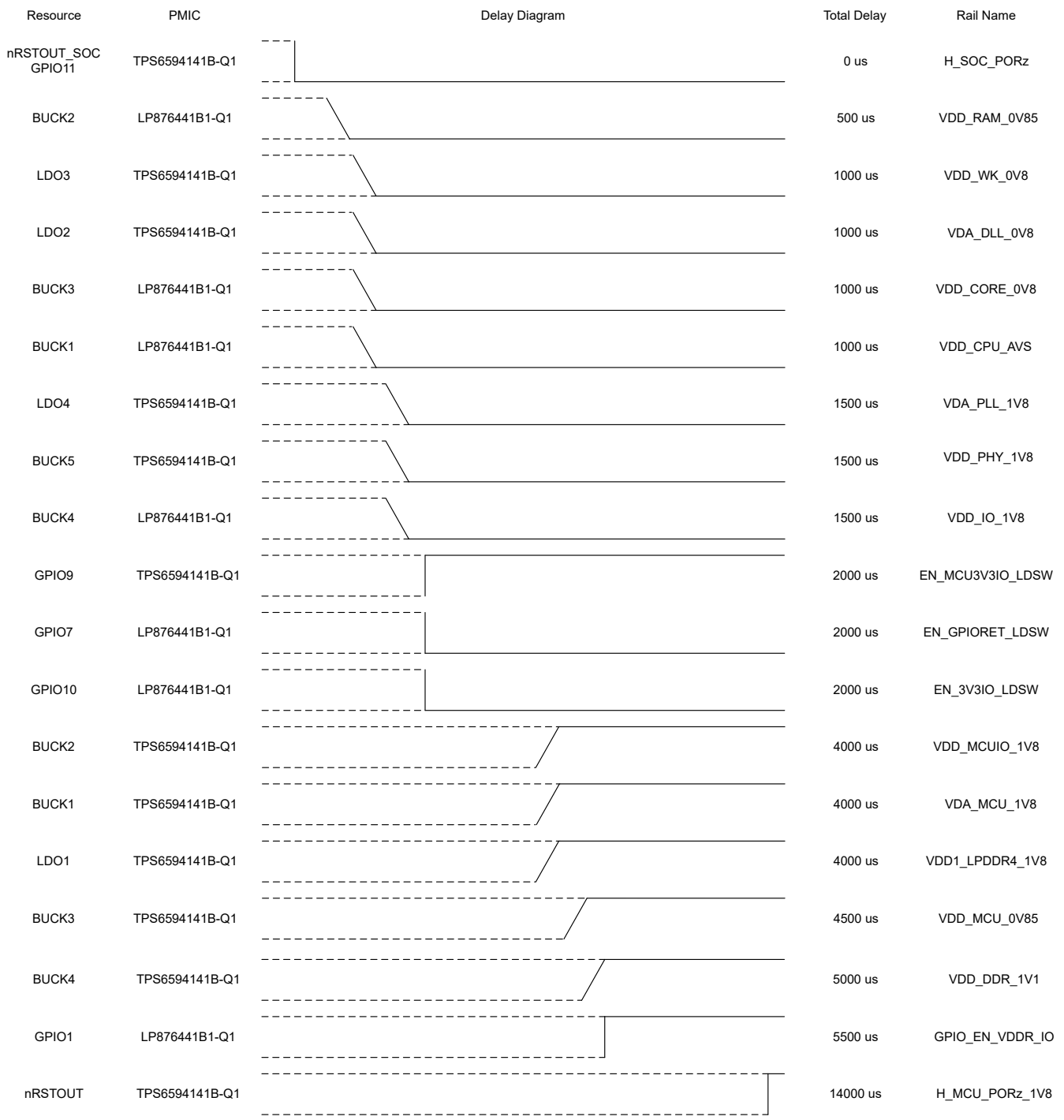


Figure 6-10. TO_MCU Sequence with I2C_6 = 0 and I2C_7 = 1 in both PMICs

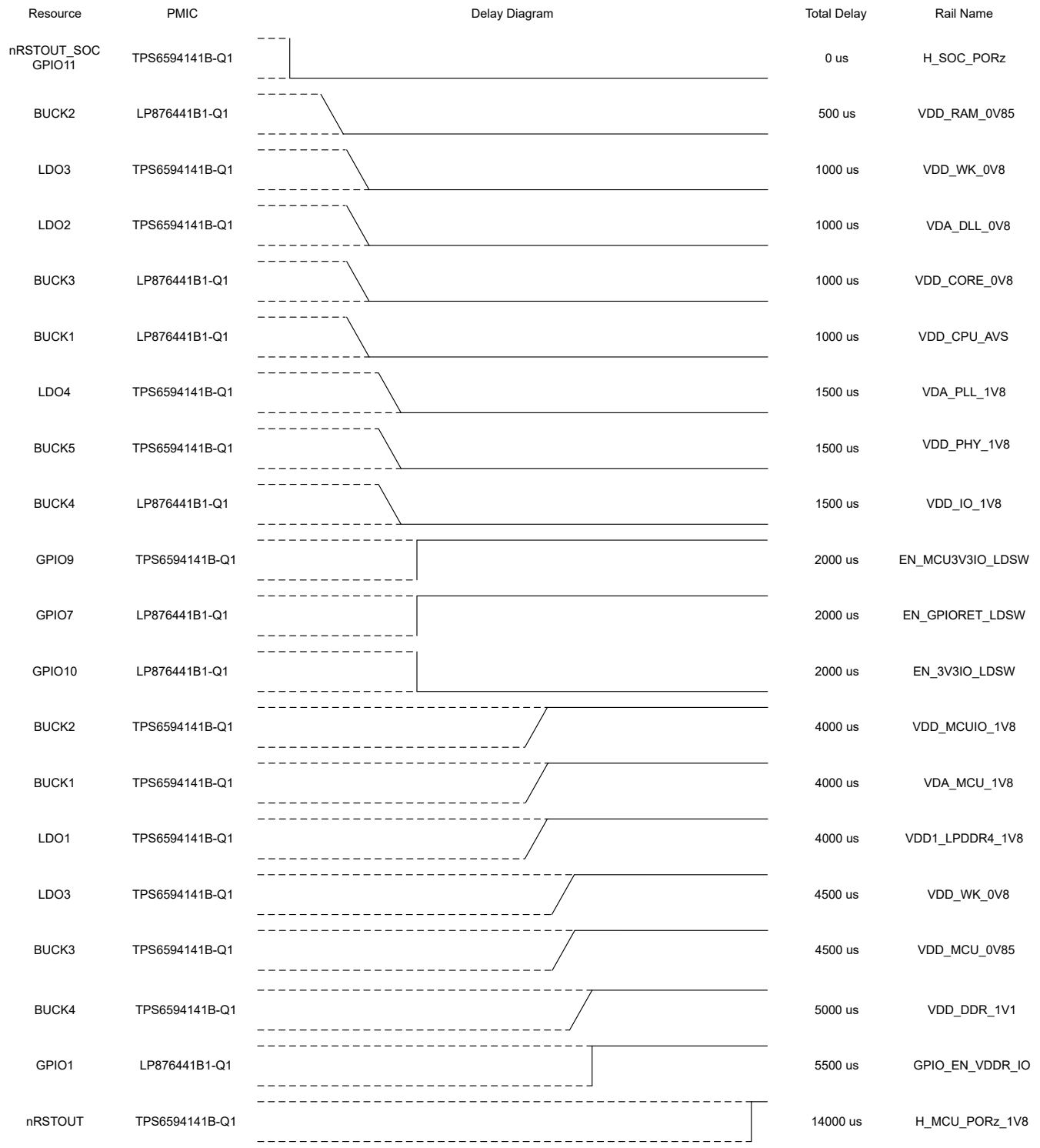


Figure 6-11. TO_MCU Sequence with I2C6 = 1 and I2C_7 = 1 in both PMICs

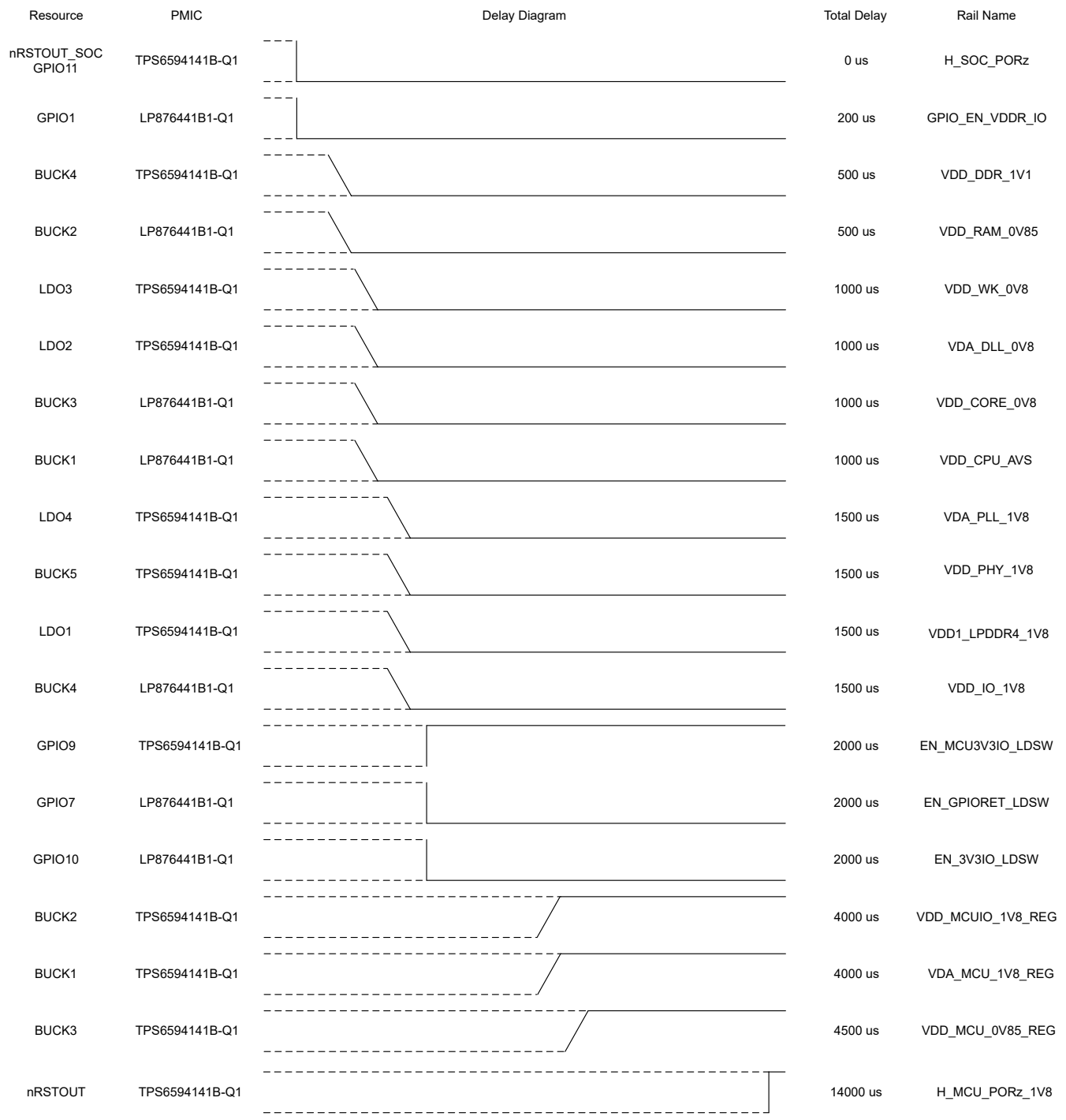


Figure 6-12. TO_MCU Sequence with I2C6 = 0 and I2C_7 = 0 in both PMICs

6.3.8 TO_ACTIVE

When a trigger causes the TO_ACTIVE sequence to execute, all rails power up in the recommended power up sequence as shown in Figure 6-13.

The delay TPS6594141B BUCK4 command and the nRSTOUT_SOC and nRSTOUT signals going high is defined in the PFSM_DELAY_REG_1 register. This delay can be changed at runtime to control how quickly the signals are released after waking up from Retention or MCU_ONLY.

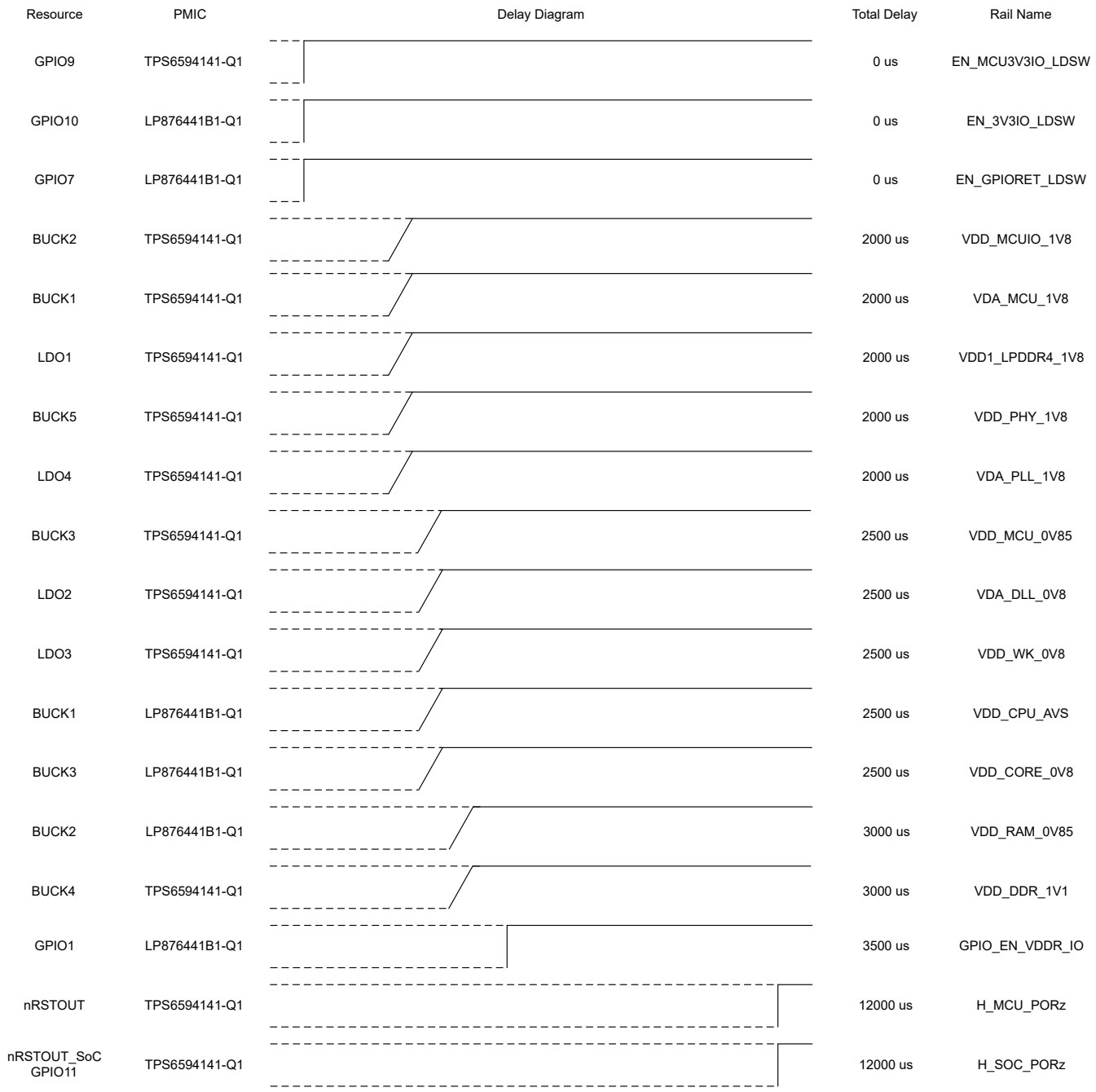


Figure 6-13. TO_ACTIVE Sequence

6.3.9 TO_RETENTION

The C and D triggers, defined by the NSLEEPx bits or pins, trigger the TO_RETENTION sequence. This sequence disables all power rails and GPIOs that are not supply the retention rails. The sequence can by modified using the I2C_6 and I2C_7 bits found in the FSM_I2C_TRIGGERS register. These bits need to be set by I2C in both PMICs before a trigger for the retention state occurs. If the I2C_6 bit is set high in both PMICs, they will enter GPIO retention state as shown in Figure 6-14. If the I2C_7 bit is set high in both PMICs, they will enter DDR retention state as shown in Figure 6-15. If both bits are set, both GPIO and DDR rail will be retained, as shown in Figure 6-16. If neither I2C_6 or I2C_7 are set high, the GPIOs and DDR will not remain active, as shown in Figure 6-17.

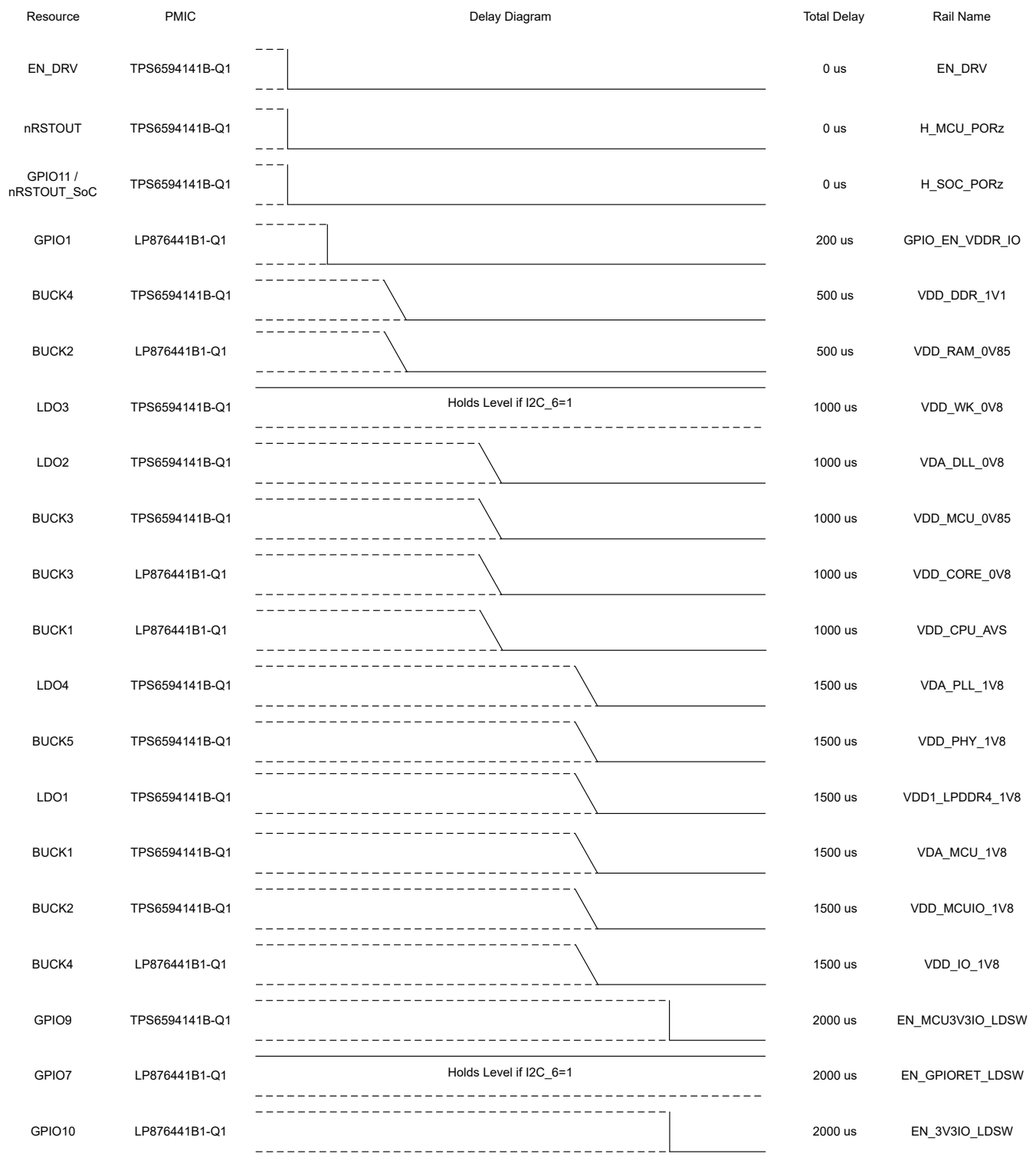


Figure 6-14. TO_RETENTION Sequence, I2C_6 = 1 and I2C_7=0 in both PMICs

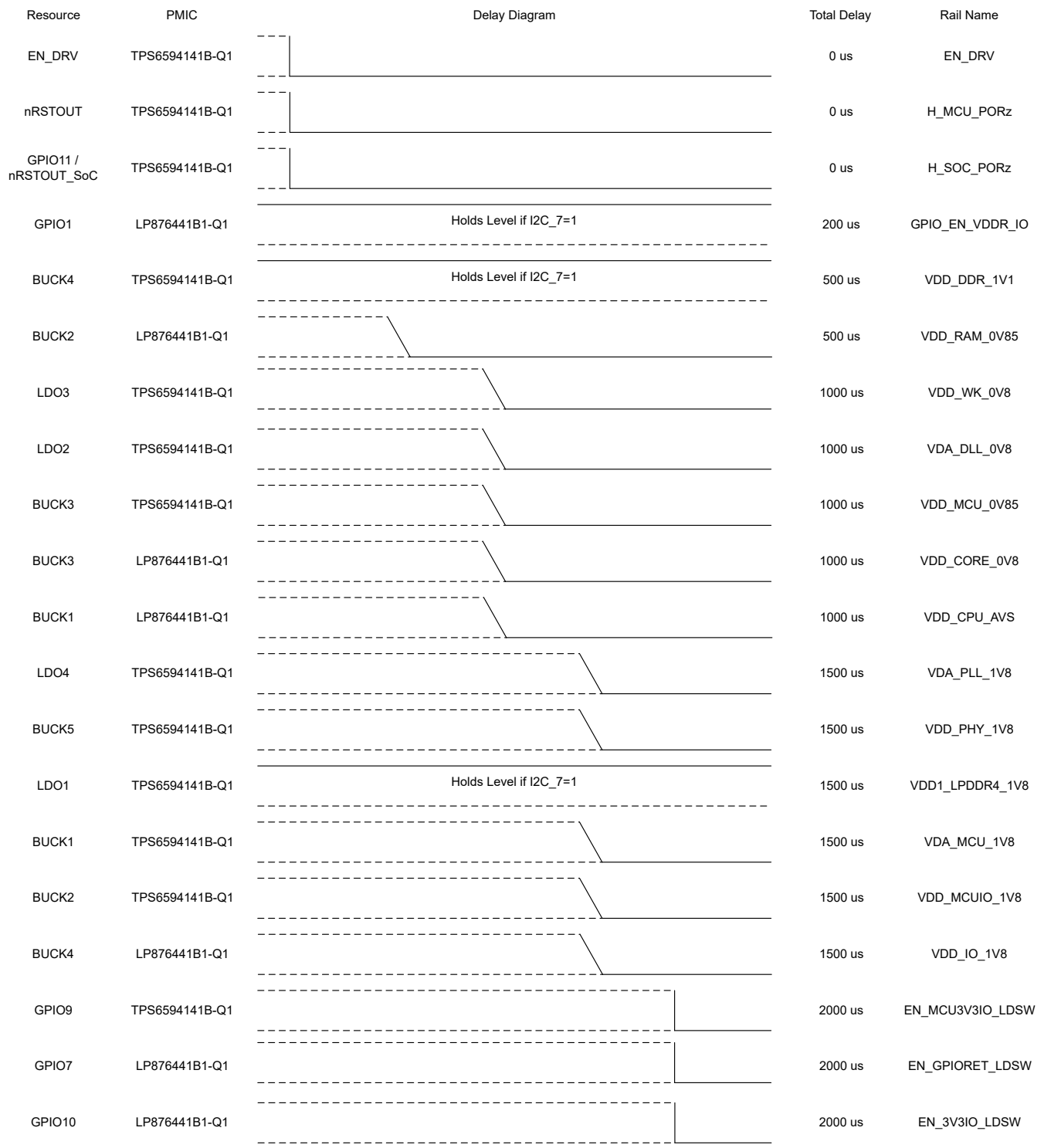


Figure 6-15. TO_RETENTION Sequence, I2C_6=0 and I2C_7 = 1 in both PMICs

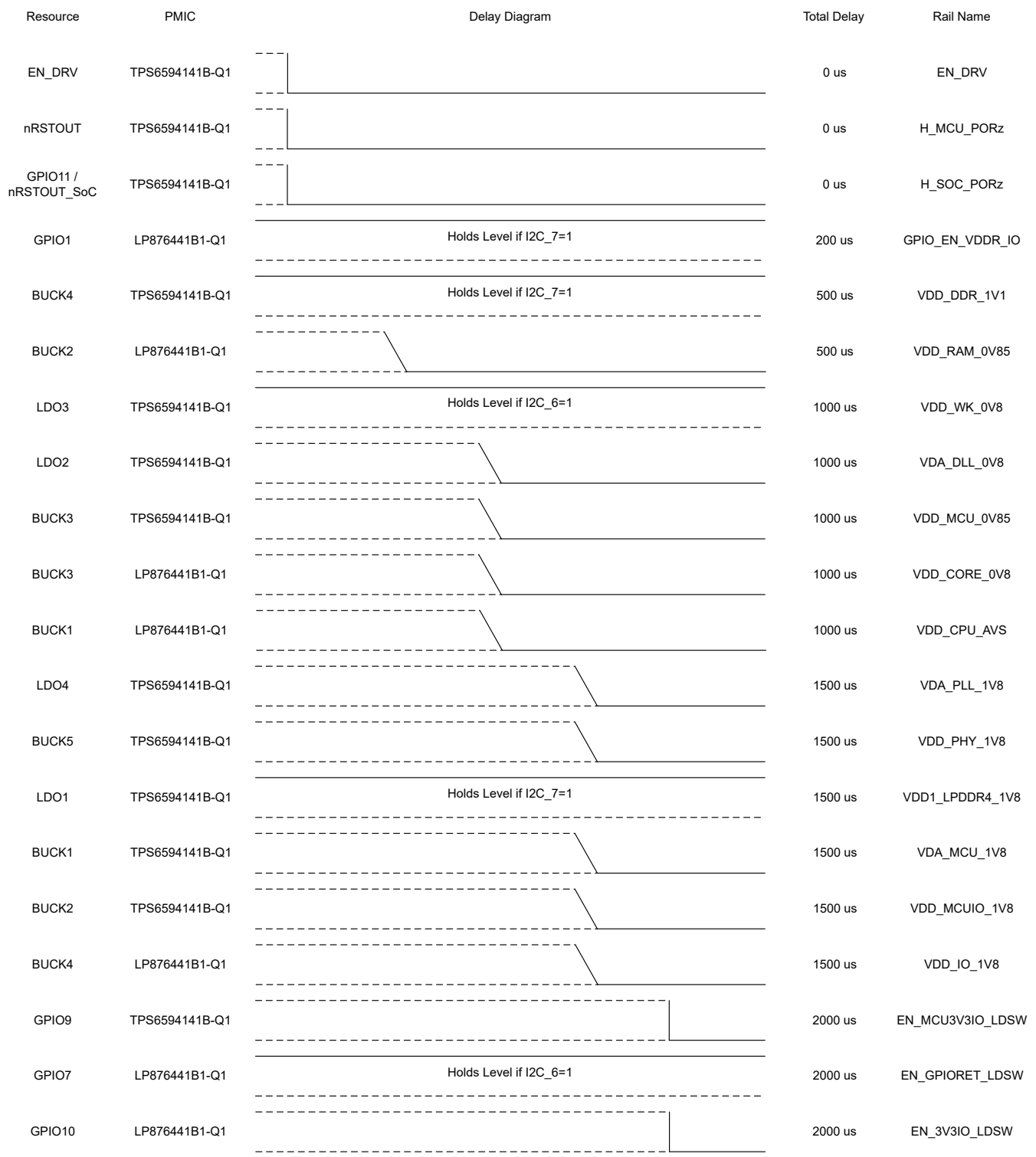


Figure 6-16. TO_RETENTION Sequence, I2C_6 = 1 and I2C_7 = 1 in both PMICs

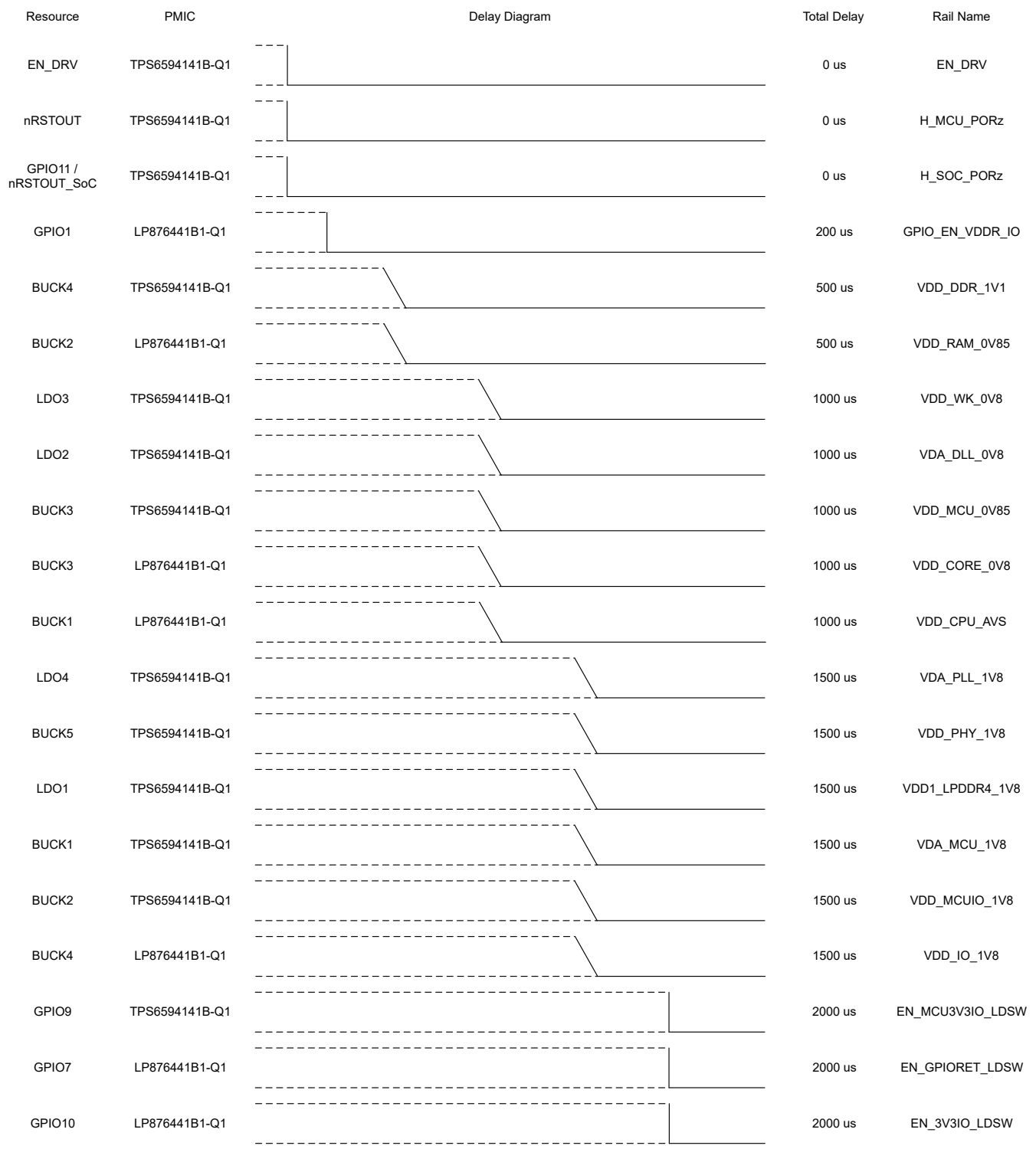


Figure 6-17. TO_RETENTION Sequence, I2C_6 = 0 and I2C_7 = 0 in both PMICs

7 Application Examples

This section provides examples of how to interact with the PMICs from the perspective of the MCU and over I²C. Table 7-1 shows how the I²C commands are presented in the following sections. These examples, when used in conjunction with the data sheet, can be generalized and applied to other use cases.

Table 7-1. I²C Instruction Format

I2C Address	Register Address	Data	Mask
0x48 or 0x4C	0x00 - 0xFF	0x00 - 0xFF	0x00 - 0xFF

7.1 Moving Between States: ACTIVE, MCU, and RETENTION

The default configuration of the NVM transitions the PMICs to the ACTIVE state when the ENABLE pin on the TPS6594141B goes high (rising edge triggered). The nINT pin goes high to indicate to the MCU that interrupts have occurred in the PMICs. After a normal power up sequence the interrupts are the ENABLE_INT and BIST_PASS_INT. The ENABLE_INT prohibits the PMICs from processing any lower priority triggers below the 'ON Request' in Table 6-1. Once the ENABLE_INT is cleared the state is defined by Table 7-2. The following sections describe the I²C commands for transitioning between the different states.

Table 7-2. State Table

NSLEEP1	NSLEEP2	I2C_7	I2C_6	State
1	1	NA	NA	ACTIVE
0	1	0	0	MCU Only
0	1	1	NA	MCU Only with DDR Retention
0	1	NA	1	MCU Only with GPIO Retention
Do not Care	0	1	NA	DDR Retention
	0	NA	1	GPIO Retention
	0	0	0	Retention

7.1.1 ACTIVE

In this example the, PMIC is already in the ACTIVE state after a normal power up event. The PMIC is kept in the ACTIVE state by setting the NSLEEP1 and NSLEEP2 bits before clearing the ENABLE_INT.

```
Write 0x48:0x86:0x03:0xFC    // Set NSLEEP1 and NSLEEP2 in TPS6594141B
Write 0x48:0x66:0x01:0xFE    // Clear BIST_PASS_INT
Write 0x48:0x65:0x26:0xD9    // Clear all potential sources of the On Request
```

7.1.2 MCU ONLY

Transitioning to the MCU ONLY state from the ACTIVE state, requires configuring the I2C_7 trigger before changing the NSLEEP bits. The configuration must be consistent between both PMICs.

```
Write 0x48:0x85:0x80:0x7F    // Set I2C_7 Trigger on TPS6594141B
Write 0x4C:0x85:0x80:0x7F    // Set I2C_7 Trigger on LP876441B1
Write 0x48:0x86:0x02:0xFC    // Set NSLEEP2 to trigger TO_MCU power sequence
```

Instead of writing to the NSLEEP bits to return to the ACTIVE state, it is also possible to use the WKUP1 pin on GPIO4 or GPIO10 to return the PMIC to the ACTIVE state.

7.1.3 RETENTION

As shown in Section 6.3.9, the MCU is powered off and therefore the transition out of the RETENTION to the MCU ONLY or the ACTIVE states must be configured before entering RETENTION. Similar to the MCU

ONLY state the I2C_6 and I2C_7 triggers must be set for both PMICs. Below is an example of entering GPIO RETENTION (I2C_6=1) and using TPS6594141B GPIO4 to wake the PMICs into the ACTIVE state.

```
Write 0x48:0x85:0x40:0x7F    //I2C_6 is high
Write 0x4C:0x85:0x40:0x7F
Write 0x48:0x34:0xC0:0x3F    //Set GPIO4 to WKUP1 (goes to ACTIVE state)
Write 0x48:0x64:0x08:0xF7    //clear interrupt for GPIO4 falling edge
Write 0x48:0x4F:0x00:0xF7    //unmask interrupt for GPIO4 falling edge
Write 0x48:0x86:0x00:0xFC    //trigger the TO_RETENTION power sequence
After the GPIO4 has gone low the the PMICs have returned to the ACTIVE state
Write 0x48:0x86:0x03:0xFC    //Set NSLEEPx bits for ACTIVE state
Write 0x48:0x64:0x08:0xF7    //clear interrupt of GPIO4
```

Below is example of entering DDR RETENTION (I2C_7 = 1) and using the TPS6594141B RTC Timer to wake the PMICs into the ACTIVE state.

```
Write 0x48:0x85:0x80:0x7F     // I2C_7 is high
Write 0x4C:0x85:0x80:0x7F
Write 0x48:0xC3:0x01;0xFE     // Enable Crystal
Write 0x48:0xC5:0x05:0xF8     // minute timer, enable TIMER interrupts
Write 0x48:0xC2:0x01:0xFE     // start timer, if the timer values are non-zero clear before starting
Write 0x4C:0x3D:0x06:0xF9     // set PMICB:GPIO2 and GPIO3
Write 0x48:0x86:0x00:0xFC     // trigger the TO_RETENTION power sequence
After the RTC Timer interrupt has occurred and the PMICs have returned to the ACTIVE state
Write 0x48:0x86:0x03:0xFC     // Set NSLEEPx bits for ACTIVE state
Write 0x48:0xC5:0x00:0xFB     // disable timer interrupt, clear bit 2
Write 0x48:0xC4:0x00:0xDF     // clear timer interrupt, clear bit 5
Write 0x4C:0x3D:0x00:0xF7     // clear PMICB:GPIO2 and GPIO3
```

7.2 Entering and Exiting Standby

STANDBY can be entered from ACTIVE, MCU ONLY, or the RETENTION states. In order to stay in the mission state of STANDBY and not enter the hardware state LP_STANDBY the LP_STANDBY_SEL bit must be cleared.

Similar to the RETENTION state the STANDBY state turns off all regulators which power the MCU. Therefore, it is required to select the state, MCU ONLY or ACTIVE, that the STANDBY state returns to.

When the ENABLE pin goes low, the TO_STANDBY sequence is triggered. When the ENABLE pin goes high again, the destination state is dependent upon the STARTUP_DEST bits. For the TPS6594141B, the STARTUP_DEST must be set for the ACTIVE state. The TO_STANDBY sequence is also triggered by the I2C_0 trigger. When triggered from I2C_0 the PMIC can be triggered to return to the ACTIVE state by GPIO4 or the RTC timer or alarm. In this example, I2C_0 trigger is used to enter the STANDBY state and the GPIO4 is used to enter the ACTIVE state.

```
Write 0x48:0xC3:0x00:0xF7  // LP_STANDBY_SEL=0
Write 0x48:0x7D:0xC0:0x3F  // Mask NSLEEP bits
Write 0x48:0x34:0xC0;0x3F  // Set GPIO4 to WKUP1 (goes to ACTIVE state)
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
Write 0x48:0x4F:0x00:0xF7  // unmask interrupt for GPIO4 falling edge
Write 0x48:0x85:0x01:0xFE  // set I2C_0 trigger, trigger TO_STANDBY sequence
After the GPIO4 has gone low and the PMICs have returned to the ACTIVE state
Write 0x48:0x7D:0x00:0x3F  // unmask NSLEEP bits
Write 0x48:0x86:0x03:0xFC  // Set NSLEEPx bits for ACTIVE state
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
```

7.3 Entering and Existing LP_STANDBY

Entering the LP_STANDBY hardware state is the same as entering STANDBY. Exiting LP_STANDBY is different and requires different initializations before entering LP_STANDBY. Also, when the PMIC returns from LP_STANDBY the PFSM triggers are gated by the ENABLE_INT while in STANDBY the triggers were gated by the GPIO interrupt.

```
Write 0x48:0xC3:0x08:0xF7  // LP_STANDBY_SEL=1
Write 0x48:0x7D:0xC0:0x3F  // Mask NSLEEP bits
Write 0x48:0x34:0xC0;0x3F  // Set GPIO4 to WKUP1 (goes to ACTIVE state)
Write 0x48:0xC3:0x60;0x9F  // Set the STARTUP_DEST=ACTIVE
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
Write 0x48:0x4F:0x00:0xF7  // unmask interrupt for GPIO4 falling edge
```

```
Write 0x48:0x85:0x01:0xFE  // set I2C_0 trigger, trigger TO_STANDBY sequence
After the GPIO4 has gone low and the PMICs have returned to the ACTIVE state
Write 0x48:0x7D:0x00:0x3F  // unmask NSLEEP bits
Write 0x48:0x86:0x03:0xFC  // Set NSLEEPx bits for ACTIVE state
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
Write 0x48:0x65:0x02:0xFD  // clear ENABLE_INT
```

7.4 GPIO8 and Watchdog

The TPS6594141B GPIO8 is configured as an input to disable the watchdog. Typically, during development this pin is tied high, so that when the nRSTOUT bit is set WD_PWRHOLD is also set. The configuration of this pin can be utilized for other features or functions but this requires servicing the watchdog before it expires. The watchdog long window is 772 seconds.

```
Write 0x12:0x09:0x00:0xBF // Disable Watchdog
Write 0x48:0x38:0x01:0x00 // configure GPIO8 as a pushpull output
```

When it is time to enable and configure the watchdog, then in addition to enabling the watchdog the WD_PWR_HOLD must be cleared.

```
Write 0x12:0x09:0x00:0xFB // Clear WD_PWRHOLD
Write 0x12:0x09:0x40:0xBF // Enable Watchdog
```

8 Additional Resources

For additional information regarding the PMIC or processor devices, use Table 8-1 for helpful resources:

Table 8-1. Additional Documents

Title	Document Type	Devices	Link
TPS6594-Q1 Power Management IC (PMIC) for Processors with 5 Bucks and 4 LDOs	Data sheet	TPS6594-Q1	Link
LP8764-Q1 Four Phase, 20-A Buck Converter with Integrated Switches	Data sheet	LP8764-Q1	Link
Jacinto™ DRA821 Automotive Processors Silicon	Data sheet	DRA821	Link
TPS6594-Q1 Safety Manual	Safety Manual	TPS6594-Q1	Request through mySecure
LP8764-Q1 Safety Manual	Safety Manual	LP8764-Q1	Request through mySecure
DRA821 Safety Manual Jacinto™ 7 Processors	Safety Manual	DRA821	Request through mySecure
TPS6594-Q1 Schematic PCB Checklist	Application Note	TPS6594-Q1	Link

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2020) to Revision A (October 2022) **Page**

- Orderable part numbers and corresponding TI_NVM_ID and TI_NVM_REV register values were updated..... 2
- Connection figures depict option of using two single load switches. TPS6594-Q1 GPIO9 is now used to enable MCU I/O load switch while GPIO3 is reserved for SOC_SAFETY_ERRORn signal..... 3
- TPS6594 GPIO9 is involved in power sequencing instead of GPIO3..... 29

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