User's Guide

TSW14J59EVM JESD204C Data Capture and Pattern Generator Card

ABSTRACT

This user's guide describes the characteristics, operation, and use of the TSW14J59EVM JESD204C high-speed data capture and pattern generator card. Throughout this user's guide, the abbreviations *EVM*, and the term *evaluation module* are synonymous with the TSW14J59EVM, unless otherwise noted.

Table of Contents

1 Introduction 2
2 Functionality 2
2.1 ADC EVM Data Capture 4
2.2 DAC EVM Pattern Generator 4
3 Hardware Configuration 5
3.1 Power Connections 5
3.2 Switches, Jumpers, and LEDs 5
3.3 LEDs 6
4 Software Start-Up 12
4.1 Installation Instructions 12
4.2 USB Interface and Drivers 12
5 Downloading Firmware 14

List of Figures

Figure 2-1. TSW14J59EVM 2
Figure 2-2. TSW14J59EVM Block Diagram 3
Figure 3-1. Add Configuration Memory Device 9
Figure 3-2. Programming Memory Device 10
Figure 3-3. Config File 11
Figure 4-1. TSW14J59EVM Serial Number 13
Figure 4-2. Hardware Device Manager 13
Figure 5-1. Select ADC or DAC Firmware to be Loaded 14
Figure 5-2. High-Speed Data Converter Pro GUI Top Level 14
Figure 5-3. Select Device Under Test and Operating Mode 15
Figure 5-4. Example When Connected to an ADC12DJ3200EVM Using JMODE30 15
Figure 5-5. GUI Does Not Connect to EVM 16

List of Tables

Table 3-1. Switch Description of the TSW14J59 Device 5
Table 3-2. Jumper Description of the TSW14J59 Device 5
Table 3-3. Power and Configuration LED Description of the TSW14J59 Device 6
Table 3-4. SMA Connectors 6
Table 3-5. FMC+ Connector Description of the TSW14J59 7

Trademarks

1 Introduction

The TI TSW14J59 evaluation module (EVM) is a next-generation pattern generator and data capture card used to evaluate performances of the new TI JESD204C_B device family of high-speed analog-to-digital converters (ADC) and digital-to-analog converters (DAC). For an ADC, by capturing the sampled data over a JESD204C_B interface when using a high-quality, low-jitter clock, and a high-quality input frequency, the TSW14J59 can be used to demonstrate data sheet performance specifications. Using the TI® JESD204C IP core, the TSW14J59 can be dynamically configurable to support lane speeds from 1Gbps to 32Gbps, from 1 to 16 lanes. Together with the accompanying High-Speed Data Converter Pro Graphic User Interface (GUI), the TSW14J59 is a complete system that captures and evaluates data samples from ADC EVMs, generates and sends desired test patterns to DAC EVMs, and perform both tasks at the same time with AFE EVMs (transceiver mode).

2 Functionality

The TSW14J59EVM has a single industry standard FMC+ connector that interfaces directly with TI JESD204B/C ADC, DAC, and AFE EVMs. The FMC+ carrier connector is compatible with the FMC mezzanine connector. When used with an ADC EVM, high-speed serial data is captured, deserialized and formatted by a Xilinx® Kintex® UltraScale® + FPGA. The data is then stored into an external DDR4 memory bank, enabling the TSW14J59 to store up to 1.536G, 16-bit data samples. To acquire data on a host PC, the FPGA reads the data from memory and transmits on a high-speed 32-bit parallel interface. An on-board high-speed USB 3.0 to parallel converter bridges the FPGA interface to the host PC and GUI.

In pattern generator mode, the TSW14J59 generates the desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14J59. The FPGA stores the data received into the board DDR4 memory module. The data from memory is then read by the FPGA and transmitted to a DAC EVM across the FMC+ interface connector. The board contains two 200-MHz oscillators used to generate the DDR4 reference clock and a general purpose clock. Figure 2-1 shows the TI TSW14J59 evaluation module.

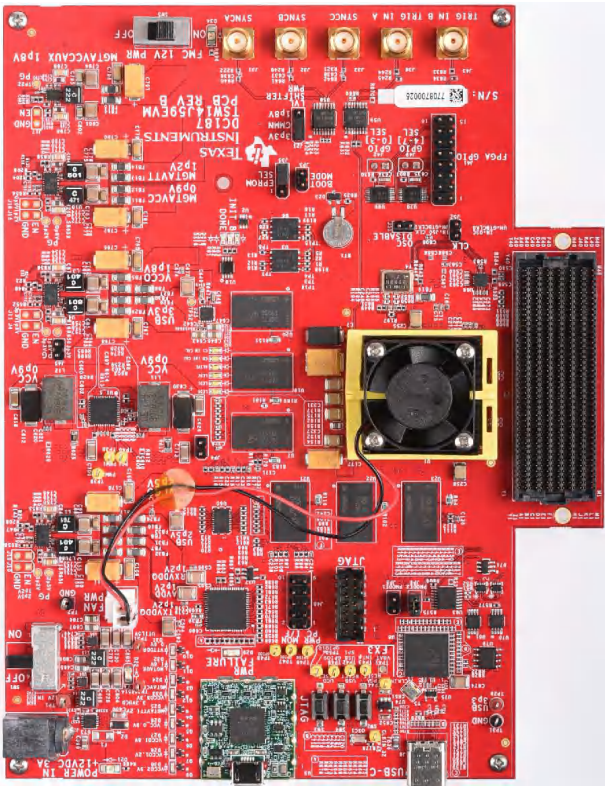

Figure 2-1. TSW14J59EVM

The major features of the TSW14J59 are:

- Backward-compatible with JESD204B (Subclasses: 0, 1, 2)
- Support for deterministic latency
- Serial lanes speeds up to 32Gbps
- 16 routed transceiver channels
- 24Gb DDR4 SDRAM (split into two banks of 3 independent 256 × 16, 4Gb SDRAMs). Quarter rate DDR4 controllers supporting up to 1200-MHz operation
- 1.536G of 16-bit samples of on-board memory
- Supports 1.8-V CMOS IO standard for spare FMC+ signals
- General purpose 200-MHz oscillator
- On-board Cypress USB FX3 USB 3.0 device for parallel interface to the FPGA and general purpose I/O interface to on-board functions and FMC+
- On-board Digilent JTAG SMT2 programmer for FPGA JTAG interface for downloading firmware
- Reference clocking for transceivers available through FMC+ port or SMAs
- Supported by TI HSDC PRO software
- FPGA firmware developed with Xilinx Vivado development tool.
  - TI JESD RX IP core with support for:
    - USB and JTAG reconfigurable JESD core parameters: L, M, K, F, HD, S, and more
    - ILA configuration data accessible through USB and JTAG
    - Lane alignment and character replacement enabled or disabled through USB and JTAG
  - TI JESD TX IP core with support for:
    - USB and JTAG reconfigurable JESD core parameters: L, M, K, F, HD, S, and more
    - ILA configuration data accessible through USB and JTAG
    - Dynamically reconfigurable Transceiver data rate.
  - Serial lane operating range from 1 to 32Gbps

Figure 2-2 shows a block diagram of the TSW14J59 EVM.

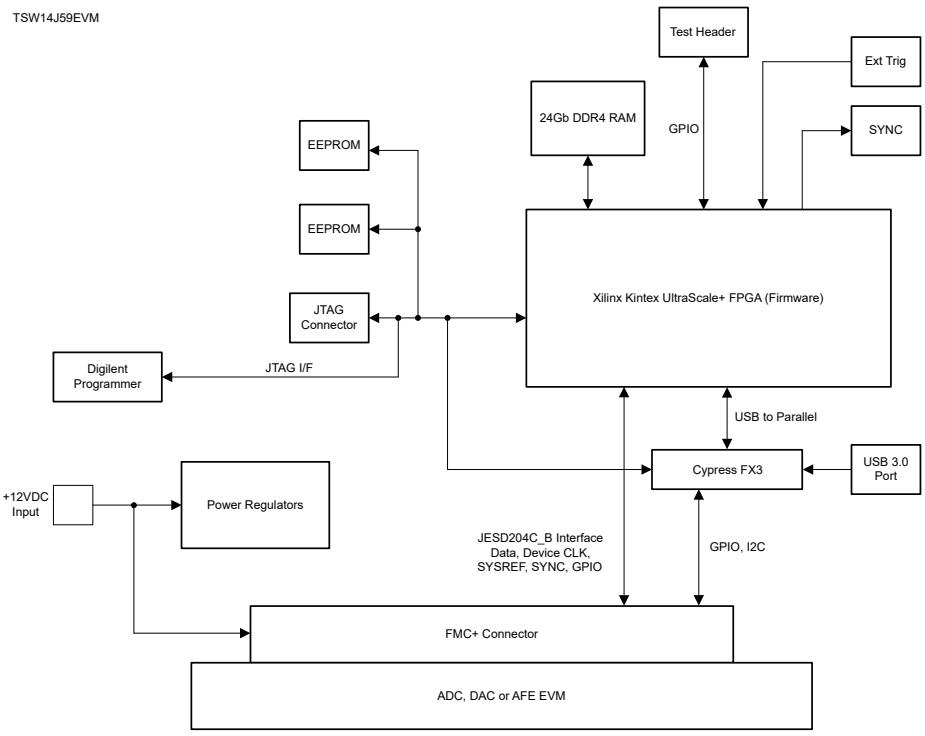

Figure 2-2. TSW14J59EVM Block Diagram

2.1 ADC EVM Data Capture

New TI high-speed ADCs and DACs now have high-speed serial data that meets the JESD204C_B standard. These devices are generally available on an EVM that connects directly to the TSW14J59EVM. The common connector between the EVMs and the TSW14J59EVM is a Samtec high-speed, high-density FMC+ connector (ASP-184329-01) designed for high-speed differential pairs up to 32.5 Gbps. A common pinout for the connector across a family of EVMs has been established. At present, the interface between the EVMs and the TSW14J59EVM has defined connections for 32 high-speed differential data pairs (16 RX and 16 TX), I2C interface, 20 single-ended spare signals, three single-ended SYNC outputs, two single-ended trigger inputs, a differential SYNC and SYSREF, and four device clock pairs (FPGA reference clock). The board has 10 spare USB3.0 interface signals, two FPGA reference clock SMAs, three reset switches, 8 general status LEDs and 13 power status LEDs.

The data format for JESD204C_B ADCs and DACs is a serialized format, where individual bits of the data are presented on the serial pairs commonly referred to as lanes. Devices designed around the JESD204C_B specification can have up to 16 lanes for transmitting or receiving data. The firmware in the FPGA on the TSW14J59 is designed to accommodate any of TI's ADC or DAC operating with any number of lanes from 1 to 16.

The HSDC Pro GUI loads the FPGA with the appropriate firmware and a specific JESD204C_B configuration, based on the ADC device selected in the device drop down window. Each ADC device that appears in this window has an initialization file (.csv) associated. This file contains JESD information, such as number of lanes, number of converters, octets per frame, and other parameters. This information is loaded into the FPGA registers after the user clicks on the capture button. After the parameters are loaded, synchronization is established between the data converter and FPGA and valid data is then captured into the on-board memory. See the *High-Speed Data Capture Pro GUI Software User's Guide* under the Technical Documents section for more information. Several .ini files are available to allow the user to load predetermined ADC JESD204C_B interfaces.

The TSW14J59 device can capture up to 1.536G 16-bit samples at a maximum line rate of 32Gbps that are stored inside the on-board DDR4 memory. The data size the user sets in the HSDC Pro GUI must be entered as multiples of 480. To acquire data on a host PC, the FPGA reads the data from memory and transmits parallel data to the on-board high-speed parallel-to-USB3.0 converter.

2.2 DAC EVM Pattern Generator

In pattern generator mode, the TSW14J59EVM generates desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14J59. The FPGA stores the data received into the on-board DDR4 memory. The data from the memory is then read by the FPGA, converted to JESD204C_B serial format, then transmitted to a DAC EVM. The TSW14J59 can generate patterns up to 1.536G 16-bit samples at a line rate up to 32Gbps.

The HSDC Pro GUI comes with several existing test patterns that can be download immediately. Like the ADC capture mode, the DAC pattern generator mode uses information from the .csv file to load predetermined JESD204C_B interface information to the FPGA.

3 Hardware Configuration

This section describes the various portions of the TSW14J59EVM hardware.

3.1 Power Connections

The TSW14J59EVM hardware is designed to operate from a single supply voltage of +12 V DC at 4 Amps. The power input is controlled by the on and off switch, SW1. 12 V is enabled on the FMC+ using switch SW5. Make sure both switches are in the off position before inserting the provided power cable. Insert the connector end of the power cable into J38 of the EVM. The board can also be powered up by providing +12 V DC to the red test point, TP1, and the return to any black GND test point.

Note

The typical power supply range for the TSW14J59EVM is 12 V with a power consumption of about 16.5W. TI recommends that at least a 4A rated supply be provided to the TSW14J59EVM due to the current consumption increase when data is being captured by HSDC Pro.

3.2 Switches, Jumpers, and LEDs

3.2.1 Switches and Push-Buttons

The TSW14J59 contains several switches and push-buttons that enable certain functions on the board. The description of the switches is found in Table 3-1.

Table 3-1. Switch Description of the TSW14J59 Device

Component	Description
SW1	12 V Input power switch
SW2	FPGA reset
SW3	UCD Power monitor reset
SW4	USB reset
SW5	FMC+ 12,V power switch

3.2.2 Jumpers

The TSW14J59 contains several jumpers (JP) and solder jumpers (SJP) that enable certain functions on the board. The description of the jumpers is found in Table 3-2.

Table 3-2. Jumper Description of the TSW14J59 Device

Component	Description	Default
J11	Disables VCCO_3V3 supply when installed	Open
JP5	USB3.0 PMODE1 configuration. With shunt installed, this sets PMODE1 high	Open
JP6	USB3.0 PMODE2 configuration. With shunt installed this sets PMODE2 low	Installed
J19	Disables VCCO_1V2 supply when installed	Open
J4	Disables VCCO_1V8 supply when installed	Open
J16	Disables MGTAVCC_0V9 supply when installed	Open
J15	Disables MGTAVTT_1V2 supply when installed	Open
J17	Disables MGTAVCCAUX_1V8 supply when installed	Open
J10	Disables VCCO_2V5 supply when installed	Open
J21	Output SYNCA/B/C and input TRIG_IN translator voltage level select. With shunt on pins 1–2, voltage is 3.3V. With shunt on pins 2–3, voltage is controlled by TP30.	1 to 2
J28	Buffers U38, U44, U46 enable. With shunt on pins 1–2, U44 is enabled and U38 and U46 are disabled. With shunt on pins 2–3, U44 is disabled and U38 and U46 are enabled.	1 to 2
J29	USB2.0 JTAG MUX enable. With shunt on pins 1–2, MUX is enabled. With shunt on pins 2–3, MUX enable is controlled by USB2.0 device.	2 to 3
J30	U47 buffer enable. With shunt on pins 1–2, U47 is disabled. With shunt on pins 2–3, U47 is enabled.	1 to 2
J34	Status LEDs enable. With shunt on pins 1–2, LEDs are disabled. With shunt on pins 2–3, LEDs are enabled.	1 to 2

Table 3-2. Jumper Description of the TSW14J59 Device (continued)

Component	Description	Default
J35	EPROM select. With shunt on pins 2–3, select is controlled by USB2.0. With shunt on pins 1–2, U3 is selected. With shunt removed, U6 is selected.	2 to 3

3.3 LEDs

3.3.1 Power and Configuration LEDs

Several LEDs are on the TSW14J59 EVM to indicate the presence of power and the state of the FPGA. The description of these LEDs is found in Table 3-3.

Table 3-3. Power and Configuration LED Description of the TSW14J59 Device

Component	Description
D21	On if 12 V is present to board
D22	On if 3.3V is present to UCD power monitor device
D29	On if there is a failure with one or more of the board's power regulators
D34	On if 12 V is present to board and FMC 12 V PWR switch is on
DS16	On after power up and firmware has been loaded
DS17	On after power up
DS18	On when FPGA INIT_B input goes low

3.3.2 Spare LEDs

The TSW14J59EVM has six spare LEDs. These turn on after board powers up.

DS2 – LED0

DS3 – LED1

DS6 – LED2

DS7 – ALIVE

DS19 – CO INT CAL

DS20 - C1 INT CAL

3.3.3 Connectors

3.3.3.1 SMA Connectors

The TSW14J59 has 5 SMA connectors. Table 3-4 defines the connectors:

Table 3-4. SMA Connectors

Component	Connector	Description
J31	SYNCA	3.3V or 1.8V CMOS logic SYNC output from FPGA pin F22. A shunt on pins 1–2 of J21 sets the level to 3.3V (default). A shunt on pins 2-3 sets the level to 1.8V.
J32	SYNCB	3.3V or 1.8V CMOS logic SYNC output from FPGA pin G22. A shunt on pins 1–2 of J21 sets the level to 3.3V (default). A shunt on pins 2-3 sets the level to 1.8V.
J33	SYNCC	3.3V or 1.8V CMOS logic SYNC output from FPGA pin M24. A shunt on pins 1–2 of J21 sets the level to 3.3V (default). A shunt on pins 2-3 sets the level to 1.8V.
J36	TRIG IN A	3.3V or 1.8V CMOS logic trigger input to FPGA pin E26. A shunt on pins 1–2 of J21 sets the level to 3.3V (default). A shunt on pins 2-3 sets the level to 1.8V.
J43	TRIG IN B	3.3V or 1.8V CMOS logic trigger input to FPGA pin L23. A shunt on pins 1-2 of J21 sets the level to 3.3V (default). A shunt on pins 2-3 sets the level to 1.8V.

Note

SYNCA, SYNCB, and SYNCC SMAs are used to provide external SYNC signals from the FPGA. The cables of each SYNC signal have equal length to verify the signal arrives at the same time for all boards using these SYNCs. The TRIG IN A/B SMA connectors can be used to trigger the FPGA from an external source. All five SMAs can use either 3.3V or 1.8V logic CMOS signals. By default, the EVM is setup for 3.3V logic levels. The EVM has on-board translators to set these inputs/outputs to the correct voltage levels for the FPGA.

3.3.3.2 FPGA Mezzanine Card (FMC+) Connector

The TSW14J59 EVM has one connector to allow for the direct plug in of TI JESD204C_B serial interface ADC and DAC EVMs. The specifications for this connector are mostly derived from the ANSI/VITA 57.4 FPGA Mezzanine Card (FMC+) Standard. This standard describes the compliance requirements for a low-overhead protocol bridge between the IO of a mezzanine card and an FPGA processing device on a carrier card. This specification is being used by FPGA vendors on their development platforms.

The FMC+ connector, J3, provides the interface between the TSW14J59EVM and the ADC or DAC EVM under test. This 560-pin Samtec high-speed, high-density connector (part number ASP-184329-01) is an excellent choice for high-speed differential pairs up to 32.5 Gbps.

In addition to the JESD204B/C standard signals, several CMOS single-ended signals and LVDS differential signals are connected between the FMC+ and FPGA. These signals can allow the HSDC Pro GUI to control the SPI serial programming of ADC and DAC EVMs that support this feature. The connector pinout description is shown in Table 3-5.

Table 3-5. FMC+ Connector Description of the TSW14J59

FMC+ Signal Name	FMC+ Pin	Standard JESD204 Application Mapping	Description
DP0_RX_P/N	C6 and C7	Lane 0± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP1_RX_P/N	A2 and A3	Lane 1± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP2_RX_P/N	A6 and A7	Lane 2± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP3_RX_P/N	A10 and A11	Lane 3± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP4_RX_P/N	A14 and A15	Lane 4± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP5_RX_P/N	A18 and A19	Lane 5± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP6_RX_P/N	B16 and B17	Lane 6± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP7_RX_P/N	B12 and B13	Lane 7± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP8_RX_P/N	B8 and B9	Lane 8± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP9_RX_P/N	B4 and B5	Lane 9± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP10_RX_P/N	Y10 and Y11	Lane 10± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP11_RX_P/N	Z12 and Z13	Lane 11± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP12_RX_P/N	Y14 and Y15	Lane 12± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP13_RX_P/N	Z16 and Z17	Lane 13± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP14_RX_P/N	Y18 and Y19	Lane 14± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP15_RX_P/N	Y22 and Y23	Lane 15± (M → C)	JESD Serial data transmitted from mezzanine and received by carrier
DP0_TX_P/N	C2 and C3	Lane 0± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP1_TX_P/N	A22 and A23	Lane 1± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP2_TX_P/N	A26 and A27	Lane 2± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP3_TX_P/N	A30 and A31	Lane 3± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP4_TX_P/N	A34 and A35	Lane 4± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP5_TX_P/N	A38 and A39	Lane 5± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP6_TX_P/N	B36 and B37	Lane 6± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP7_TX_P/N	B32 and B33	Lane 7± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP8_TX_P/N	B28 and B29	Lane 8± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP9_TX_P/N	B24 and B25	Lane 9± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP10_TX_P/N	Z24 and Z25	Lane 10± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP11_TX_P/N	Y26 and Y27	Lane 11± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP12_TX_P/N	Z28 and Z29	Lane 12± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine

Table 3-5. FMC+ Connector Description of the TSW14J59 (continued)

FMC+ Signal Name	FMC+ Pin	Standard JESD204 Application Mapping	Description
DP13_TX_P/N	Y30 and Y31	Lane 13± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP20_TX_P/N	Z8 and Z9	Lane 14± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
DP21_TX_P/N	Y6 and Y7	Lane 15± (C → M)	JESD Serial data transmitted from carrier and received by mezzanine
GBTCLK0_M2C_P/N	D4 and D5	DEVCLKA± (M → C)	Primary carrier-bound reference clock required for FPGA giga-bit transceivers. Equivalent to device clock.
GBTCLK1_M2C_P/N	B20 and B21	Alt. DEVCLKA± (M → C)	Alternate Primary Carrier-bound reference clock required for FPGA giga-bit transceivers. For use when DEVCLKA (M → C) is not available
Device Clock, SYSREF, and SYNC			
CORE_CLK_P/N	G6 and G7	DEVCLKB± (M → C)	Secondary carrier-bound device clock. Used for special FPGA functions such as sampling SYSREF
SYSREFP/N	G9 and G10	SYSREF± (M → C)	Carrier-bound SYSREF signal
SYNCB_IN	H31	SYNC	Carrier-bound SYNC signal
SYNCB_OUT	H32	SYNC	Mezzanine-bound SYNC signal
AFE_SYNCOUT	F10	AFE DAC SYNC	Carrier-bound SYNC signal for use in class 0/1/2 JESD204B systems
Special Purpose I/O			
GPIO_G12/G13	G12 and G13		Spare IO from FPGA pins AA13 and Y13. Enabled with jumper J42 removed
SPIO_SCLK	G31		Spare SPI SCLK from FPGA pin
GPIO_H25	H25		Spare IO from FPGA pin AF15. Enabled with jumper J42 removed
GPIO_H26	H26		Spare IO from FPGA pin AF14. Enabled with jumper J42 removed
GPIO_H28	H28		Spare IO from FPGA pin AF13. Enabled with jumper J42 removed
GPIO_H29	H29		Spare IO from FPGA pin AE13. Enabled with jumper J42 removed
SPIO_CSB_0	H34		Spare SPI chip select from FPGA pin Y15
SPIO_CSB_1	H35		Spare SPI chip select from FPGA pin Y16
SPIO_CSB_2	H37		Spare SPI chip select from FPGA pin H14
SPIO_CSB_3	H38		Spare SPI chip select from FPGA pin J14
PRSNT_M2C_L	H2	Present	I2C input. Indicates if a mezzanine card is present
SPI1_SCLK	D26		SPI clock from FPGA pin J15
SPI1_CSB	D27		SPI chip select from FPGA pin G12
HSPC_PRSNT_M2C_L	Z1	Present	I2C input. Indicates if a mezzanine card is present.
SPI1_SDIO_0	C26		Spare from FPGA pin W15
SPI1_SDIO_1	C27		Spare from FPGA pin W16
FMC_I2C_SCL	C30		Spare USB2.0 I/F
FMC_I2C_SDA	C31		Spare USB2.0 I/F
GPIO_G27/G28	G27, G28		Spare IO from FPGA pins W13 and W12. Enabled with jumper J42 removed
GPIO30	G30		Spare IO from FPGA pin AD14
SPI0_SDIO_0	G33		Spare SPI data I/O from FPGA pin AD13
SPI0_SDIO_1	G34		Spare SPI data I/O from FPGA pin AC14
SPI0_SDIO_2	G36		Spare SPI data I/O from FPGA pin AC13
SPI0_SDIO_3	G37		Spare SPI data I/O from FPGA pin AA15
12P0V	C35, C37, L36, L37, L40		12 V output supply
3P3V	C39, D32, D36, D38, D40, Z40		3.3V output supply
VADJ	E39, G39, H40, F40		Adjustable output supply. Default set to 1.8V.

3.3.3.3 JTAG Connectors

The TSW14J59EVM includes one industry-standard JTAG connector, P2, that connects to the JTAG port of the FPGA. The FPGA can be programmed using this connector or through the USB 3.0 interface. The USB 3.0 interface allows the FPGA to be programmed using the HSDC Pro software GUI. Every time the TSW14J59EVM is powered-down, the FPGA configuration is removed. The user must program the FPGA through the GUI after every time the board is powered-up. The FPGA can also be configured using the two on-board flash devices, U3 and U6.

The TSW14J59EVM also has a surface mount Digilent JTAG programmer, U5, which can be used to program the FPGA as well.

FLASH DEVICES The TSW14J59EVM includes two serial flash programming EEPROMS that can load FPGA firmware. Jumper J35 determines which EEPROM configures the FPGA when switch SW2 is pressed. If the EEPROMs are programmed, then, after power up, pressing SW2 loads the FPGA with the content of flash device U3 if J35 has a shunt between pins 1-2. The FPGA is programmed with the content of U6 if the shunt is between pins 2-3 or removed.

Program the Memory Device

To program U3 and U6 with new files, use the following steps:

Note

Install Vivado® version 2018.3 or later (Lab Edition)

1. Connect the TSW14J59 Capture card to the PC through a JTAG Xilinx Programmer cable. This is the JTAG connect P2.
2. Install a shunt on JP3.
3. Open the Vivado Installation:
   - Double click *Open Hardware Manager*.
4. In the Hardware Manager, left click on *Open target* and select *Auto Connect*.
5. The last step lists all the FPGAs connected to the PC through JTAG Programmer cables.
6. Right click on “xcku5p_0” -> click on *Add Configuration Memory Device*.

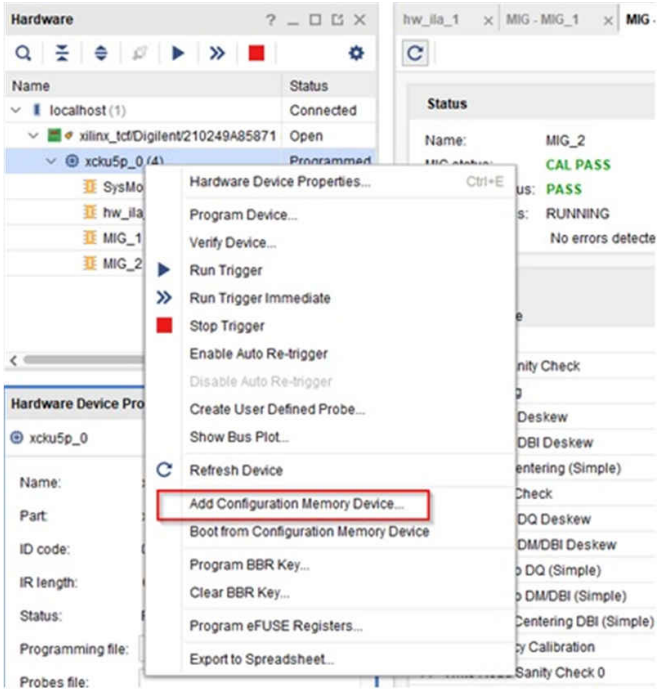

Figure 3-1. Add Configuration Memory Device

7. In the pop-up window, search for the “mt25qu256-spi-x1_x2_x4” component. Click the *OK* button.

8. Right click on device “mt25qu256-spi-x1_x2_x4”, and click on *Program Configuration Memory Device* (see Figure 3-2).

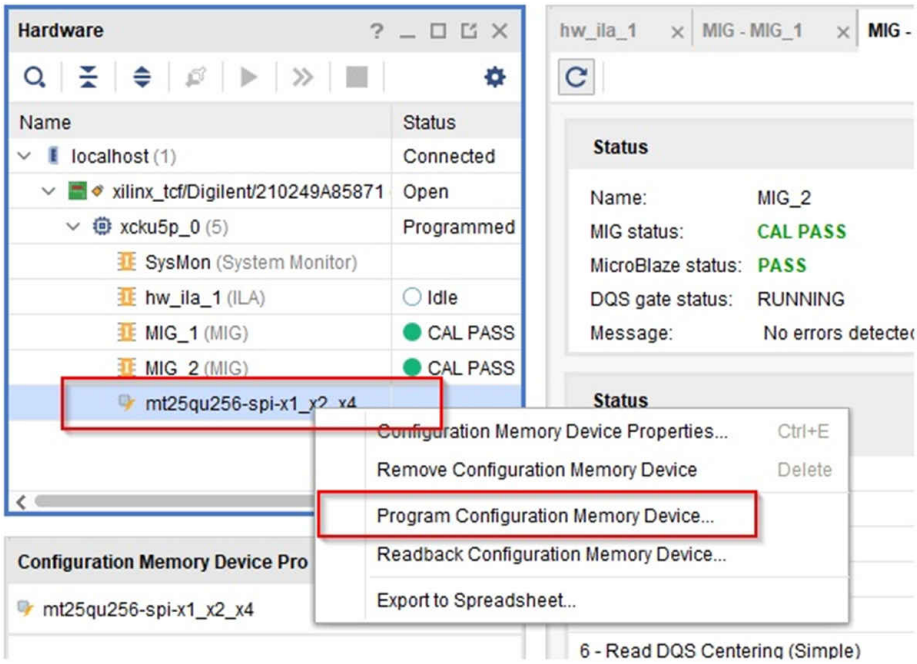

Figure 3-2. Programming Memory Device

9. To program U3, insert a shunt on J35 pins 1–2, open up the new “xx.mcs” file to be loaded, and check the following setup in the programming. Click the *OK* button when completed. Figure 3-3 illustrates the configuration file to be loaded. If the file loads properly, then a new message opens stating *Flash programming completed successfully*. Click on the OK button.

Figure 3-3. Config File

10. To program U6, place a shunt on J35 pins 2–3, open up the new “yy.mcs”file to be loaded and check the following setup in the programming. Click the *OK* button when completed.
11. After the programing is completed, click on SW2, FPGA RESET, to load the image to the FPGA. With the shunt on pins 2-3 of J35, the image stored in U6 is loaded into the FPGA. With the shunt on 1-2 of J35, the image stored in U3 is loaded into the FPGA.

3.3.3.4 USB3.0 I/O Connection

Control of the TSW14J59EVM is through the USB 3.0 connector J9 and a Cypress FX3 USB3.0 Controller. This provides the interface between the HSDC Pro GUI running on a PC using the Microsoft® Windows® operating system and the FPGA. This provides a high speed 32 bit parallel data interface between the USB3.0 controller and the FPGA.

For the computer, the drivers needed to access the USB port are included on the HSDC Pro GUI installation software that can be downloaded from the web. The drivers are automatically installed during the installation process. On the TSW14J59EVM, the USB3.0 port is used to identify the type and serial number of the EVM under test, load the desired FPGA configuration file, capture data from ADC EVMs, and send test pattern data to the DAC EVMs.

Power Monitor PMBUS Connector: The power monitor device, UCD90120A, is programmed though header J48. Using the TI Fusion GUI, the user can program the device and monitor all power rails used by the TSW14J59EVM. This interface also allows the user to monitor the status of the FPGA core power supply U1, TI part number TPS40428.

4 Software Start-Up

4.1 Installation Instructions

Follow the steps below:

1. Download the latest version of the *HSDC Pro GUI* to a local directory on a host PC. This is found on the TI website by entering *HIGH SPEED DATA CONVERTER PRO GUI INSTALLER*.
2. Unzipping the software package generates a folder called “High Speed Data Converter Pro - Installer vx.xx.exe", where x.xx is the version number. Run this program to start the installation.
3. Make sure to disconnect all USB cables from any TSW14xxx boards before installing the software.
4. Follow the on-screen instructions during installation.
5. Click on the *Install* button. A new window opens. Click the *Next* button.
6. Accept the License Agreement. Click on the *Next* button to start the installation. After the installer has finished, click the *Next* button one last time.
7. The installation is now complete. The GUI executable and associated files resides in the following directory: C:\Program Files\Texas Instruments\High Speed Data Converter Pro.
8. Power up the TSW14J59 under test. Connect the USB3.0 cable between the EVM and a host computer.
9. To start the GUI, click on the file called “High Speed Data Converter Pro.exe", located under C:\Program Files\Texas Instruments\High Speed Data Converter Pro.

Note

If an older version of the GUI has already been installed, then make sure to uninstall before loading a newer version. If the GUI detects that a newer version of the GUI is available online (http://www.ti.com/tool/DATACONVERTERPRO-SW), then the GUI assists the user with downloading the latest version from the TI website. The GUI automatically prompts the product website for the latest version every seven days but the latest version check can also be manually invoked through use of the pull-down menu *Help→Check for updates*.

Note

When new TI high-speed data converter EVMs or JESD204C_B interface modes become available that are not currently supported by the latest release of HSDC Pro GUI, the HSDCProv_xpxx_Patch_setup executable, available on the TI website under the High Speed Data Converter Pro Software product folder (http://www.ti.com/tool/DATACONVERTERPRO-SW), allows the user to add these to the GUI device list. After the patch has been downloaded, follow the on-screen instructions to run the patch. The software displays the files that are added. After running the patch, open HSDC Pro and the new parts and modes appear in the ADC and DAC device drop-down selection box. The patch is always specific to a core GUI version and do not work for a GUI version for which the patch was not explicitly created.

4.2 USB Interface and Drivers

- Connect a USB 3.0 cable between J9 of the TSW14J59EVM and a host PC.
- Connect the provided power cable between J38 of the EVM and a +12 VDC source rated for at least 3 A.
- Set SW1 to ON. LEDs D21 (+12 V present), D22 (power monitor supply), and several power status LEDs are turned on.

1. Click on the *High-Speed Data Converter Pro* icon that was created on the desktop panel, or go to C:\Program Files\Texas Instruments\High Speed Data Converter Pro and double click on the executable called *High Speed Data Converter Pro.exe* to start the GUI.
2. The GUI first attempts to connect to the EVM USB interface. If the GUI identifies a valid board serial number, then a pop-up opens displaying this value, as Figure 4-1 shows. The user can connect several TSW14J59 EVMs to one host PC, but the GUI can only connect to one at a time. When multiple boards are connected to the PC, the pop-up displays all of the serial numbers found. The user then selects which board to associate the GUI with.

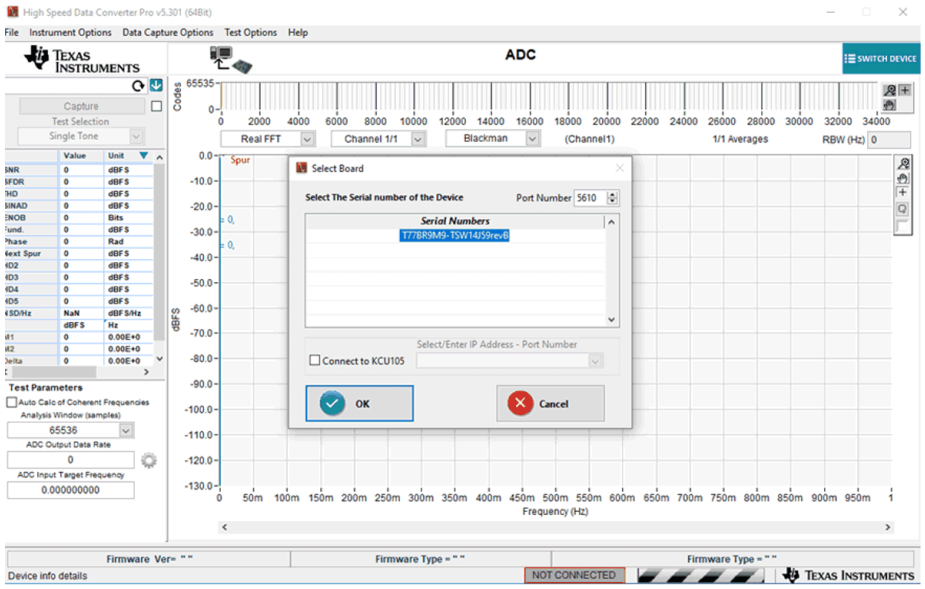

Figure 4-1. TSW14J59EVM Serial Number

3. Click the *OK* button to connect the GUI to the board. The top-level GUI opens and appears.
4. If the message *No Board Connected* opens, then double check the USB cable connections and that power switch SW1 is in the on position. Remove the USB3.0 cable from the board then re-install. Click on the *Instrument Option* tab at the top left of the GUI and selecting *Connect to the Board*. If this still does not correct this issue, then check the status of the host USB port.
5. When the software is installed and the USB cables are connected to the TSW14J59EVM and the PC, the TSW14J59 USB 3.0 converter is located in the Hardware Device Manager under the universal serial bus controllers as shown in Figure 4-2, labeled as Cypress FX3 USB StreamerExampleDevice. When the USB 3.0 cable is removed, this driver is no longer visible in the device manager. If the drivers are present in the device manager window and the software still does not connect, then remove the USB cable from the board then reconnect the cable. Attempt to connect to the board using the GUI. If the problem still exists, then cycle power to the board and repeat the prior steps.

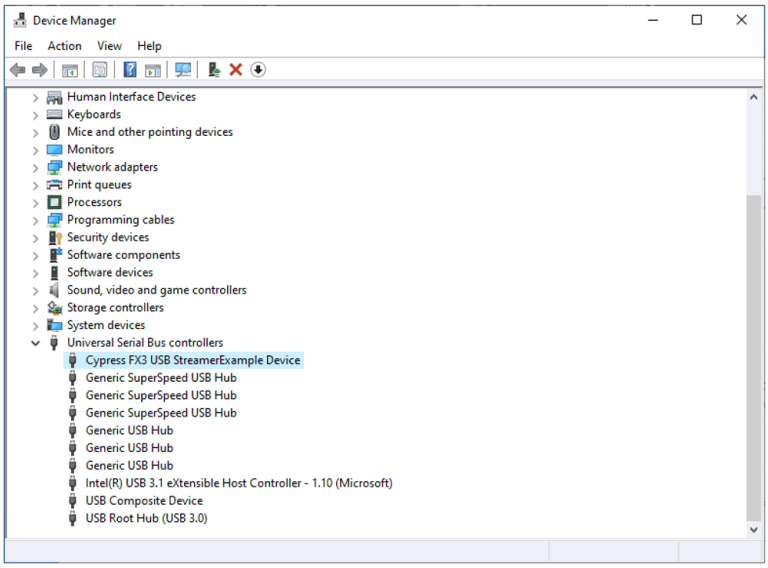

Figure 4-2. Hardware Device Manager

5 Downloading Firmware

The TSW14J59EVM has an Xilinx® Kintex® UltraScale® XCKU5P device that requires firmware to be downloaded every time power is cycled to operate if the on-board EEPROM's are not programmed. The firmware files needed are special .bin or .bit formatted files that are provided with the software package. The files used by the GUI reside in the directory called C:\Program Files\Texas Instruments\High Speed Data Converter Pro\14J59 Details\Firmware. Follow the steps below:

1. After connecting to the GUI, a new window opens.
2. Click on the drop down arrow which opens another window. Select either ADC, DAC or AFE, based on which data converter EVM is being tested.
3. After making this selection, click on the drop down arrow in the upper left of the GUI to select the device name and JMODE as shown in Figure 5-1.

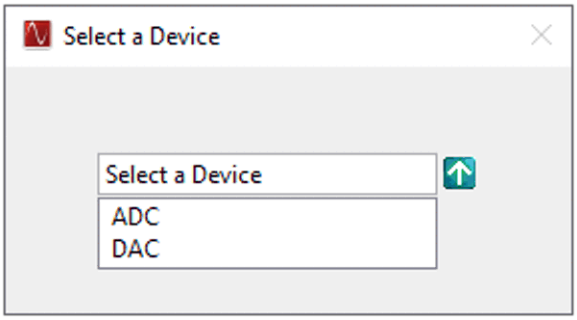

Figure 5-1. Select ADC or DAC Firmware to be Loaded

4. Click on the drop down arrow in the upper left of the GUI next to Select ADC and device mode.

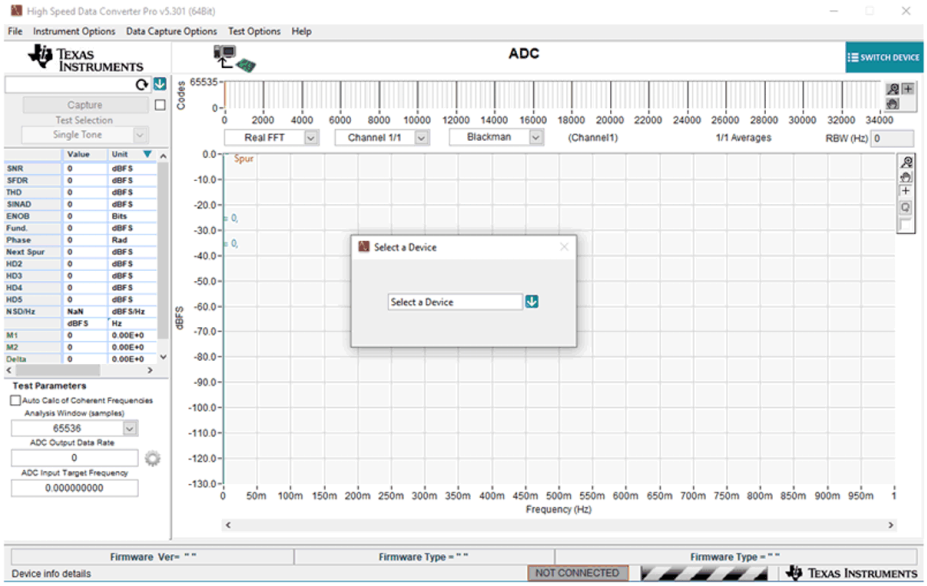

Figure 5-2. High-Speed Data Converter Pro GUI Top Level

5. Click on the two drop down arrows in the upper left of the GUI to select the device name and JMODE, for example, ADC12DJxx00 and JMODE30.

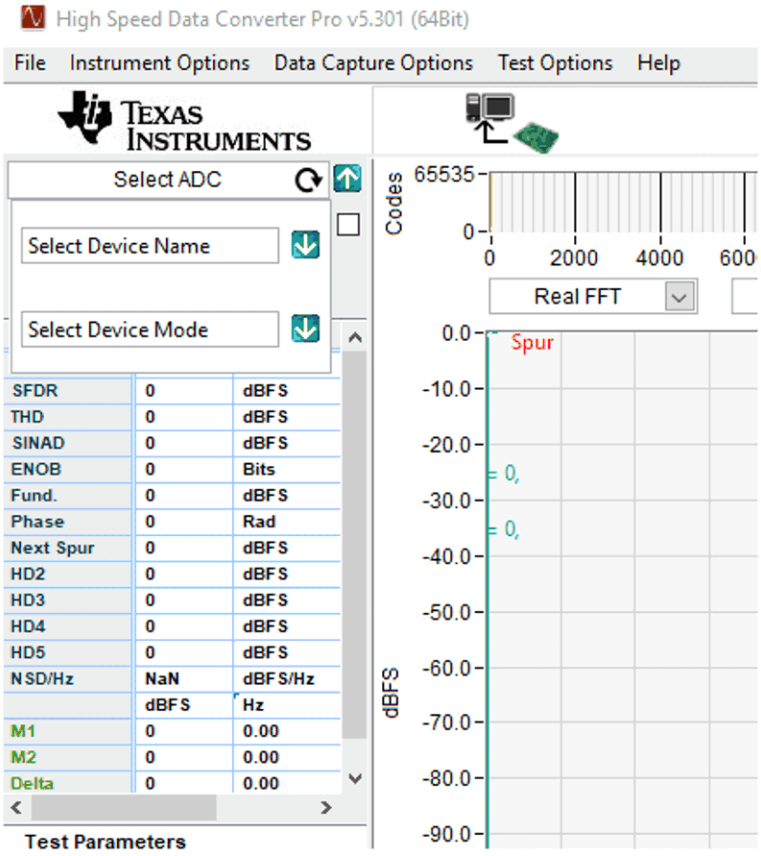

Figure 5-3. Select Device Under Test and Operating Mode

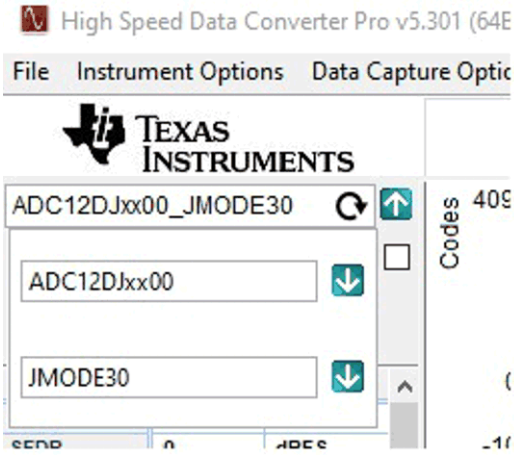

Figure 5-4. Example When Connected to an ADC12DJ3200EVM Using JMODE30

6. The GUI prompts the user to update the firmware for the ADC. Click *Yes*. The GUI displays the message *Downloading Firmware, Please Wait*. The software now loads the firmware from the PC to the FPGA, a process that takes about 6 seconds. Once completed, the GUI reports an Interface Type in the lower right corner and red LEDs DS16 and DS17 turns on.

For information regarding the use of the TSW14J59EVM with a TI ADC, DAC or AFE JESD204C_B serial interface EVM, consult the *High-Speed Data Converter Pro GUI User's Guide* and the individual EVM User's Guide, available on www.ti.com.

If the message appears as shown in c, then verify that all jumpers are in the default position and the power and USB status LEDs are illuminated. If the 12-V power status LED is off, then there can be a problem with the external power supply. Make sure this supply can source at least 3 A of current. If the available current is too low, then this can prevent the firmware from downloading. Unplug and re-install the USB connectors and try to connect to the board. If this fails, then cycle the power switch to re-initialize the power-up sequencer to try to correct this problem.

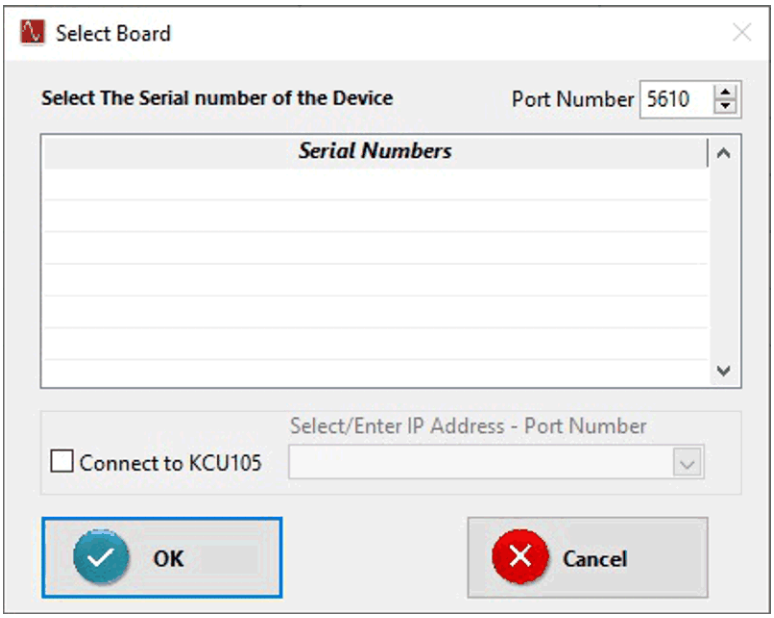

Figure 5-5. GUI Does Not Connect to EVM

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   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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西新宿三井ビル

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

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4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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