

Power-Supply Design for High-Speed ADCs

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ABSTRACT

System designers are increasingly faced with the challenge of maximizing power savings in their designs without compromising the performance of any system components like a high-speed data converter. Designers may move to battery-powered operation for applications like a handheld, software-defined radio or a portable ultrasound scanner, or they may simply shrink the product's form factor and then need to find ways to reduce heat.

One option for significantly reducing system power consumption is to optimize the power supply for the high-speed data converter. Recent advances in data-converter design and process technology allow newer ADCs to be driven directly from a switching power supply for maximum power efficiency.

Traditionally, system designers have used low-noise, low-dropout regulators (LDOs) between the switching regulator and the ADC to clean up output noise and switching-frequency spurs (see [Figure 1](#)). However, this clean power-supply design comes at the expense of additional power consumption because the LDO requires headroom for dropout voltage in order to function properly. The minimum dropout voltage is typically 200 to 500 mV, but in some systems it may be as high as 1 to 2 V when, for example, a 3.3-V rail for an ADC is generated from a 5-V switching supply using an LDO.

For a data converter that requires a 3.3-V rail, an LDO dropout voltage of 300 mV increases the ADC's power consumption by about 10%. This effect is amplified with data converters that have smaller process nodes and lower supply voltages. At 1.8 V, for example, the same 300-mV dropout voltage increases ADC power consumption by about 17% ($300\text{ mV}/1.8\text{ V}$). Therefore, eliminating the low-noise LDO from this chain can bring significant power savings. Removing the LDO also reduces the design's board space, heat, and cost.

This article demonstrates that high-speed ADCs from Texas Instruments (TI), including ultrahigh-performance 16-bit ADCs, can be powered directly from a switching regulator without noticeably degrading the ADC's performance. For this demonstration, two different data converters—one designed with high-performance-BiCOM technology (TI's ADS5483) and one with low-power-CMOS technology (TI's ADS6148)—were investigated for susceptibility to noise from a switching power supply. The rest of this article presents the results.

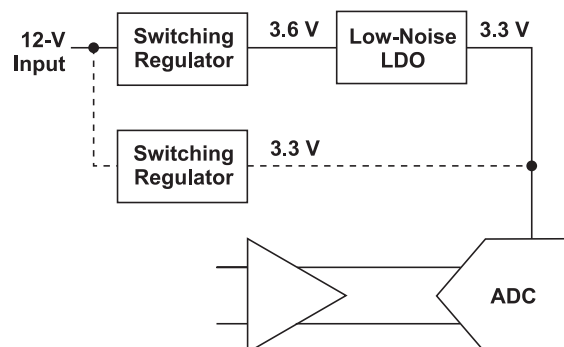


Figure 1. Moving From a Traditional Power Supply to a Maximum-Efficiency Supply

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1 BiCOM Technology—ADS5483

This process technology enables a high signal-to-noise ratio (SNR) and a high spurious-free dynamic range (SFDR) over a wide input-frequency range. BiCOM converters usually also have a lot of on-chip decoupling capacitors and a pretty good power-supply-rejection ratio (PSRR). The power-supply investigation was performed on the ADS5483 evaluation module (ADS5483EVM), which has an onboard power supply with TI's TPS5420 switching regulator (Sw_Reg); a low-noise LDO (TI's TPS79501); and an option to use an external lab supply. Five experiments were conducted with the setup variations shown in Figure 2 to determine the performance degradation that occurred when the ADS5483 was run directly from a switching regulator. Since the analog 5-V supply of the ADS5483 by far showed the most sensitivity to powersupply noise, this investigation ignored noise on the 3.3-V supplies. The PSRR listed in the ADS5483's data sheet supports this: The PSRR on the two 3.3-V supplies is at least 20 dB higher than that for the 5-V analog supply.

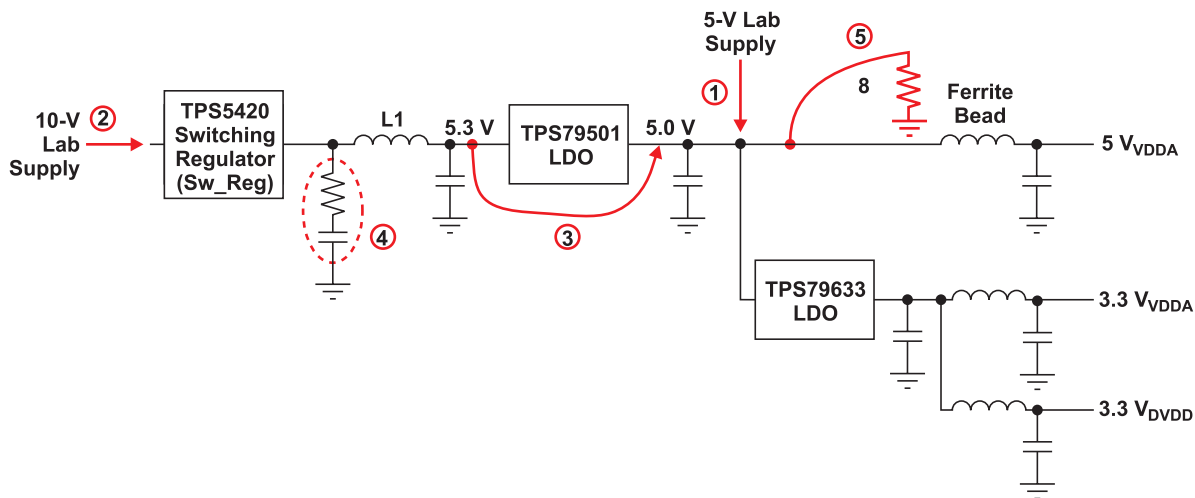


Figure 2. Power-Supply Setup for Five Experiments With ADS5483EVM

The setup variations for the five experiments were configured as follows:

Experiment 1—A 5-V lab supply was connected directly to the 5-V analog input, bypassing both the switching regulator (TPS5420) and the low-noise LDO (TPS79501). An onboard LDO (TI's TPS79633) was used to generate the 3.3-V rail for the ADS5483's less sensitive 3.3-V analog and digital supplies.

Experiment 2—A 10-V lab supply was connected to the TPS5420 buck regulator, which was configured with a 5.3-V output. This provided a 300-mV dropout voltage for the TPS79501, generating a 5-V supply rail.

Experiment 3—The TPS5420 was configured to generate a 5-V rail from a 10-V lab supply. The TPS79501 low-noise LDO was bypassed in this experiment. Figure 3a shows that the LDO as connected in Experiment 2 did a good job of reducing the spike on the 5.3-V output of the switching regulator. However, Figure 3b shows no significant difference in the output after the ferrite bead on the 5-V_{VDDA} rail.

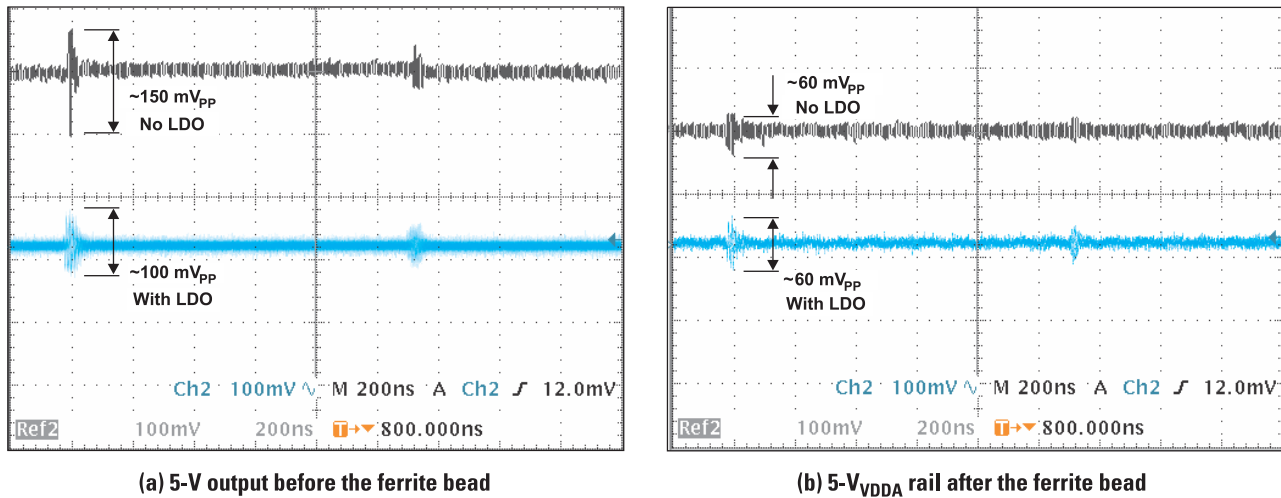


Figure 3. Scope-Shot Comparison of Experiments 2 (With LDO) and 3 (Without LDO)

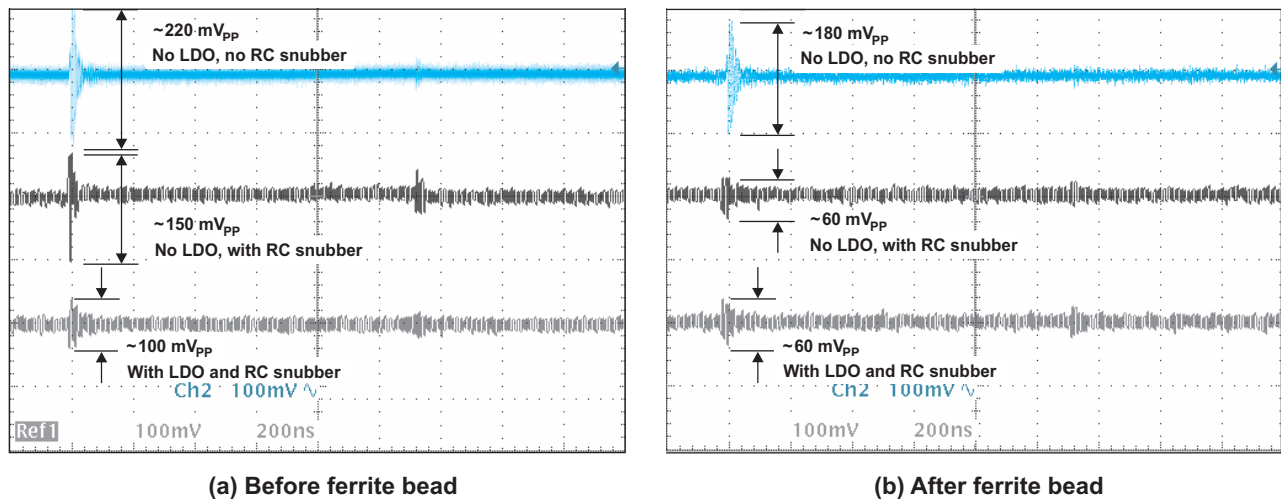


Figure 4. Power-Supply Noise on 5-V_{VDDA} Rail

Experiment 4—This experiment was configured the same way as *Experiment 3* except that the RC-snubber circuit at the output of the TPS5420 was removed, which caused increased ringing and larger switching-frequency spurs.

The impact of the RC-snubber circuit can clearly be observed in [Figure 4](#). While removing the LDO didn't show a noticeable difference after the ferrite bead, removing the RC-snubber circuit resulted in a larger voltage spike on the clean 5-V_{VDDA} rail going to the ADC.

The impact of the RC-snubber circuit will be examined in detail later on.

Experiment 5—An 8- Ω power resistor was connected to the 5-V supply, mimicking an additional load like a fieldprogrammable gate array (FPGA). The TPS5420 had to supply a higher output current and drive its internal switches harder, generating larger spurs on the output. This configuration was tested by repeating Experiments 2, 3, and 4.

Using a 135-MSPS sampling rate, the frequency sweeps for the SNR and SFDR are shown in [Figure 5](#). The maximum variation in SNR across the input frequencies from 10 to 130 MHz was about 0.1 dB. The SFDR results were very close also; at some input frequencies (e.g., 80 MHz), a degradation of 1 to 2 dB was observed.

A comparison of the FFT plots for the five experiments (see [Figure 6](#)) shows that there was no significant increase of the noise floor or the spur amplitudes. Using the LDO to clean up the switching noise made the output spectrum look almost identical to that of the clean 5-V lab supply. When the LDO was removed, two spurs from the switching regulator were observed that had a frequency offset of about 500 kHz from the 10-MHz input tone. The RCsnubber circuit reduced the amplitude of these spurs by about 3 dB, from about -108 dBc to about -111 dBc. This is quite a bit below the average spur amplitude of the ADS5483, which shows that the ADS5483 can be powered directly from a switching regulator without sacrificing SNR or SFDR performance.

1.1 Measurement Results

The five experiments were compared by using a frequency sweep of the input signal. The experiment was performed on three ADS5483EVMs with the sampling rate set to 135 MSPS and then to 80 MSPS. No significant differences in performance could be observed.

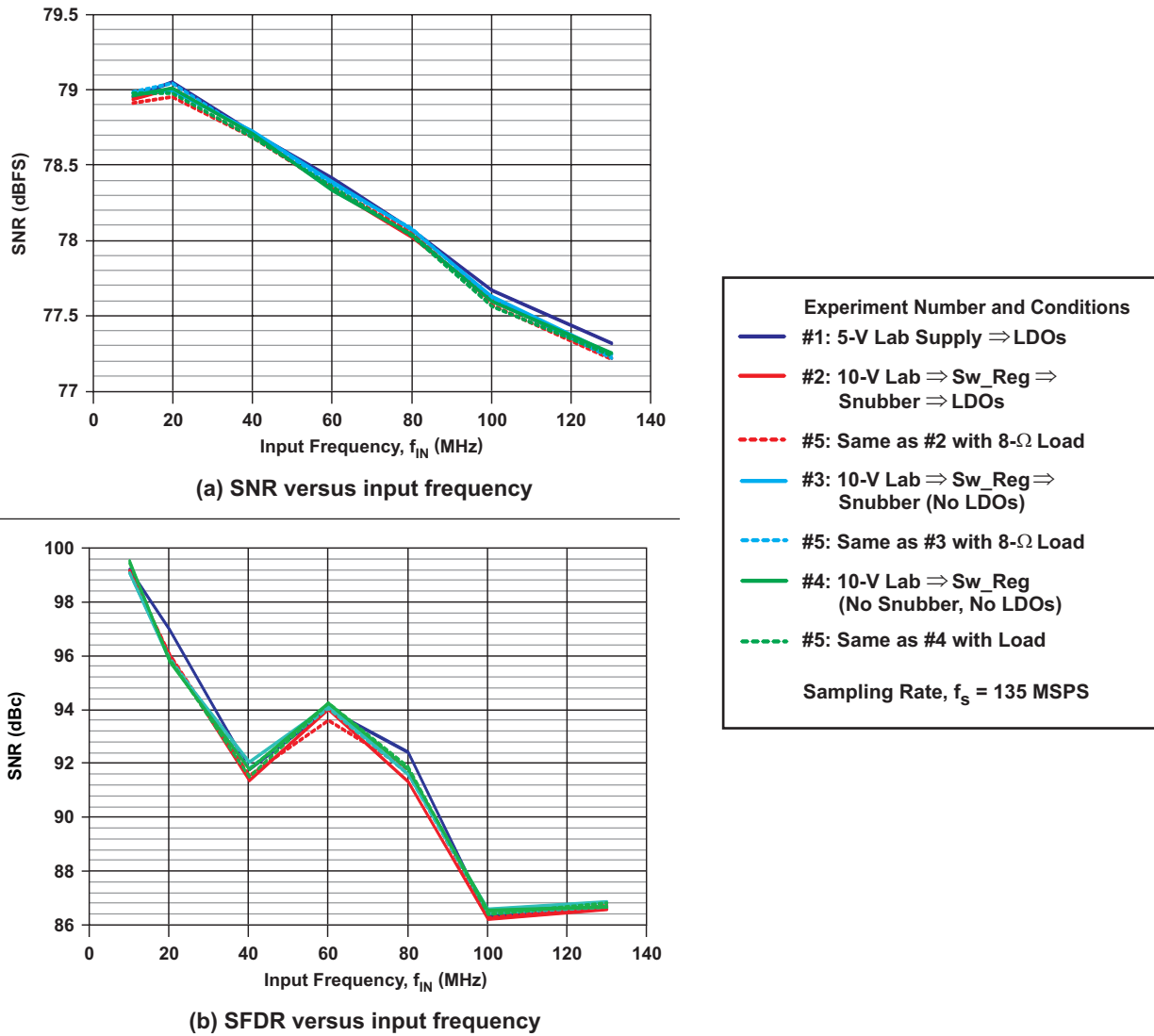


Figure 5. Input-Frequency Sweeps From 10 to 130 MHz

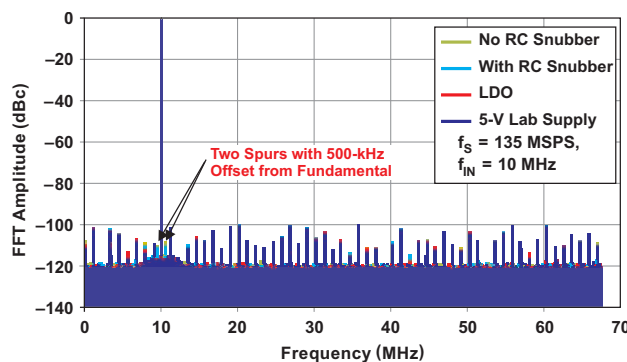
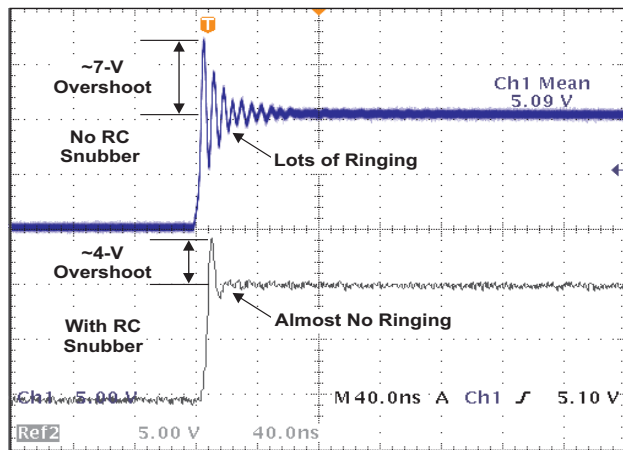
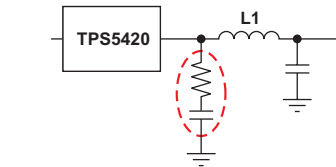


Figure 6. 65k-Point FFT Plots With Spurs at 500-kHz Offset



(a) Comparison of Output With and Without RC Snubber



(b) With RC-Snubber Circuit Added

Figure 7. TPS5420 Switching Regulator

1.1.1 RC Snubber

The output of a buck regulator can switch fairly large voltages at fairly fast switching speeds. In the investigation for this article, the input rail for the TPS5420 was set to 10 V, and quite a bit of overshoot and ringing at the output could be observed, as shown in Figure 7a. In order to absorb some of the energy from the reactance of the power circuit, the RC-snubber circuit was added to the output of the TPS5420 (Figure 7b). This circuit provided a high-frequency path to ground, which dampened the overshoot a little bit. Figure 7a illustrates that the RC snubber reduced overshoot by about 50% and almost completely eliminated the ringing. Component values of $R = 2.2 \Omega$ and $C = 470 \text{ pF}$ were chosen. The switching frequency of the regulator can range from 500 kHz up to about 6 MHz, depending on the manufacturer, so the R and C values may need to be adjusted. This solution comes at the expense of some additional AC-power dissipation in the shunt resistor (although resistance is very small), which reduces the overall power efficiency of the regulator by less than 1%.

FFT plots normalized to the 10-MHz input signal were generated to compare Experiments 1 through 4 (see Figure 8). The spur from the TPS5420 is clearly visible at an offset of about 500 kHz. The snubber decreases the spur amplitude by about 3 dB, and the low-noise LDO completely eliminates it. It is important to note that the spur amplitude with the RC snubber (and no LDO) is about -112 dBc , far below the average spur amplitude of the ADS5483, so the SFDR performance is not degraded.

In Experiment 5, an 8- Ω power resistor was added to the 5- V_{VDDA} rail to mimic a heavy load on the supply. The normalized FFT plots (Figure 9) don't show much change. With the RC snubber removed, the spur increases by about 4.5 dB; yet it is still far below the average spur amplitude.

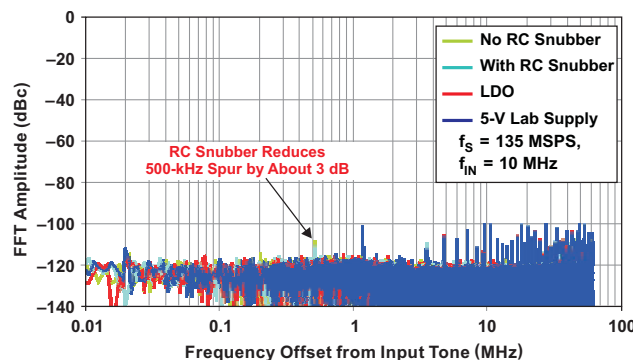


Figure 8. Normalized FFT Plots for Experiments 1 Through 4

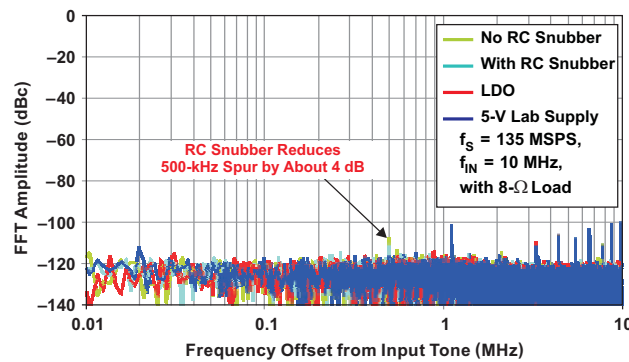


Figure 9. Normalized FFT Plots With Added 8-Ω Load

2 CMOS Technology—ADS6148

High-speed data converters are typically developed with CMOS technology when the key concern is to reduce power consumption as much as possible while still maintaining good SNR and SFDR performance. However, the PSRR of CMOS converters is usually not as good as that of BiCOM ADCs. The ADS6148 data sheet lists a PSRR of 25 dB, while the ADS5483's PSRR is listed as 60 dB on the analog input-supply rail.

The ADS6148EVM comes with an onboard power supply consisting of a switching regulator (TPS5420) and a lownoise, 5-V-output LDO (TPS79501), followed by low-noise LDOs for the 3.3-V and 1.8-V power rails (Figure 10). Similar to the five experiments conducted with the ADS5483EVM, the following five additional experiments were performed with the ADS6148EVM, focusing only on the noise on the 3.3- V_{VDDA} rail. Experiments with an external TPS5420 on the 1.8- V_{DVDD} rail showed an insignificant effect on the SNR and SFDR performance.

Experiment 6—A 5-V lab supply was connected to the input of two low-noise LDOs, one with a 3.3-V output and one with a 1.8-V output. The LDOs did not add any significant noise to the lab supply.

Experiment 7—A 10-V lab supply was connected to the TPS5420 buck regulator, which was configured with a 5.3-V output like Experiment 2 with the ADS5483. The TPS79501 generated a filtered 5.0-V rail, which fed the 3.3-V-output and 1.8-V-output LDOs as shown in Figure 10.

Experiment 8—All the LDOs for the 3.3- V_{VDDA} rail were bypassed. The TPS5420 was configured with a 3.3-V output directly connected to the 3.3- V_{VDDA} rail. The TPS79601 generated the 1.8- V_{DVDD} rail and was powered from an external 5-V lab supply.

Experiment 9—This experiment was configured the same way as Experiment 8 except that the RC-snubber circuit at the output of the TPS5420 was removed.

Experiment 10—A 4-Ω power resistor was connected to the 3.3-V output of the TPS5420. This drastically increased the output current of the TPS5420, simulating an additional load. Furthermore, it caused higher switching spurs and more ringing like Experiment 5 with the ADS5483. Figure 11 shows some of the waveforms for the 3.3- V_{VDDA} output that resulted from Experiments 7, 8, and 9. There is little difference in spike amplitudes with or without the LDOs, but the RC snubber provides a 60% decrease in spike noise.

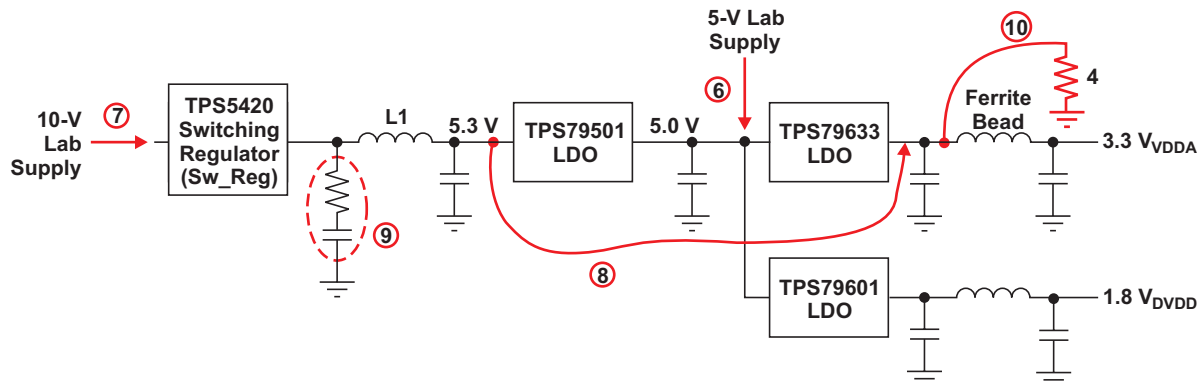


Figure 10. Power-Supply Setup for Five Experiments With ADS6148EVM

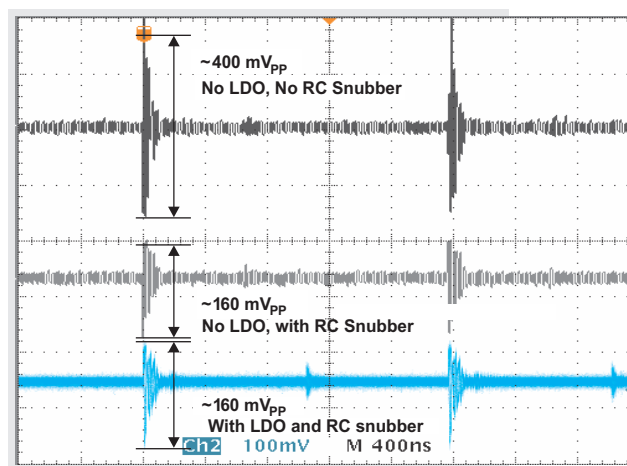


Figure 11. Scope-Shot Comparison of Experiments on 3.3-V_{VDDA} Rail Measured After Ferrite Bead

2.1 Measurement results

The susceptibility of the ADS6148 to power-supply noise was examined by comparing Experiments 6 through 10 with a frequency sweep of the input signal. The experiments were performed on three ADS6148EVMs with the sampling rate (f_s) set to 135 MSPS and then to 210 MSPS. No significant differences in performance could be detected.

Using a 135-MSPS sampling rate, the frequency sweeps for the SNR and SFDR are shown in Figure 12. The maximum variation in SNR across input frequencies of up to 300 MHz was 0.1 to 0.2 dB. However, once the RC-snubber circuit was removed, the noise increased significantly, reducing the SNR by about 0.5 to 1 dB.

Figure 12 shows the SFDR variation across the input frequencies for the five ADS6148 experiments. No significant degradation can be observed.

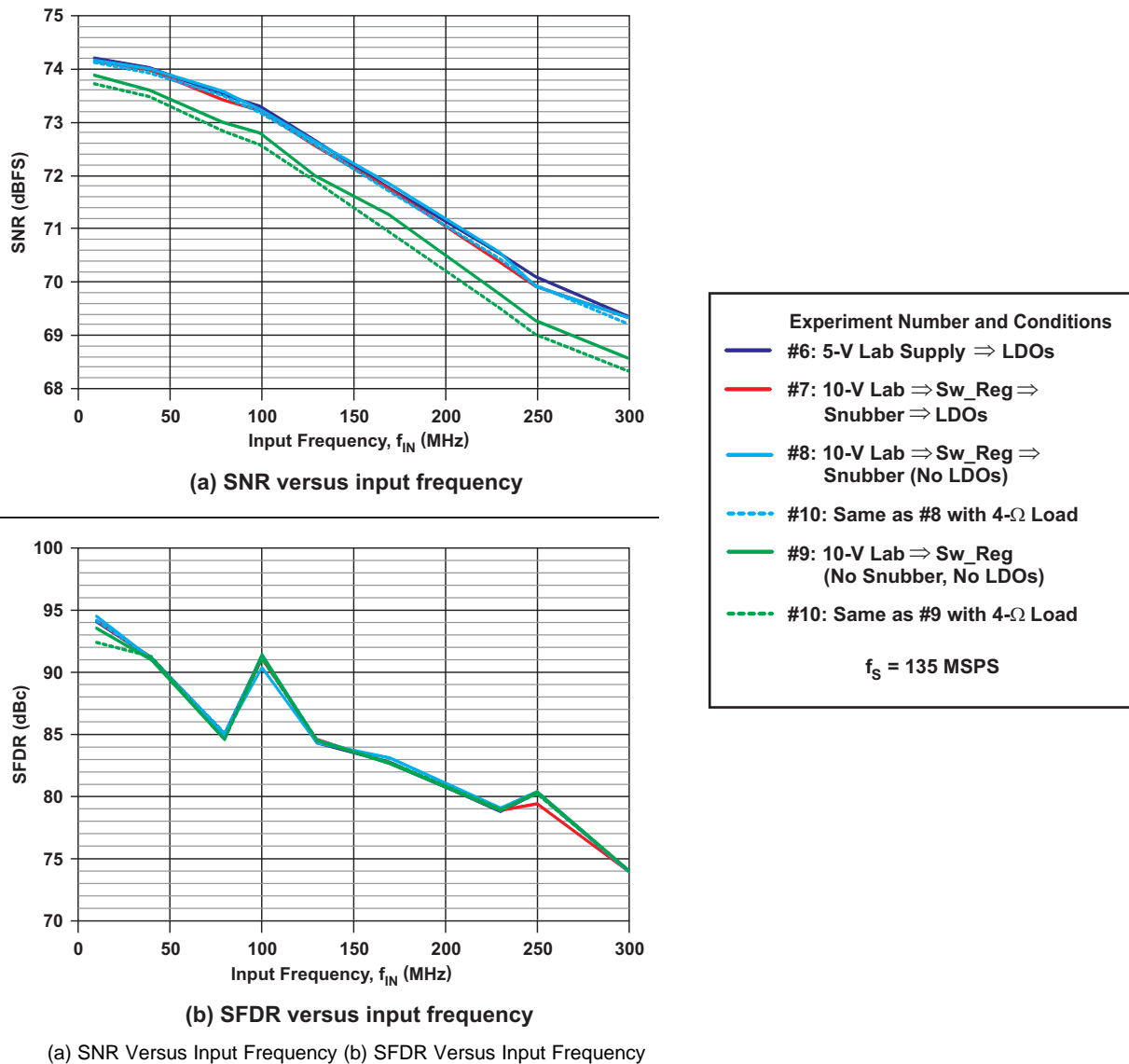


Figure 12. Input-Frequency Sweeps From 10 to 300 MHz

Comparing the FFT plots in Figure 13 shows why the SNR without the RC snubber is degraded a bit. When the RC-snubber circuit was removed, numerous little spurs spaced at intervals of about 500 kHz (the TPS5420's switching frequency) were visible in the output spectrum of the ADS6148, as illustrated in Figure 13. The little spurs were more dominant and degraded the SNR more than with the ADS5483 because of the inherent lower PSRR of the ADS6148. However, the FFT plots in Figure 13 also show that the added RC-snubber circuit compensated for that deficiency very well.

The normalized FFT plots in Figure 14 show that the spurs from the switching regulator were about 5 to 6 dB higher than the average noise floor of the ADC. They were too low to cause any SFDR degradation but definitely affected the SNR of the ADC.

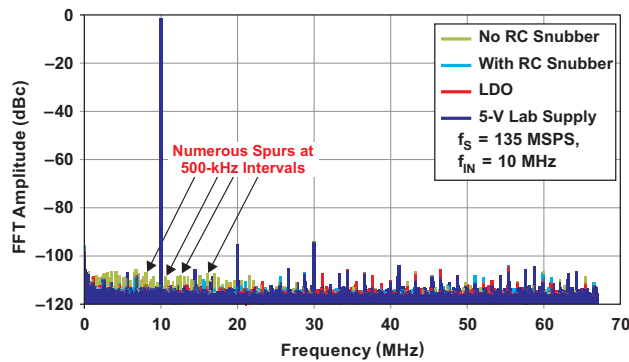


Figure 13. 65k-Point FFT Plots With Numerous Spurs

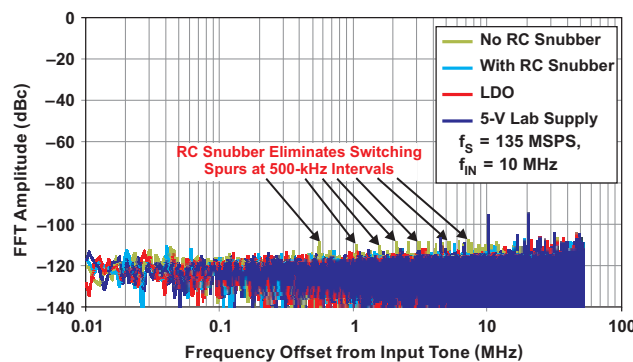


Figure 14. Normalized FFT Plots Show the Benefit of Using an RC Snubber

3 Conclusion

The experiments presented in this article have shown that data converters designed with high-performance-BiCOM technology and low-power-CMOS technology can be powered directly from a switching regulator. However, necessary precautions such as careful layout and an appropriate RC-snubber filter may be required to eliminate switching-frequency spurs from the ADC's output and the resulting degradation of the SNR. A very small SNR degradation may well be worth the big power savings achieved by removing the LDO from the power-supply chain.

4 References

- power.ti.com
- www.ti.com/product/partnumber
 Replace *partnumber* with [ADS5483](#), [ADS6148](#), [TPS5420](#), [TPS79501](#), [TPS79601](#), or [TPS79633](#).

Revision History

Changes from Original (February 2010) to A Revision	Page
• Changed document to the latest TI application report template.....	1

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