MOSFET power losses and how they affect power-supply efficiency

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Power-supply efficiency is a critical criterion for today's cloud-infrastructure hardware. The efficiency of the chosen power solutions relates to system power loss and the thermal performance of integrated circuits (ICs), printed circuit boards (PCBs), and other components, which determines the power-usage effectiveness of a data center.

This article revisits some of the basic principles of power supplies and then addresses how MOSFETs—the power stage of any switching-voltage regulator—affect efficiency. For the linear regulator shown in Figure 1, power loss and efficiency are defined by Equations 1 and 2.

$$\text{Power Loss} = (V_{IN} - V_{OUT}) \times I_L \tag{1}$$

$$\text{Efficiency} = \frac{V_{OUT} \times I_L}{V_{IN} \times I_L} = \frac{V_{OUT}}{V_{IN}} \tag{2}$$

In the ideal switching regulator shown in Figure 2, the current is zero when the switch is open and the power loss is zero, thus V_{IN} is being chopped. When the switch is closed, the voltage across it is zero and the power loss is also zero. An ideal switch implies zero losses, thus offering 100% efficiency. However, components are not ideal, as is illustrated in the following examples.

An efficient switching regulator results in less heat dissipation, which reduces system cost and size for elements such as heat sinks, fans and their assembly. In battery-operated systems, less power loss means that these devices can use the same battery for a longer run time because the device pulls less current from the battery.

To consider the various factors that contribute to efficiency, the focus of this article is on the step-down (buck) DC/DC converter topology, which is the most popular switching-regulator topology in today's cloud infrastructure systems. Figure 3 shows the key power-loss contributors in a buck converter: conduction losses, switching losses, and static (quiescent) losses.

MOSFETs have a finite switching time, therefore, switching losses come from the dynamic voltages and currents the MOSFETs must handle during the time it takes to turn on or off.

Switching losses in the inductor come from the core and core losses. Gate-drive losses are also switching losses because they are required to turn the FETs on and off. For the control circuit, the quiescent current contributes to power loss; the faster the comparator, the higher the bias current. For the feedback circuit, the voltage divider, error amplifier and comparator bias currents contribute to power loss. Megaohm resistors cannot be used to reduce

Figure 1. Typical linear regulator

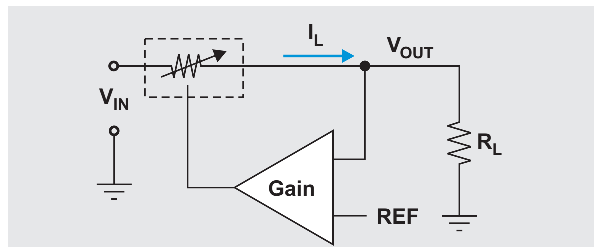


Figure 2. Ideal switching regulator with the switch open

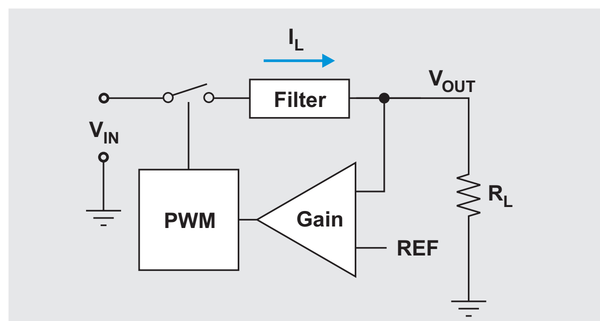
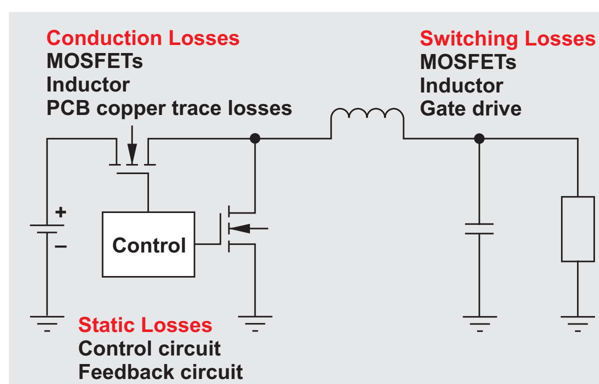


Figure 3. Power-loss contributors in a buck switching regulator



power loss because of the bias current into the feedback circuit. Figure 4 shows a basic switching circuit and Equation 3 is used to calculate conduction losses for Q1 or Q2.

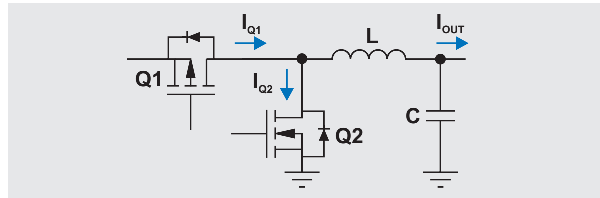
$$P_{CON} = R_{DS(on)} \times I^2_{QSW(RMS)}$$
$$= R_{DS(on)} \times \frac{V_{OUT}}{V_{IN}} \times \left(I^2_{OUT} + \frac{I^2_{RIPPLE}}{12} \right) \quad (3)$$

Note that R is the $R_{DS(on)}$ of the selected MOSFET, I is the root-mean-square (RMS) current through the MOSFET, and that neither of these is a function of switching frequency. In general, a higher switching frequency and higher input voltage require a lower QG (gate charge) to cut down the switching losses in the switch MOSFET (Q1).

For a rectifier MOSFET (Q2), low $R_{DS(on)}$ is most important, but don't ignore the gate power. Also, changing the MOSFET $R_{DS(on)}$ changes the duty cycle (D), which effects RMS currents and losses elsewhere. The inductor current also affects MOSFET conduction loss.

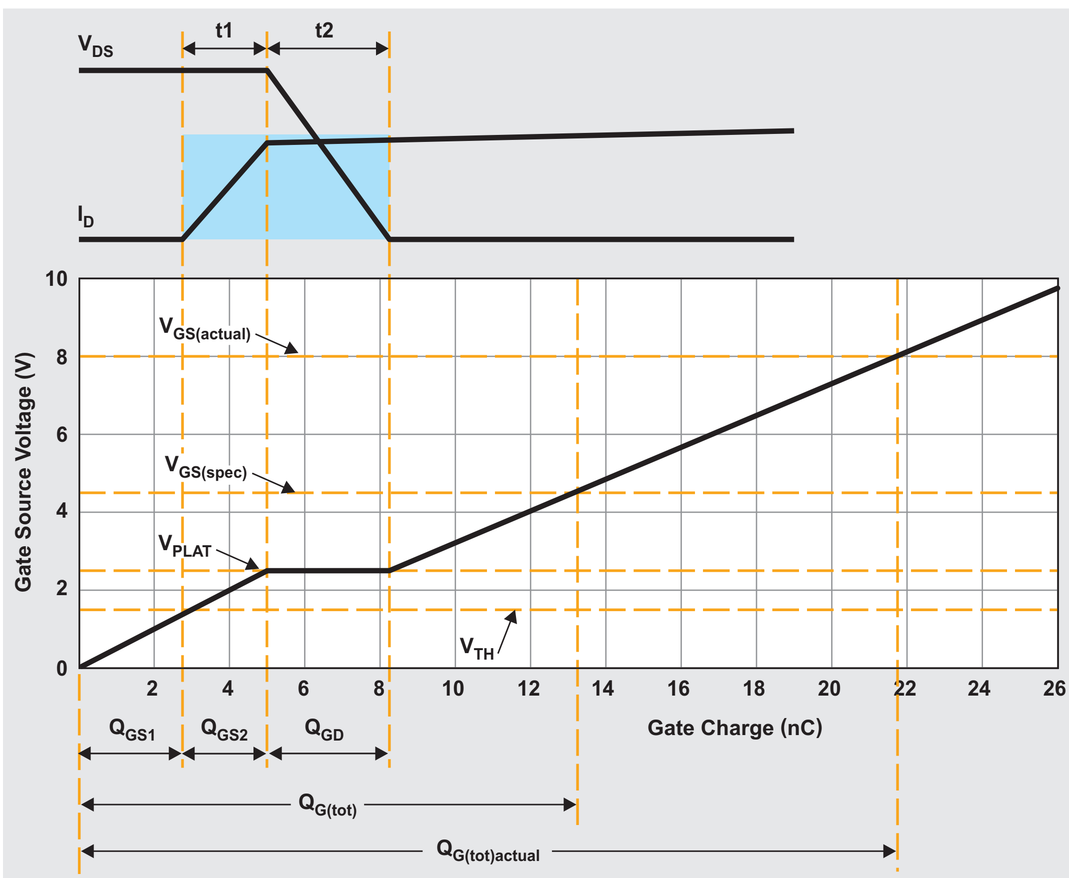
The high-side MOSFET (Q1) switching losses are evaluated first in Figure 5 because they are more complex.

Figure 4. MOSFET conduction losses



Relationships for Figure 5 to derive loss equation:
$E_{t1} = (V_{DS} \times I_D/2) \times t1$,
$E_{t2} = (V_{DS}/2 \times I_D) \times t2$,
$P_{SW} = 2 \times (E_{t1} + E_{t2}) \times f_{SW}$,
$t1 = Q_{GS2}/I_G$,
$t2 = Q_{GD}/I_G$,
V_{PLAT} = Miller plateau,
V_{TH} = Gate-to-source threshold voltage,
$I_G = Cdv/dt$,
$Q = C \times V$,
dt = t1 or t2, and
$V_{GS(actual)}$ is the actual gate-to-source drive voltage driving the MOSFET.

Figure 5. MOSFET switching losses



MOSFET switching losses are a function of load current and the power supply's switching frequency as shown by Equation 4.

$$P_{SW} = V_{IN} \times I_{OUT} \times f_{SW} \times \frac{(Q_{GS2} + Q_{GD})}{I_G} \quad (4)$$

where $V_{IN} = V_{DS}$ (drain-to-source voltage), $I_{OUT} = I_D$ (drain current), f_{SW} is the switching frequency, Q_{GS2} and Q_{GD} depend on the time the driver takes to charge the FET, and I_G is the gate current.

Switch-MOSFET gate losses can be caused by the energy required to charge the MOSFET gate. That is, the $Q_{G(TOT)}$ at the gate voltage of the circuit. These are both turn-on and turn-off gate losses.

Most of the power is in the MOSFET gate driver. Gate-drive losses are frequency dependent and are also a function of the gate capacitance of the MOSFETs. When turning the MOSFET on and off, the higher the switching frequency, the higher the gate-drive losses. This is another reason why efficiency goes down as the switching frequency goes up.

Larger MOSFETs with lower $R_{DS(on)}$ provide lower conduction losses at the cost of higher gate capacitances, which results in higher gate-drive losses. These losses can be significant for power-supply controllers (with external MOSFETs) at very high switching frequencies in the multiple-megahertz region. There is no known method for calculating a "best" Q_G and $R_{DS(on)}$ in a given situation, although figure-of-merit (FOM) numbers are typically mentioned in data sheets as (FOM = $R_{DS(on)} \times Q_G$).

For the switch MOSFET shown in Figure 6, a lower gate charge (Q_G) in Equation 5 enables lower power loss and a faster switching time; however, this contributes to more parasitic turn-on of the rectifier MOSFET. A happy medium can be obtained in the design to accommodate these trade-offs.

$$P_{GATE} = Q_{G(TOT)} \times V_G \times f_{SW} \quad (5)$$

There are also general gate losses as shown in Figure 7. The MOSFET effect on the gate-driver IC, or a pulse-width modulation (PWM) controller with an integrated gate driver, add to the power-dissipation losses.

As shown by Equation 6, gate-drive losses do not all occur on the MOSFET.

$$P_{DRV} = \frac{V_{G\_DRV} \times Q_{G(tot)} \times f_S}{2} \times \left(\frac{R_{GHI}}{R_{GHI} + R_G + R_{GI}} + \frac{R_{GLO}}{R_{GLO} + R_G + R_{GI}} \right) \quad (6)$$

where:

- P_{DRV} is the total gate drive loss divided to calculate the driver loss,
- R_{GHI} is turn on of the driver,
- R_{GLO} is the turn off of the driver,
- replacing R_{GHI} with R_G is the loss in the gate resistor,
- replacing R_{GHI} with R_{GI} is the switching FET loss,
- higher Q_G increases driver dissipation, and
- adding external R_G reduces internal driver dissipation because it reduces the overall resistance path to the MOSFET gate.

Figure 6. Switch MOSFET gate losses

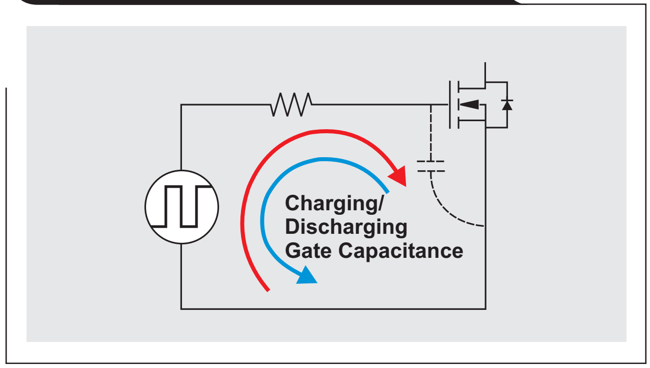


Figure 7. General gate losses

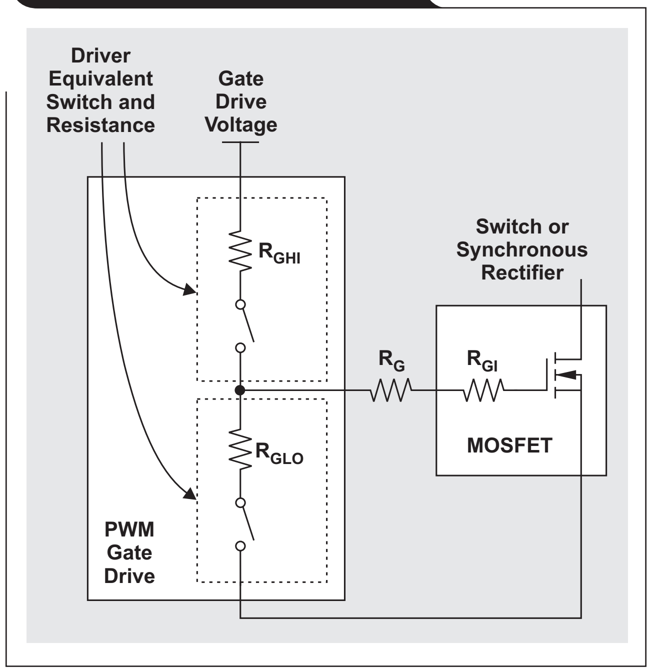


Figure 8 shows the various contributors that affect total switch MOSFET losses.

Now consider the rectifier (synchronous) MOSFET total and conduction losses. Power loss in a rectifier MOSFET consists of conduction losses (P_{CON}), body-diode conduction losses (P_{BD}), and gate losses (P_{GATE}).

There are no switching losses because of the body diode. The body diode conducts and the voltage across the FET is the diode voltage, which is zero. The body diode ensures zero-voltage switching per Equation 7.

$$P_{QSR} = P_{CON} + P_{BD} + P_{GATE} \tag{7}$$

Conduction losses are simple I^2R losses when the MOSFET channel conducts per Equation 8.

$$P_{CON} = R_{DS(on)} \times \left[1 - \frac{V_{OUT}}{V_{IN}} - \left(t_{DLYUpLo} + t_{DLYLoUp}\right) \times f_{SW}\right] \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12}\right) \tag{8}$$

where:

- R is the $R_{DS(on)}$ of the selected MOSFET,
- I is the RMS current through the MOSFET,
- $t_{DLYUpLo}$ is the delay between the upper MOSFET turning off and the lower MOSFET turning on, and
- $t_{DLYLoUp}$ is the delay between the lower MOSFET turning off and the upper MOSFET turning on.

The rectifier MOSFET also has body-diode losses. The average body-diode current can be calculated during dead time.

The blue waveform in Figure 9 shows the dead time, which is the time between when the high-side FET turns off and the low-side FET (rectifier FET) turns on. We want the average current in the switching cycle. The output inductor (L) dictates the slope of the dotted line, I_{BD1}, I_{BD2}, I_{BD3}. This slope is the average current through the body diode.

Equations 9a through 9e can be used to determine the body-diode current:

$$I_{BD(1)} = I_{BD(PK)} - \frac{V_O \times t_{DLYUpLo}}{L} \tag{9a}$$

$$I_{BD(2)} = I_{BD(PK)} - I_{RIPPLE} + \frac{V_O \times t_{DLYLoUp}}{L} \tag{9b}$$

$$I_{AVGUpLo} = I_{BD(PK)} - \frac{V_O \times t_{DLYUpLo}}{2 \times L} \tag{9c}$$

$$I_{AVGLoUp} = I_{BD(PK)} - I_{RIPPLE} + \frac{V_O \times t_{DLYLoUp}}{2 \times L} \tag{9d}$$

$$I_{BD(AVG)} = \left[\begin{array}{l} \left(I_{BD(PK)} - \frac{V_O \times t_{DLYUpLo}}{2 \times L}\right) \times t_{DLYUpLo} \\ + \left(I_{BD(PK)} - I_{RIPPLE} + \frac{V_O \times t_{DLYLoUp}}{2 \times L}\right) \\ \times t_{DLYLoUp} \end{array}\right] \times f_{SW} \tag{9e}$$

Figure 8. Total switch MOSFET losses

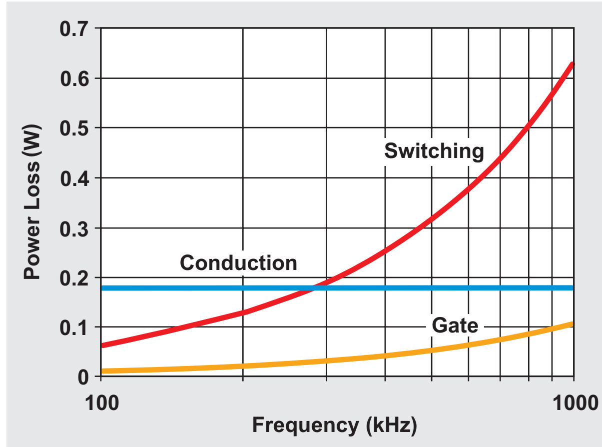
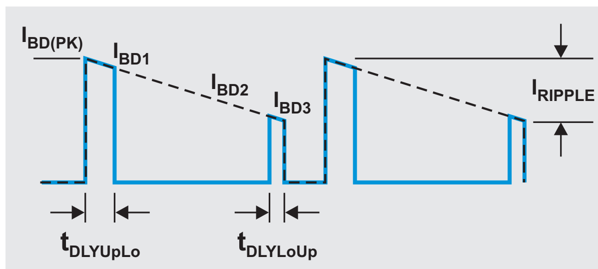


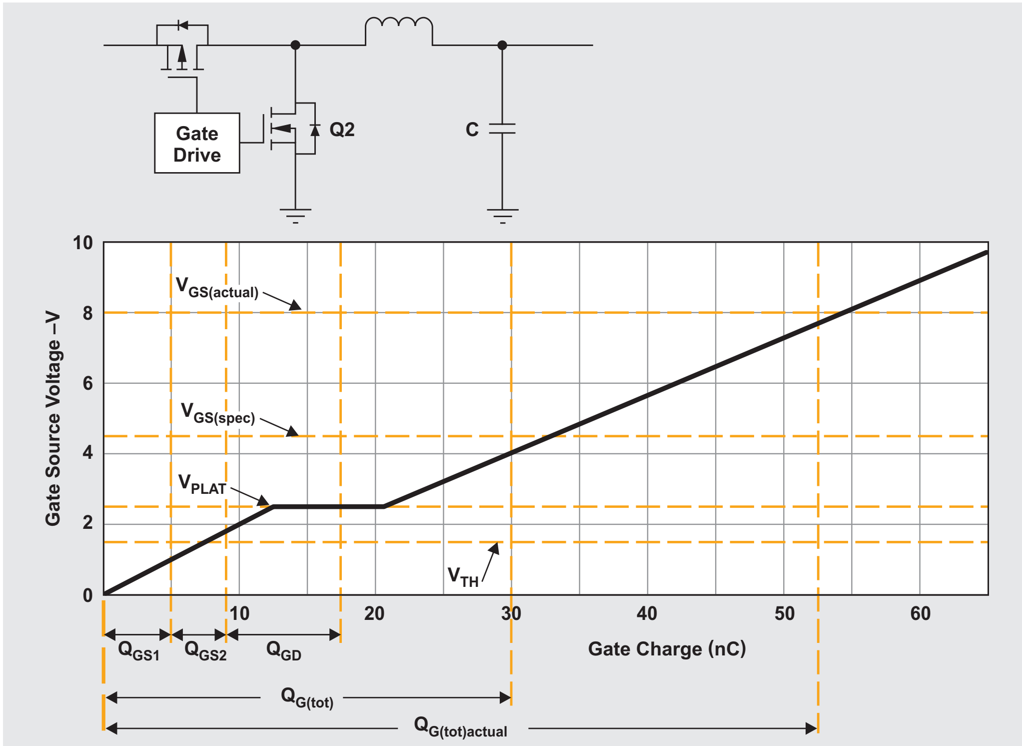
Figure 9. Rectifier MOSFET body-diode current



Equation 10 can be used to approximate the body-diode power loss.

$$P_{BD} \approx V_F \times I_{OUT} \times \left(t_{DLYUpLo} + t_{DLYLoUp}\right) \times f_{SW} \tag{10}$$

Figure 10. Rectifier MOSFET gate driver and losses



The final consideration in Figure 10 is for the gate losses of the rectifier MOSFET (Q2). Gate losses are calculated in the same manner as with the switch MOSFET. Losses can be significant because of a higher gate charge.

Figure 11 shows the various contributors that affect total losses attributed to the rectifier MOSFET.

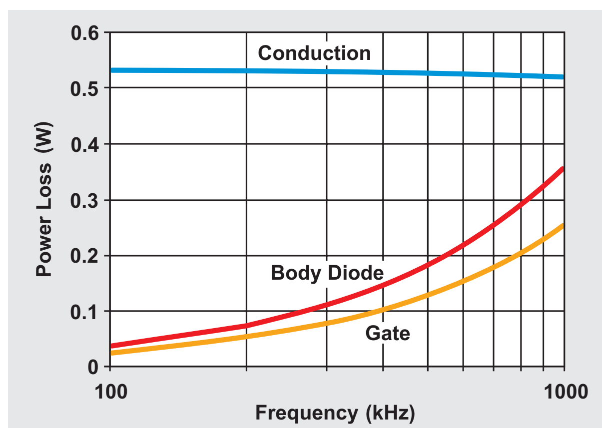
Conclusion

The efficiency of a synchronous step-down power converter with integrated or external MOSFETs can be optimized when the designer understands the parameters that affect efficiency and the specifications to look for in data sheets.

In the absence of an ideal power converter, the designer has to make trade-offs and optimize the parameters that affect power-supply efficiency.

A wide portfolio of discrete MOSFETs is available from Texas Instruments, including power blocks (dual-MOSFETs in one package) and power stages (gate driver and dual-MOSFETs in one package). Power supply control ICs that use MOSFETs are buck PWM controllers and SWIFT™ integrated MOSFET buck converters (both analog and PMBus™). An example of a PWM controller is the TPS40428 dual-output/dual-phase, PMBus, driverless PWM controller that is paired with the CSD95378B NexFET™ smart power stage An example of a SWIFT integrated-FET converter is the TPS544C25, a 30-A PMBus buck converter with frequency synchronization.

Figure 11. Total rectifier MOSFET losses



This device includes integrated MOSFETs where all the design equations of this article may be applied.

Related Web sites

Product information:
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